ESD PROTECTION DESIGN FOR LOW TRIGGER VOLTAGE AND HIGH LATCH-UP IMMUNITY

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***Abstract*—An embedded silicon-controlled rectifier (SCR) protection structure is proposed with a compatible CMOS layout. It first turns on like a gate-coupled NMOSFET, and then provides second-snapback conduction by a parasitic SCR. As compared with a conventional gate-ground NMOS transistor, the trigger voltage and the human body mode (HBM) test immunity are both greatly improved. Also, this cell is latch-up resistant, both the holding voltage and the turn-on current are adjustable and greatly raised than those of a conventional SCR device.**

Keywords- ESD, latch-up, device reliability

I. INTRODUCTION

An excellent electrostatic discharge (ESD) protection cell or circuit should have fast reaction with a small dimension, as well as the ultra-low trigger voltage and turn-on resistance to achieve high ESD protection capability. However, an ideal ESD protection structure is also expected to offer high latch-up immunity under the normal operation condition [1-2]. For the general input/output (I/O) pads and power clamp ESD protection, the dynamic floating gate-coupled and the RC transient-detect gate-driven n-channel metal-oxide-semiconductor field-effect transistors (NMOSFETs) have been widely implemented to lower the trigger voltage and improve the non-uniformity turn-on issue for ESD protection of the complementary MOS integrated circuits (CMOS ICs) [3-6]. However, the rather large area consuming is an important concern for the chip size reduction. Therefore, a silicon-controlled rectifier (SCR) device becomes an attractive option for its high current handling capability and small area penalty, but it suffers the issues of high trigger voltage for ESD and poor latch-up immunity for normal operation. As reported, there are two common methods to improve the latch-up immunity for SCR devices. One is to increase the trigger or turn-on current. The other is to elevate the holding voltage [7-13]. In this paper, an embedded SCR protection structure is proposed to resolve the aforementioned issues with low trigger voltage for ESD and high turn-on or holding current for latch-up. Additionally, it only needs a small layout area and is compatible to the MOSFET layout style.

II. EXPERIMENT

The devices are fabricated by a conventional 0.32 μm CMOS process with 7 nm-thick gate oxides. The total width and length of channels are 200 μm and 0.35 μm, respectively. The ESD and latch-up characterization is as follows: The human body mode (HBM) ESD tests were performed by a Key-Tek ESD Wafer Master tester. The transmission line pulsing system (TLP) impulse I-V characteristics, such as the trigger voltage (V_{t1}) and current (It1), holding voltage (V_h) and current (I_h), secondary breakdown fail voltage (V_{t2}) and current (I_{t2}) were measured by a commercial Barth–4002 system. This system applies the square waveform with 100 ns pulse width and 10 ns rise/fall time to a device, while measuring the voltage across and current through it [14]. The failure criterion was defined as the drain leakage current exceeds 1μA under 3.6 V biasing after ESD zapping. For the latch-up evaluation, the Tektronix–370A curve tracer was used to measure the low frequency I-V characteristics and extract the holding voltage (V_h).

III. RESULTS AND DISCUSSION

Generally, the turn-on voltage of a gate-ground NMOSFET (GGNMOS) depends on the junction breakdown voltage between drain and substrate. In addition to the rather high trigger voltage, GGNMOS also suffers the non-uniform turn on issue due to the different parasitic substrate resistance of different positions of device. These issues cause a low ESD level beyond expectation. To solve these problems, a gate coupled and driven NMOS are invented. However, the layout area is still too large. So, a new embedded SCR structure with gate-couple technique (emSCR GCNMOS) is designed to obtain a low turn-on voltage as well as the high ESD immunity as follows: A parasitic p-n-p-n SCR structure is formed by adding an anode structure (P+ in NW) close to the source region of the gate-couple NMOSFET (GCNMOS), which is composed of a diode, a normally turn-on NFET (soft-pull NMOSFET) and a big NFET clamp. Figure 1(a) and (b) show the circuit schematic diagram and the exact layout snapshot of this cell, respectively.

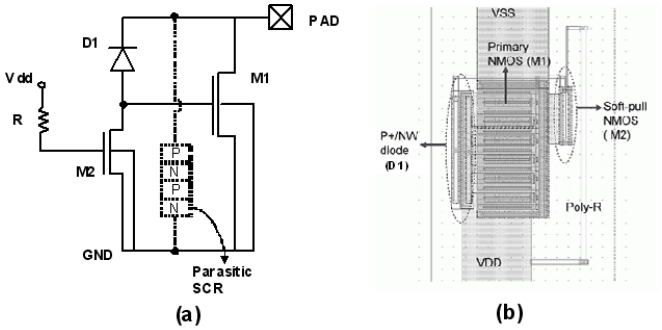

Figure 1 The circuit schematic diagram (a) and exact layout snapshot (b) of the embedded SCR protection cell.

The cross-section view schematic diagram of this test structure is shown in Figure 2. The inserted P+/NW diode is placed at the guard ring region of the primary ESD NFET (M1). During normal operation, the soft-pull NFET (M2) will

turn on and M1 will be turned off to prevent leakage current. When a positive ESD impulse applies to the I/O pad, the P+/NW diode will act as a capacitor and the M2 will act as a resistor. The gate voltage of M1 will be coupled and elevated, then M1 is turned on and conducts some channel current. Once the induced substrate current is large enough to reach the trigger current of the parasitic SCR, the whole cell will turn on with low on-resistance (R_{on}) and high I_{t2}. Importantly, by optimizing the spacing between the inserted P+/N-well anode and the source of M1, the holding voltage and current can be adjusted ($V_h > V_{dd}$) to further enhance the latch-up immunity [15].

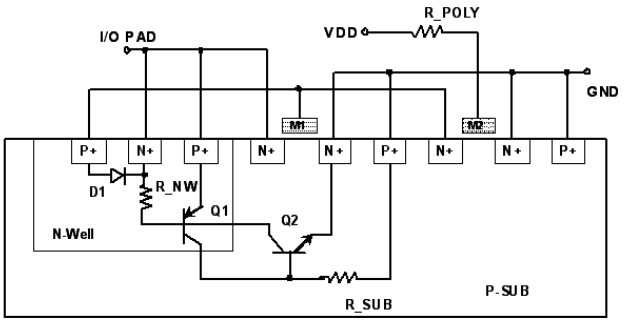

Figure 2 The cross-section view schematic diagram of the embedded SCR protection cell..

Figure 3 shows the TLP test results of the GGNMOS, GCNMOS and the embedded SCR protection cells. There is an obvious improvement on V_{t1} of the GCNMOS as compared with the GGNMOS, but the embedded SCR cell can further improve both V_{t1} and I_{t2}. According to the I-V plot of the embedded SCR cell, the channels of NFET first turn on due to the coupling voltage on the gates. As the drain current keeps on increasing and exceeds 1 A, the induced substrate currents will increase a lot and trigger the parasitic SCR. Once the parasitic SCR turns on, currents go below the channel surface and the current paths increase at the same time. R_{on} is therefore greatly decreased.

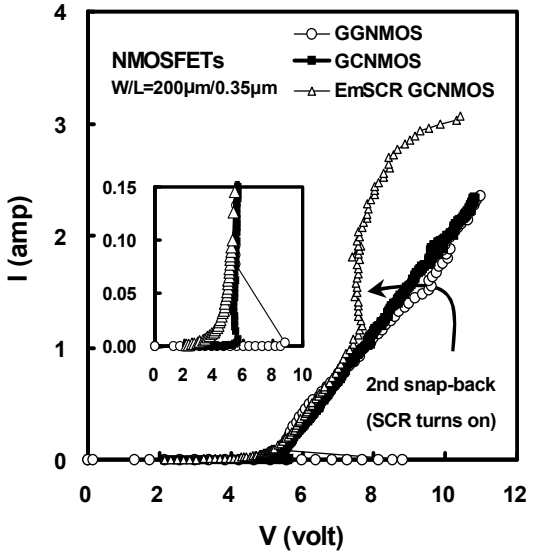

Figure 3 The TLP measurement results of the GGNMOS, GCNMOS and the embedded SCR protection cells.

Table.1 shows the comparisons of the characteristics of TLP I-V plots and HBM test results. Apparently, the breakdown voltages are the same, but the V_{t1}, I_{t2} and HBM levels of the proposed embedded SCR protection cell are all greatly improved in comparison with the conventional GGNMOS and GCNMOS transistors. Both the early trigger and uniform turn-on are achieved. Figure 4 shows the low frequency I-V measurement (by a 60 Hz rectified sine wave) results of the GGNMOS, conventional SCR and embedded SCR cells for the latch-up evaluation. The second snapback resulted by the turn on of parasitic SCR is clearly observed and the trigger current is increased to about 250 mA, which is much higher than that (7 mA) of a conventional SCR device as well as the specifications (100 mA) of JESD 78 latch-up standard. Also, the holding voltage is elevated from 1.3 V to 2.2V. As a result, the latch-up immunity of the embedded SCR cell is greatly improved.

NO		1	2	3
Cell		GGNMOS	GCNMOS	emSCR GCNMOS
BV (volt)		8	8	8
HBM reverse (kV)	Avg.	4.3	4.85	6.5
	Min.	**4**	**4.75**	**6.5**
I_{t1} (Amp)		5.08E-03	6.50E-03	1.16E-02
V_{t1} (volt)		**9.02**	**5.6**	**3.8**
I_h (Amp)		9.20E-02	3.27E-02	
V_h (volt)		5.72	5.31	
I_{t2} (Amp)		**2.32**	**2.34**	**3.03**
V_{t2} (volt)		10.2	10.82	10.3
HBM forward (kV)	Avg.	-8	-8	-8
	Min.	-8	-8	-8

Table.1 The comparisons of the characteristics of TLP I-V and HBM test results.

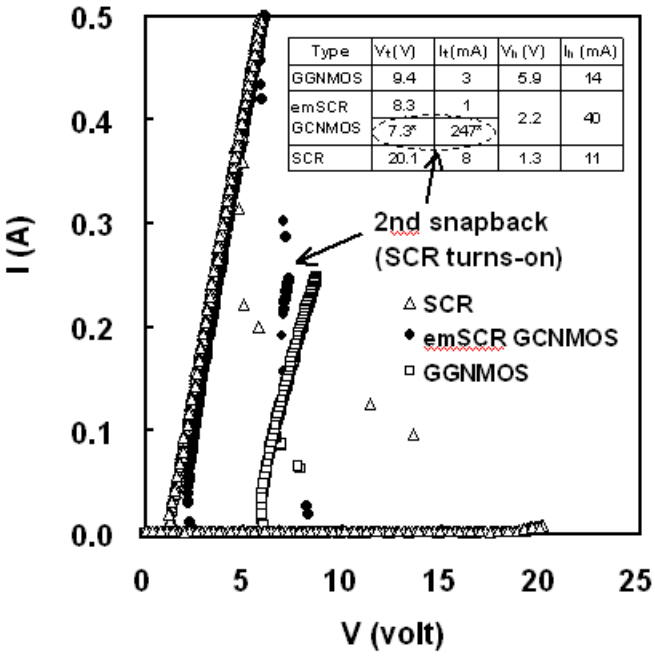

Figure 4 The low frequency I-V measurement results of the GGNMOS, conventional SCR and the embedded SCR protection cells.

Figure 5 shows the emission microscopy (EMMI) experimental results of different turn-on stages of the protection cell by using the Tektronix–370A low-frequency curve tracer tester. Stage A stands for the "OFF" state. Stage B and E stand for the onset of turning on of the NFET channel and the parasitic SCR, respectively. Please note that the trigger voltage at stage B is slightly larger than the V_{t1} of TLP measurement due to the higher rise time and smaller displacement current that can help to trigger the NFET. As indicated, the finger edges of the primary NFET first conduct channel currents due to the local high electric field in the beginning of turn on. Afterward the center fingers turn on and the current distribution extends to the whole fingers. Importantly, it is revealed from stage E to stage F, the intensity of hot spots decreases because of the turn on of embedded SCR. It implies that a major part of conduction currents migrate from the surface to the deeper paths below NEFT channels. Note that the on resistance begins to increase after the stage F. The root cause should be due to the self-heating effect at contacts and metal interconnection.

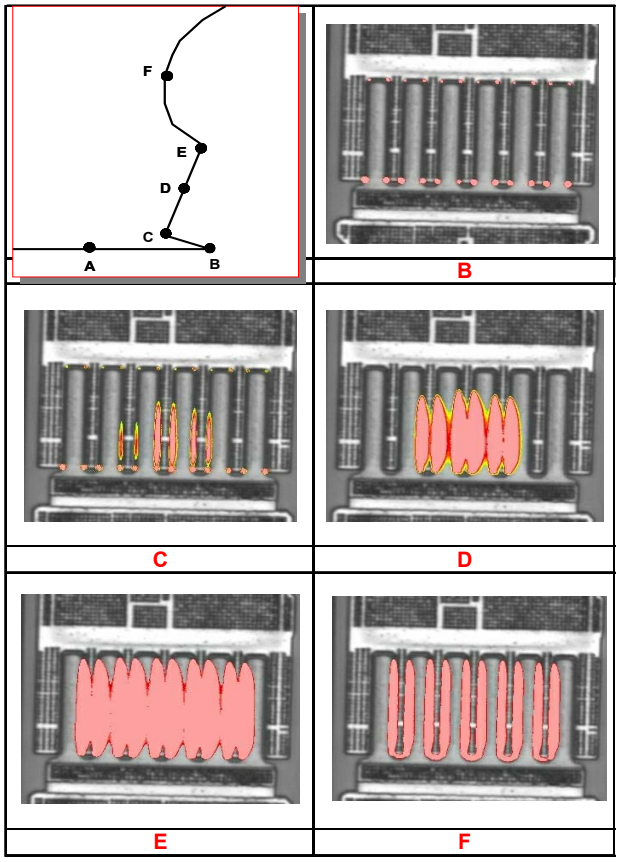

Figure 5 The emission microscopy (EMMI) experimental results of different turn-on stages of the protection cell.

Figure 6 shows the TCAD simulation results of the simplified embedded SCR cell using a TLP-like pulse waveform. The simplified cell removes the normally turn-on NFET, M2, which acts as an equivalent resistor. As the figure shown, there are different turn-on stages, including the beginning of channel conduction, the snapback of parasitic npn bipolar transistor, the triggering and the strongly turning on of the embedded SCR device. At stage F, it is worth noting that the embedded SCR does work and shares the major part of conduction currents from the NFET channel regions. This can explain why it can greatly improve the on resistance and the ESD immunity at the same time.

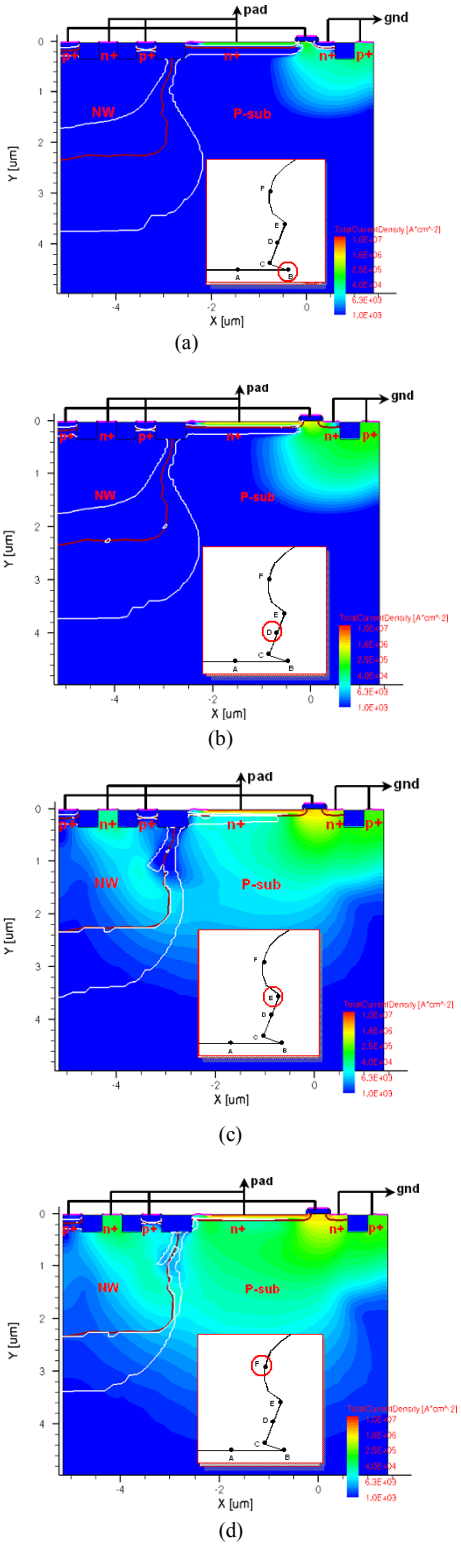

Figure 6 The TCAD simulation results of the protection cell at stage B (a), stage D (b), stage E (c), and the stage F (d).

IV. CONCLUSION

An excellent embedded SCR protection cell with the CMOSFET compatible layout style has been proposed and verified. Two operation regimes are provided, including the first conduction of gate-coupled NMOSFET and the second turn on of parasitic SCR. In comparison with a conventional gate-ground NMOSFET, the trigger voltage is decreased from 9.02 V to 3.8 V and the HBM level is improved from 21.5 V/μm to 32.5 V/μm. Additionally, this cell has a high noise margin to tolerate the overshooting glitch and current injection on the I/O pad. Compared to a conventional SCR device, the trigger current is greatly raised from 7.3 mA to 247 mA and the holding voltage is elevated from 1.3 V to 2.2V. Hence, the high latch-up resistance, early trigger and uniform turn on are all achieved simultaneously.

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