ESD Protection Design with Lateral DMOS Transistor in 40-V BCD Technology

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***Abstract*-ESD protection designs for smart power applications with lateral double-diffused MOS (LDMOS) transistor were proposed. With the proposed ESD detection circuits, the n-channel LDMOS can be quickly turned on to protect the output drivers during ESD stress. The proposed ESD protection circuits have been successfully verified in a 0.35-μm 5-V/40-V bipolar CMOS DMOS (BCD) process. In addition, the power-rail ESD protection design can be also achieved with stacked structure to protect 40-V power pins without latchup issue in the smart power ICs.**

I. Introduction

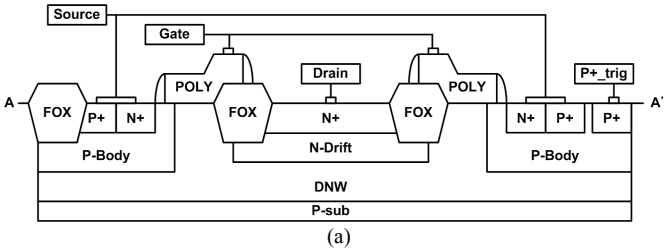
DMOS power transistors have been commonly used as output driver in the smart power technologies [1], [2], including the automotive ICs. Such high-voltage transistor is often self protecting against electrostatic discharge (ESD) stress. The DMOS devices were employed for ESD protection of high-voltage pins by channel current under gate biasing condition [3]. However, the high-voltage device with a large amount of finger numbers did not have high ESD robustness after entering the snapback breakdown region. Such device exhibits random and unconstrained failures during the snapback breakdown before reaching its intrinsic limitation [4]. The medium sized drivers is usually not robust enough to pass the typical industrial ESD specifications of human-body-model (HBM) 2kV and machine-model (MM) 200V. This is attributed to the current crowding effect among the multiple fingers and then inducing inhomogeneous triggering of the parasitic BJT to cause the non-uniform turn-on issue [5], [6]. Therefore, additional ESD protection design is needed to protect such output drivers in the high-voltage technologies [7].

To improve the turn-on speed of MOS transistors for ESD protection, RC-based ESD protection design (with a MOS capacitor) has been widely used in advanced CMOS processes [8]. However, no MOS capacitor is available to sustain high-voltage operation due to the thin gate-oxide structure of the lateral DMOS transistor (e.g. Vd = 40V and Vg = 5V) in such a high-voltage technology studied in this work. Furthermore, the ESD ballast resistor of several hundred Ohms is forbidden to be placed between the output pad and the output driver which was often designed with a specification of small turn-on resistance in applications. In such a case, the additional ESD protection circuit is placed in parallel with the output driver from the pad to ground. If the additional ESD protection circuit was not turned on quickly enough, the output driver would be damaged during ESD stress event. Therefore, it is important to develop an efficient ESD protection circuit which can effectively protect high-voltage output drivers for various applications.

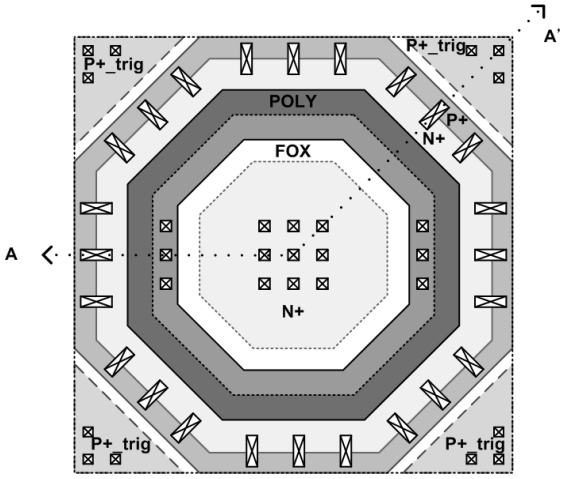
In this work, two efficient ESD protection designs with n-channel lateral DMOS (LDNMOS) are proposed without suffering the gate-oxide reliability under the normal circuit operation. With the gate-driven and substrate-triggered circuit techniques, the turn-on speed of the LDNMOS device can be improved during ESD stress event. Such ESD protection design with gate-driven ESD detection circuit can be further modified to achieve a latchup-free power-rail ESD protection circuit for the high-voltage power pins. The proposed ESD protection circuits have been successfully verified in a 0.35-μm 5-V/40-V BCD process.

II. Structure of LDNMOS as ESD Protection Device

The device cross-sectional view and the layout top view of the n-channel LDMOS (LDNMOS) with a field oxide (FOX) located at the drain region in a 0.35-μm 5V/40V BCD process are shown in Figs. 1(a) and 1(b), respectively. The gate-oxide thickness of such device is only 14nm, limiting the maximum applicable gate voltage to 5V. The N-Drift and the P-Body layers in Fig. 1(a) are lightly doped regions. The device is completely surrounded by the deep n-well (DNW) structure.



(a)



(b)

Fig. 1. (a) Layout top view and (b) the device cross-sectional view of the octagonal unit cell of the n-channel LDMOS with 5-V gate oxide and 40-V drain-to-source operating voltage in a 0.35-μm 5V/40V BCD process.

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The LDNMOS used as the ESD clamp device in the ESD protection circuit is drawn in multiple octagonal cells with side length of the octagon is 10μm (the channel length of each side), and therefore the perimeter of each cell is 80μm. The P+_trig regions at the four corners are drawn as the trigger nodes for implementation of the substrate-triggered technique. In the traditional multiple-fingers structure, the P-Body regions of all fingers are fully separated by FOX, and the individual P-Body regions could worsen the non-uniform turn-on behavior of the LDNMOS device. The ESD robustness is hard to be improved by only increasing the device dimension. On the other hand, the P-Body regions at the source side are connected to each other if the LDNMOS is constructed by multiple octagonal cells with the P+_trig regions located around the LDNMOS. The LDNMOS can be assembled by multiple cells of row number and column number to reach a larger total device width for higher current conducting capability. In this work, the LDNMOS is built up by 2×2 octagonal cells, and the equivalent total device width is 320μm. Such octagonal structure can be applied for gate-biased technique or substrate-triggered technique (which is widely used in CMOS process [9]) by connecting the gate node or the P+_trig node to the bias/trigger circuits.

III. ESD Protection Circuits with LDNMOS

The proposed ESD protection designs with gate-driven ESD detection circuit (gate-biased effect) and substrate-triggered ESD detection circuit are shown in Figs. 2(a) and 2(b), respectively, which are named as the gate-driven ESD protection circuit and the substrate-triggered ESD protection circuit in this work. The ESD clamp device (M_{ESD}) is implemented by LDNMOS with 2×2 octagonal cells.

In Fig. 2(a), the gate-driven ESD detection circuit is composed of a 40-V HV diode (HVDIO), a 7-V zener diode (ZDIO), a 10-kΩ resistor (R), and a 5-V NMOS device (M1). The reverse-biased HV diode and zener diode are connected in series to sustain the high-voltage (40V) applications on the output pad (O/P) during the normal circuit operating condition. The margin of 7V from the total breakdown voltage of the diodes to the operating voltage is used to avoid mis-triggering on the LDNMOS, even if a 10% overshooting voltage happens to the pad. Therefore, the gate-driven ESD protection circuit can be ensured against gate-oxide overstress issue under the normal circuit operating condition. The gate of M1 is connected to the low-voltage power supply (VDDA). The turned-on NMOS (M1) keeps the gate of the LDNMOS at VSS, so the ESD clamp device (M_{ESD}) is guaranteed to be kept off during the normal operating condition. When a positive fast-transient ESD voltage is applied to the output pad with VSS grounded and VDDA floating, the HV diode and the zener diode will enter the breakdown mode to conduct some of ESD current across the resistor R to generate bias voltage to the gate of M_{ESD}. Therefore, the gate voltage of M_{ESD} can be quickly pulled up to turn itself on by the gate-biased technique during ESD stress. After that, the ESD clamp device enters the snapback region to discharge ESD current from the output pad to VSS. The VDDA is initially floating with an initial voltage level of ~0V during ESD stress event, so M1 is kept in off state without influence on the operation of ESD clamp device.

In Fig. 2(b), the substrate-triggered ESD protection circuit includes not only the HVDIO, ZDIO, R, and M1 (which are used in gate-driven ESD detection circuit), but also an additional LDNMOS (M_N) as driving element and a 5-V NMOS device (M2). The gates of M1 and M2 are connected to VDDA to keep the voltage levels at the gate of M_N and the P+_trig node of the ESD clamp device (M_{ESD}) at VSS. During the ESD transient event, the driving element M_N is turned on by the gate-biased effect from the diodes in breakdown mode, and then generates some channel current through M_N into the P+_trig node of the ESD clamp device (M_{ESD}). The substrate-triggered effect can be accomplished to accelerate the turn-on speed of the ESD clamp device.

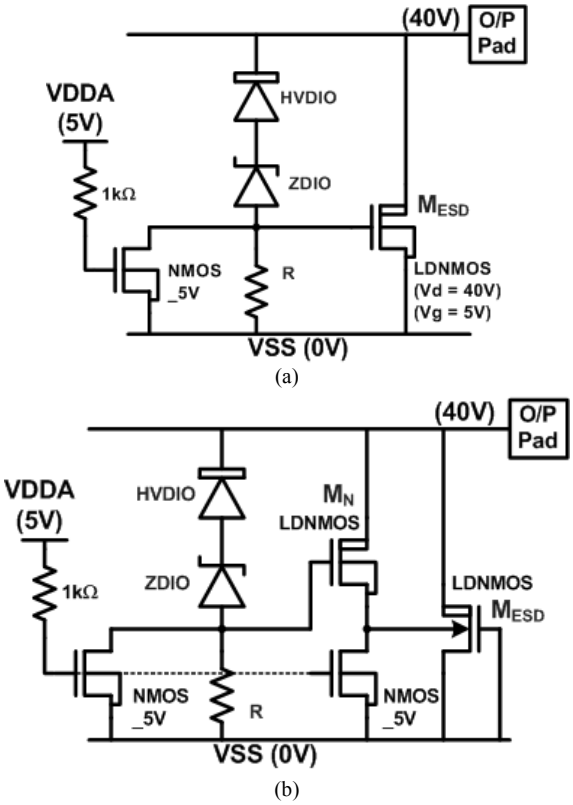

Fig. 2. The proposed ESD protection circuits with (a) gate-driven and (b) substrate-triggered ESD detection circuits.

IV. Experimental Results

The proposed ESD protection circuits have been fabricated in a 0.35-μm 5-V/40-V BCD process. The typical gate-coupled LDNMOS by connecting a resistor from its gate to VSS has been also fabricated in the same wafer for comparison with the proposed gate-driven and substrate-triggered ESD protection circuits. The gate-coupled LDNMOS is drawn by multiple finger structure with each finger width of 75μm, and the total device width is 300μm. On the other hand, the ESD clamp device in the proposed ESD protection circuits are drawn by 2×2 octagonal cells with equivalent total device width of 320μm. To investigate the device behavior during

ESD stress, the transmission line pulsing (TLP) technique has been used to measure the trigger voltage (Vt1) and the secondary breakdown current (It2) of ESD devices. The TLP generator (TLPG) with a pulse width of 100 ns and a rise time of 10 ns is used in this work to find the Vt1 and It2 of the LDNMOS with gate-biased or substrate-triggered technique. The HBM ESD levels and MM ESD levels of the ESD protection circuits are measured by KeyTek ZapMaster and the failure criterion is defined as the I-V characteristic curve shifting over 30% from its original curve after three continuous ESD zaps at every ESD test level.

A. ESD Performance of LDNMOS with Gate-Coupled Design

The TLP-measured I-V characteristics of the gate-coupled LDNMOS with the resistor of 10kΩ and 50kΩ are shown in Fig. 10. The trigger voltage of the gate-coupled LDNMOS with device width of 300μm is still ~60V which is the same as the Vt1 of the standalone gate-grounded LDNMOS with the same device width. Moreover, there is no obvious difference between these two conditions with resistors of 10kΩ and 50kΩ, because the parasitic capacitance from gate to drain of the LDNMOS device is too small to couple sufficient transient voltage to the gate for triggering on the LDNMOS device.

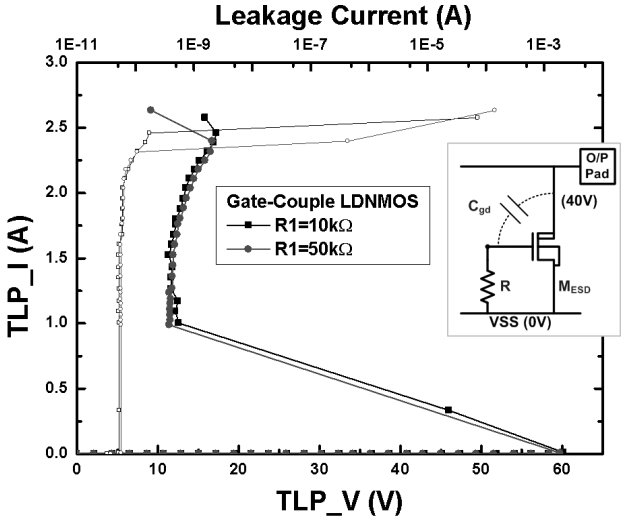

Fig. 3. The TLP-measured I-V characteristics of the gate-coupled LDNMOS (drawn by multiple-finger structure with width of 300μm) with resistors of 10kΩ and 50kΩ connected from gate to source.

B. ESD Performance of LDNMOS with Gate-Driven and Substrate-Triggered ESD Detection Circuits

The TLP-measured I-V characteristics of the gate-driven ESD protection circuit and the substrate-triggered ESD protection circuit are shown in Fig. 4(a), where the I-V characteristic of the gate-coupled LDNMOS with resistor of 10kΩ is also plotted into the figure for comparison. The room-in view on the trigger point of each ESD protection circuit is shown in Fig. 4(b). The LDNMOS starts to be turned on by the gate-driven or substrate-triggered ESD detection circuit when the applied voltage is higher than 47V. The Vt1 of the LDNMOS with the gate-driven ESD detection circuit and substrate-triggered ESD detection circuit can be reduced to ~55V and ~51V, respectively. From the TLP measured I-V curves, both gate-driven and substrate-triggered ESD detection circuits are effective in triggering on the LDNMOS device, where the substrate-triggered ESD detection circuit gains more benefit to reduce the Vt1. However, it needs an additional device M_N as the driving element which will occupy some layout area. The failure criterion for the It2 measurement is determined by leakage current increasing 30% compared to that of fresh samples in this work. Therefore, the It2 level of the gate-coupled LDNMOS is determined as 2.1A. However, the It2 of the LDNMOS drawn by 2×2 octagonal cells with the gate-driven and substrate-triggered ESD detection circuits can be improved up to 2.6A and 2.7A, respectively.

The HBM and MM ESD levels of the gate-coupled LDNMOS, the gate-driven ESD protection circuit, and the substrate-triggered ESD protection circuit are listed in Table I. The gate-coupled LDNMOS has ESD levels of 3kV in HBM and 200V in MM ESD tests. With the gate-driven or substrate-triggered ESD detection circuit, the HBM and MM ESD levels of LDNMOS can be improved to higher than 4kV and 275V, respectively. If a higher ESD level is desired, the number of the octagonal cells in LDNMOS should be increased to sustain the ESD stress.

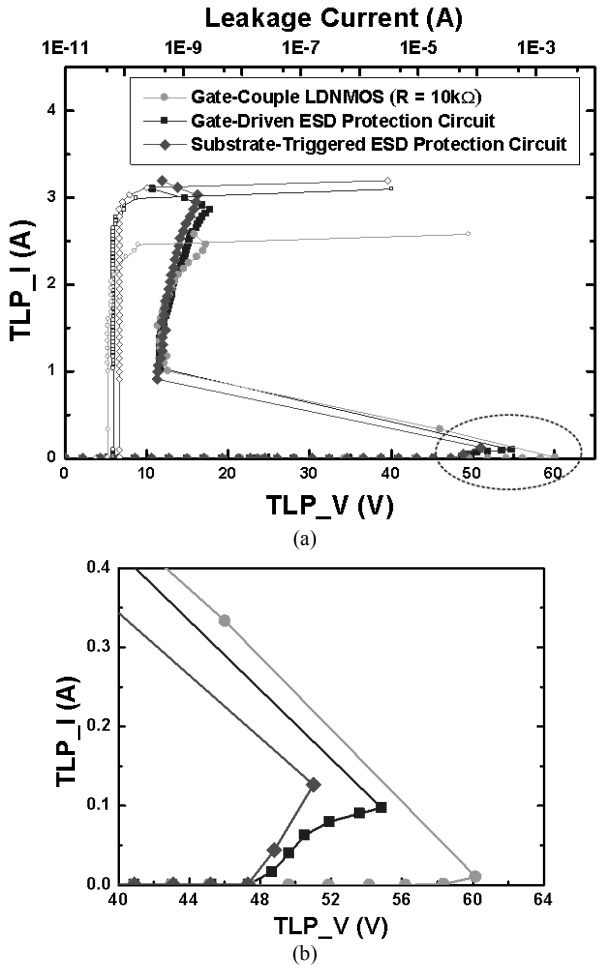

Fig. 4. (a) The TLP-measured I-V characteristics of the gate-coupled LDNMOS (drawn by multiple-finger structure with width of 300μm) with resistors of 10kΩ and 50kΩ connected from gate to source. (b) The room-in view on the trigger point of each ESD protection circuit.

Table I
COMPARISON OF ESD ROBUSTNESS AMONG THE GATE-COUPLED LDNMOS, GATE-DRIVEN ESD PROTECTION CIRCUIT, AND SUB-STRATE-TRIGGERED ESD PROTECTION CIRCUIT

	Layout Type of M_{ESD}	Width of M_{ESD}	HBM ESD Level	MM ESD Level	It2 (TLP)
Gate-Coupled LDNMOS	Multiple-Finger	300μm	3kV	200V	2.1A
Gate-Driven ESD Protection Circuit	Octagonal Cells	320μm	4.4kV	275V	2.6A
Substrate-Triggered ESD Protection Circuit	Octagonal Cells	320μm	4.2kV	275V	2.7A

V. Latchup-Free ESD Protection Design

From the TLP-measured I-V characteristic in Fig. 4(a), the snapback holding voltage of LDNMOS with the gate-driven or substrate-triggered ESD detection circuit is ~12V, which is smaller than the HV power supply voltage (VDD_HV) of 40V. Such an ESD element used in the power-rail ESD protection circuit may be mis-triggered on by the system-level ESD transient pulse to cause latchup failure [10], [11]. To overcome the latchup issue between the power rails, the stacked-LDNMOS structure is used to increase the total holding voltage. With the gate-driven ESD detection circuit, the trigger voltage of the stacked LDNMOS structure can be still kept the same as that of the design in Fig. 2(a). The circuit diagram of the stacked-LDNMOS structure (four LDNMOS devices in series, where each LDNMOS is drawn by multiple finger structure with width of 300μm) with the gate-driven ESD detection circuit is shown in Fig. 5. The corresponding TLP-measured I-V characteristic is shown in Fig. 6. During ESD stress, the stacked LDNMOS can be triggered into snapback region to discharge ESD current. With a total holding voltage of ~50V, the latchup issue can be successfully overcome for 40-V applications. Therefore, the latchup-free power-rail ESD protection circuit can be safely applied in IC products with high-voltage power supply voltage of 40V. The It2 level is still kept at ~2.5A, so the ESD performance of the stacked-LDNMOS structure with gate-driven ESD detection circuit can be kept as good as that of a single LDNMOS device. The stacked-LDNMOS can be also implemented with the layout of octagonal cells in the power-rail ESD protection circuit.

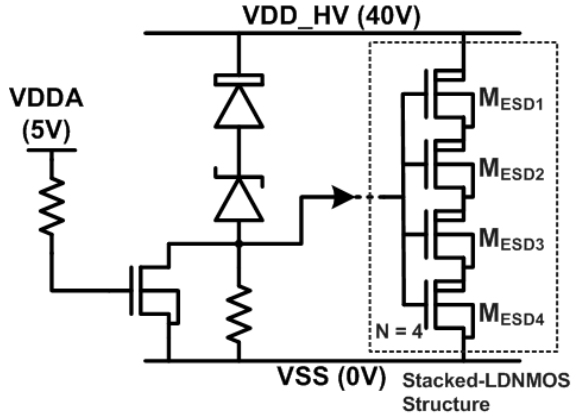

Fig. 5. The latchup-free ESD protection circuit realized with four stacked-LDNMOS devices and the gate-driven ESD detection circuit for 40-V power pins.

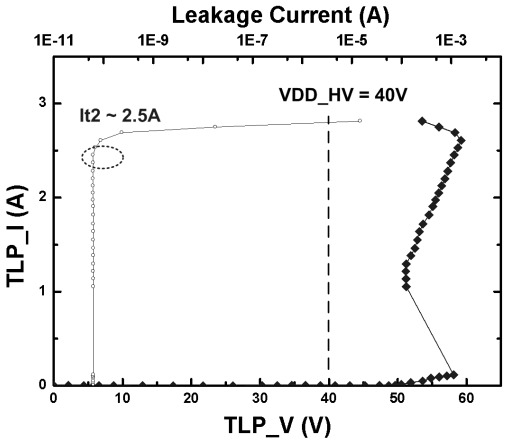

Fig. 6. The TLP-measured I-V characteristics of the latchup-free ESD protection circuit.

VI. Conclusion

Two ESD protection circuits cooperated with LDNMOS for 40-V output pad have been successfully verified in a 0.35-μm 5-V/40-V BCD process. The proposed ESD protection circuits have performed the efficient turn-on uniformity with robust ESD levels, which are excellent design solutions to protect the high-voltage output drivers for smart power applications. By using the stacked-LDNMOS structure with the gate-driven ESD detection circuit, the latchup-free ESD protection circuit can be achieved for protecting the high-voltage power pins.

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