2×VDD-Tolerant Power-Rail ESD Clamp Circuit With Low Standby Leakage in 65-nm CMOS Process

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***Abstract*—With the consideration of low standby leakage in nanoscale CMOS processes, a new 2×VDD-tolerant ESD clamp circuit was presented in this paper. The new ESD clamp circuit had a high-voltage-tolerant ESD detection circuit to improve the turn-on efficiency of the silicon-controlled-rectifier-based (SCR-based) ESD device. This design had been successfully verified in a 65-nm CMOS process. The leakage current of this ESD clamp circuit under normal circuit operating condition was only ~200 nA. Besides, this ESD clamp circuit can achieve 4.8-kV HBM ESD robustness. Therefore, this design was very suitable for mixed-voltage I/O interfaces in nanoscale CMOS processes.**

I. Introduction

In advanced CMOS technologies, the thickness of gate oxide has been scaled down to improve circuit performance with the decreased power supply voltage for low-power applications. However, for the system-on-a-chip (SoC) applications, the I/O buffers with low-voltage devices will drive or receive high-voltage signals to communicate with other ICs in the microelectronic systems or subsystems. Therefore, the I/O buffers must be designed with the consideration of high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of the devices in I/O buffers. To avoid this gate-oxide-reliability issue without using additional thick-gate-oxide devices, the stacked NMOS configuration has been widely used in the mixed-voltage I/O buffers [1], [2]. Without the thick-gate-oxide devices in low-voltage processes, the process steps can be reduced, the fabrication yield can be increased, and the chip cost can be lowered. However, the stacked NMOS configuration usually has a lower electrostatic discharge (ESD) level and slow turn-on speed of the parasitic lateral n-p-n device, as compared with the single NMOS [3], [4]. Therefore, additional ESD protection design must be provided to protect the stacked NMOS in the mixed-voltage I/O buffer without additional leakage current path.

This work was partially supported by National Science Council (NSC), Taiwan, under Contract of NSC 98-2220-E-009-034; by the "Aim for the Top University Plan" of National Chiao-Tung University and Ministry of Education, Taiwan; and by Faraday Technology Corporation, Taiwan.

The ESD protection scheme with ESD bus and high-voltage-tolerant ESD clamp circuit for a SoC with mixed-voltage I/O interfaces has been presented [5], as shown in Fig. 1. This ESD protection scheme is realized with ESD diodes (D_P, D_N, and D_1), ESD bus, 1×VDD ESD clamp circuit, and 2×VDD-torelant ESD clamp circuit. Each ESD stress at the mixed-voltage I/O pad, ESD bus, VDD, or VSS line has the corresponding well-designed ESD discharging path in this scheme. Besides, some ESD protection designs with high-voltage tolerance have also been studied [6]-[8].

In nanoscale CMOS technologies, the leakage current must be considered during the circuit design [9]. With the consideration of low standby leakage, a new 2×VDD-tolerant power-rail ESD clamp circuit by using only thin-oxide devices is proposed in this work. The new proposed ESD clamp circuit has an efficient ESD detection circuit to improve the turn-on efficiency of the silicon-controlled-rectifier-based (SCR-based) ESD clamp device. Such ESD detection circuit with only thin gate-oxide devices can be used to tolerate 2×VDD supply voltage, and the standby leakage current under normal circuit operating condition can be significantly reduced. The proposed design has been successfully verified in a 1-V 65-nm CMOS process.

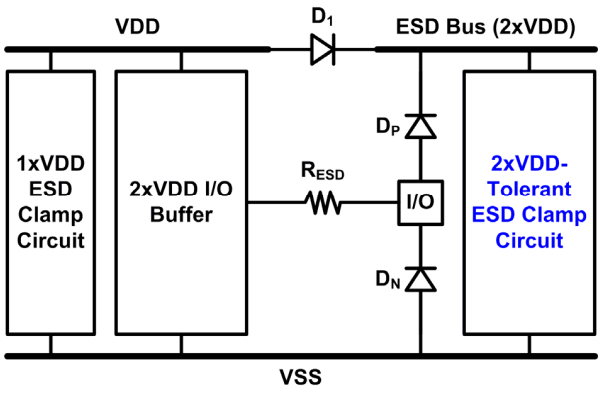


Figure 1. ESD protection scheme with on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer.

II. ESD Clamp Circuit Design

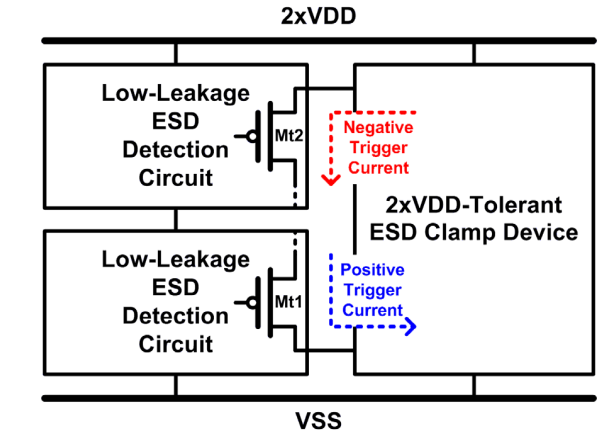
A. Circuit Operations

The proposed 2×VDD-tolerant ESD detection circuit is composed of two low-leakage ESD detection circuits to divide 2×VDD voltage into 1×VDD voltage by their self, as shown in Fig. 2(a). With this symmetry between these low-leakage ESD detection circuits, each low-leakage ESD detection circuit sustains only 1×VDD voltage. Besides, the initial-on PMOS devices (Mt1 and Mt2) [10] existed in each low-leakage ESD detection circuit to effectively trigger the ESD clamp device under ESD stress conditions. Fig. 2(b) shows the implementation of 2×VDD-tolerant ESD clamp circuit. The main ESD current discharging path consists of the double-triggered SCR (DTSCR) with a diode in series (DTSCR+diode), which has high enough holding voltage to prevent from latchup issues. Moreover, the SCR device without poly gate layer has good immunity against the gate-leakage and gate-oxide overstress problems. The SCR device, which is composed of cross-coupled p-n-p and n-p-n BJTs with regenerative feedback loop, and a forward biased diode can sustain high ESD level within a small silicon area in CMOS process. To improve the turn-on speed of SCR device, the trigger currents are absorbed from the base terminal of p-n-p BJT, and injected to the base terminal of n-p-n BJT.

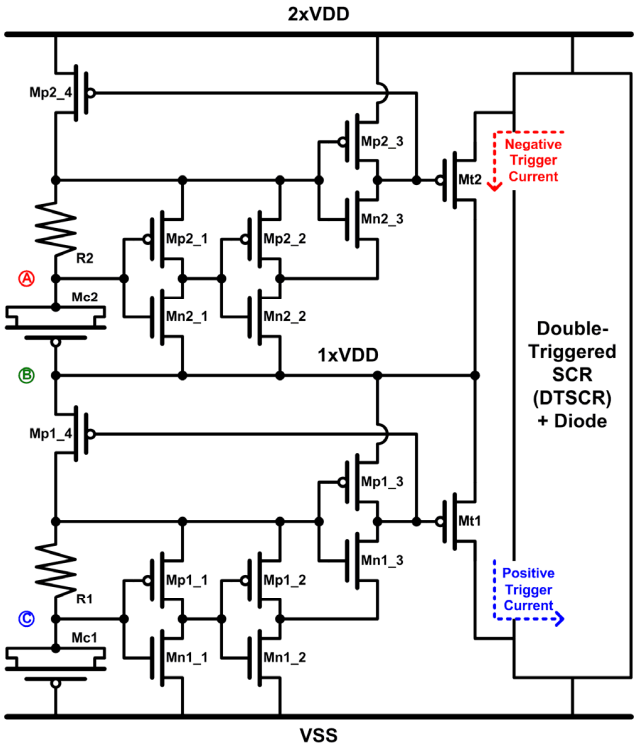
Under the normal power-on condition with 2-V 2×VDD and grounded VSS, node B of the circuit in Fig. 2(b) sustains only 1-V. In other words, all low-voltage devices sustain only 1-V voltage, which prevents from gate-oxide overstress issue. The gate voltage of Mt1 (Mt2) is biased at logic high through the turned-on Mp1_3 (Mp2_3), and the Mt1 (Mt2) can be kept off and no trigger current is generated from the ESD detection circuit to the DTSCR device. Besides, the gate voltage of Mp1_4 (Mp2_4) is also biased at logic high to turn-off Mp1_4 (Mp2_4), so the voltage across the gate oxide of Mc1 (Mc2) and the gate-leakage current through the MOS capacitor under the normal circuit operating condition can be further reduced.

Once the Mt1 (Mt2) in ESD detection circuit is accidentally turned-on under normal circuit operating condition, the node C (node A) can still be charged to logic high to turn-off Mn1_3 (Mn2_3). The gate voltage of Mt1 (Mt2) can be restored to logic high to turn-off Mt1 (Mt2). Therefore, this design can prevent from latchup event.

When a positive fast-transient ESD voltage is applied to 2×VDD line with VSS grounded, the trigger currents will pass through the initial-on PMOS devices (Mt1 and Mt2) to trigger the DTSCR device. The trigger currents will also pump the node B voltage to half of the voltage of 2×VDD line. In the mean time, the gate voltage of Mp1_4 (Mp2_4) is still floating, so the gate voltage of Mn1_3 (Mn2_3) can be charged through Mp1_4 (Mp2_4) to logic high to turn on Mn1_3 (Mn2_3). The RC delay of R1 and Mc1 (R2 and Mc2) keeps the gate voltage of Mp1_1 (Mp2_1) at logic low, and the gate voltage of Mn1_2 (Mn2_2) is at logic high. Therefore, the gate voltage of Mt1 (Mt2) can be kept at logic low through the turned-on Mn1_2 and Mn1_3 (Mn2_2 and Mn2_3) to continuously turn-on the Mt1 (Mt2) and generate the trigger currents. Finally, the DTSCR device can be fully turned-on into holding state to discharge ESD current from 2×VDD line to VSS.



(a)



(b)

Figure 2. (a) Design and (b) implementation of new 2×VDD-tolerant ESD clamp circuit.

B. Simulation Results

Fig. 3 shows the Hspice-simulated results of the proposed ESD clamp circuit under normal circuit operating conditions. The node B voltage is exactly at 1 V, even if the temperature varies from 25°C to 100°C. The node A voltage is only ~1.25 V, and the node C voltage is only ~0.25 V. In other word, the voltage across Mc1 (Mc2) is only ~0.25 V, which is much lower than that in the traditional RC-based ESD detection circuits. Therefore, the gate-leakage currents through the Mc1 and Mc2 can be significantly reduced, and the total leakage currents can be reduced.

Fig. 4 shows the simulated transient responses of the ESD detection circuit. With the voltage disturbance on 2×VDD line, the ESD detection circuit is accidentally turned-on under normal circuit operating condition. However, the MOS capacitors can be restored to logic high to turn off the trigger currents. Therefore, this design can prevent from latchup events.

Under ESD stress conditions, the trigger ability of the proposed ESD detection circuit is also simulated and summarized in Fig. 5. As the ESD-like pulses with 10-ns rise time and various voltages are applied to 2×VDD line to simulate the fast transient voltage of human-body-model (HBM) ESD events, the trigger currents can be successfully generated. The DTSCR device will be triggered-on through the trigger circuit rather than through the junction breakdown.

The ESD clamp devices with and without the proposed ESD detection circuit have been fabricated in a 1-V 65-nm CMOS process. The sizes of ESD clamp devices are selected to be 50 μm. Besides, the trigger PMOS (Mt1 and Mt2) of ESD detection circuit are designed to be 25 μm and 50 μm.

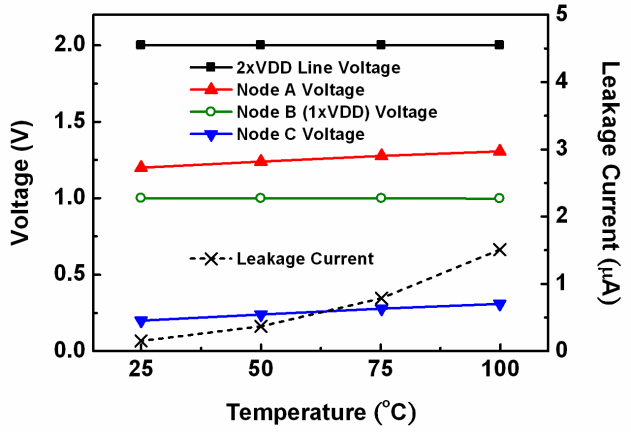


Figure 3. Hspice-simulated results of 2×VDD-tolerant ESD clamp circuit under normal power-on conditions within 25 °C and 100 °C.

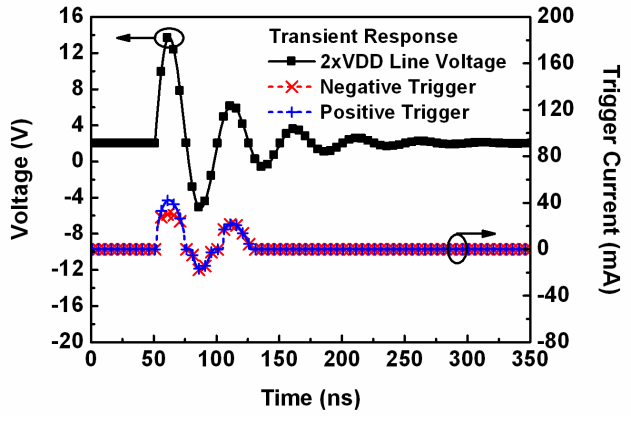


Figure 4. Hspice-simulated transient responses of 2×VDD-tolerant ESD clamp circuit.

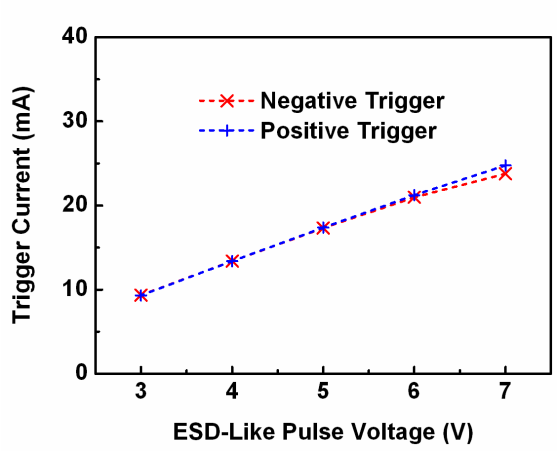


Figure 5. Hspice-simulated results of 2×VDD-tolerant ESD detection circuit under ESD-like pulse zapping.

III. Experimental Results

A. *Transmission Line Pulsing (TLP) Measurement*

The I-V characteristics of the circuits are measured by using TLP generator with 100-ns pulse width and 10-ns rise time. Fig. 6 shows the TLP-measured I-V curves of the fabricated ESD clamp circuits. The trigger voltage (V_{t1}) of the standalone DTSCR+diode ESD device is 11.8 V. With 25-μm and 50-μm trigger PMOS, the trigger voltage of ESD clamp circuits can be reduced to 7.3 V and 6.5 V, respectively. The secondary breakdown current (I_{t2}) of all ESD clamp circuits are ~2.9 A. These data are summarized in Table I.

B. *ESD Robustness*

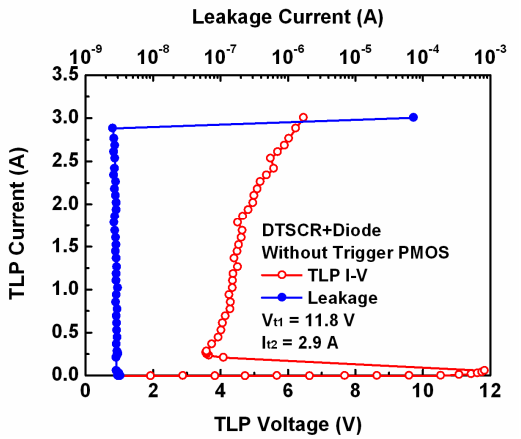
The human-body-model (HBM) ESD robustness of the fabricated ESD clamp circuits are evaluated by the ESD simulator. All ESD clamp circuits can achieve 4.8-kV HBM ESD robustness. These data are also summarized in Table I.

C. *DC Measurement*

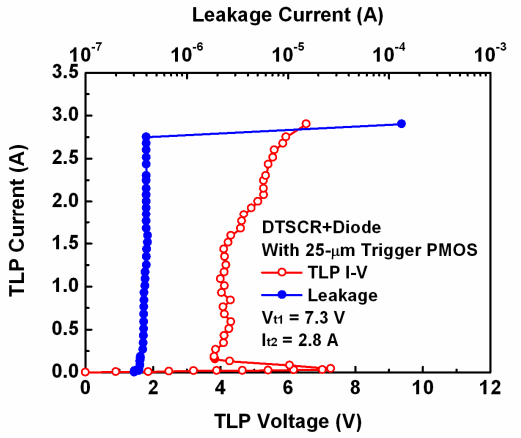
The standby leakage current of the standalone DTSCR+diode ESD device under 2-V bias is only 5 nA at room temperature. Even if the proposed ESD detection circuit is applied to the DTSCR+diode ESD device, the standby leakage current under 2-V bias is ~200 nA at room temperature. Therefore, the new ESD clamp circuit of this work can provide the excellent ESD robustness with low standby leakage current by using only low-voltage devices.

TABLE I. Comparison Among ESD Clamp Circuits

ESD Device	ESD Detection Circuit	TLP V_{t1} (V)	TLP I_{t2} (A)	HBM ESD (kV)	DC I_{Leak} (nA)
DTSCR +Diode	None	11.8	2.9	4.8	5
	With 25-μm Trigger PMOS	7.3	2.8	4.8	170
	With 50-μm Trigger PMOS	6.5	2.9	4.8	293



(a)



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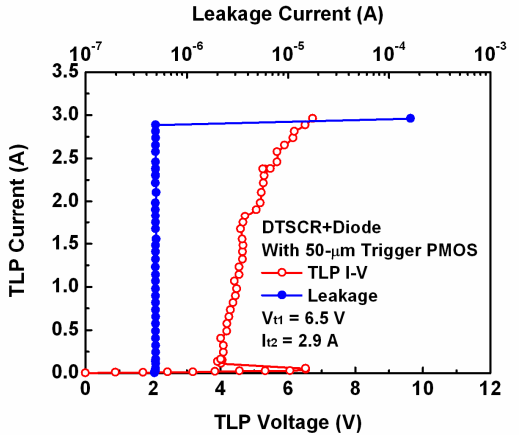

(c)

Figure 6. TLP I-V curves of DTSCR+diode (a) without trigger PMOS, (b) with 25-μm trigger PMOS, and (c) with 50-μm trigger PMOS.

IV. Conclusion

The new 2×VDD-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage current and high ESD robustness for SoC applications with mixed-voltage I/O interfaces has been successfully designed and verified in a 65-nm CMOS process. The 2×VDD-tolerant ESD clamp circuit can operate without gate-oxide reliability issue, and the leakage current is only ~200 nA under normal circuit operating condition. The test patterns can achieve 4.8-kV HBM ESD robustness. In addition, the new ESD detection circuit shows significant help on increasing the turn-on speed of ESD device. With trigger currents generated from the ESD detection circuit, the trigger voltage of the SCR-based ESD device can be reduced, as compared with that of the stand-alone SCR device. Therefore, the new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is the useful circuit solution for on-chip ESD protection design with mixed-voltage I/O interfaces in SoC applications.

References

[1] D. Seo, H. Dabag, Y. Guo, M. Mishra, and G. McAllister, "High-voltage-tolerant analog circuits design in deep-submicrometer CMOS technologies," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 54, no. 10, pp. 2159-2166, Oct. 2007.

[2] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 53, no. 9, pp. 1934-1945, Sep. 2006.

[3] T. Suzuki, M. Kojima, J. Iwahori, T. Morita, N. Isomura, K. Hashimoto, and N. Yokota, "A study of ESD robustness of cascoded NMOS driver," in *Proc. EOS/ESD Symp.*, 2007, pp. 403-407.

[4] T. Tang, S. Chen, S. Liu, M. Lee, C. Liu, M. Wang, and M. Jeng, "ESD protection for the tolerant I/O circuits using PESD implantation," *J. Electrostatics*, vol. 54, no. 3-4, pp. 293-300, Mar. 2002.

[5] M.-D. Ker and W.-J. Chang, "ESD protection design with on-chip ESD bus and high-voltage-tolerant ESD clamp circuit for mixed-voltage I/O buffers," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1409-1416, Jun. 2008.

[6] M.-D. Ker and C.-T. Wang, "Design of high-voltage-tolerant ESD protection circuit in low-voltage CMOS processes," *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 1, pp. 49-58, Mar. 2009.

[7] M.-D. Ker, W.-J. Chang, C.-T. Wang, and W.-Y. Chen, "ESD protection for mixed-voltage I/O in low-voltage thin-oxide CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2006, pp. 546-547.

[8] S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1-5.

[9] Y. Lin, C. Wu, C. Chang, R. Yang, W. Chen, J. Liaw, and C. Diaz, "Leakage scaling in deep submicron CMOS for SoC," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1034-1041, Jun. 2002.

[10] S.-H. Chen and M.-D. Ker, "Implementation of initial-on ESD protection concept with PMOS-triggered SCR devices in deep-submicron CMOS technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1158-1168, May 2007.