ESD Protection Circuit for High-Voltage CMOS ICs with Improved Immunity Against Transient-Induced Latchup

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***Abstract*—With high normal operating voltages, latchup is an important reliability issue for high-voltage (HV) ICs. Harsh operating environments further deteriorate the transient-induced latchup (TLU) immunity of HV ICs. High immunity against TLU has therefore become an important reliability factor of HV ESD protection circuits. In this work, a novel ESD protection circuit with HV silicon controlled rectifier as the main ESD protection element has been proposed. The new proposed ESD protection circuit has been verified in a 0.5-µm 16-V Bipolar CMOS DMOS process. Experimental results showed that the new proposed ESD protection circuit has high TLU immunity of +220V/-295V and high human body model (machine model) ESD robustness of 4.5kV (500V) at the same time.**

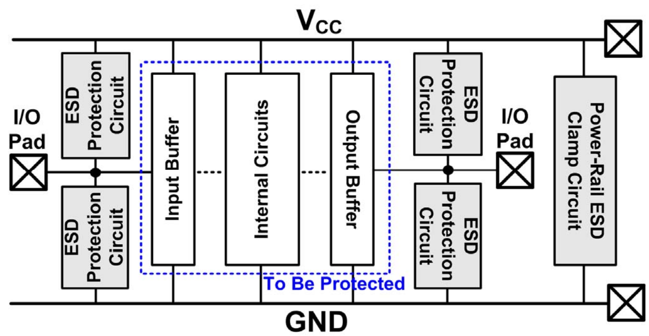

Fig. 1. Whole-chip ESD protection scheme of CMOS ICs.

I. INTRODUCTION

With the increasing demands on automotive electronics, biomedical sensors, liquid-crystal display driver circuits, and light-emitting-diode driver circuits, high-voltage (HV) technologies are playing an important role in nowadays integrated circuits (ICs). With the high power characteristic or sturdy requirement in automotive or biomedical applications, rigorous reliability design is usually required for HV ICs. Unfortunately, HV ICs are usually operated under harsh environments, which increase the difficulty to guarantee high reliability of HV ICs.

Among the reliability issues of HV ICs, electrostatic discharge (ESD) is an inevitable event of ICs during fabrication, packaging, testing, and assembly processes. Because every IC pin can be touched by a human body or a testing machine, ESD protection circuit is required at every input/output (I/O) pad. The ESD protection circuit is also required between V_{CC} and GND supply lines (the power-rail ESD clamp circuit) for whole-chip ESD protection. A typical whole-chip ESD protection scheme of CMOS ICs is shown in Fig. 1. Typically, on-chip ESD protection circuits are required to protect IC products against at least 2-kV human-body model (HBM) and 200-V machine-model (MM) ESD stresses without failure on ICs [1], [2].

In HV ICs, holding voltages (V_h) of ESD protection devices are usually smaller than the specified operating voltages at I/O pads or the normal power supply voltage (V_{CC}). Accordingly, latchup is another serious reliability concern of HV ICs. Even if ICs can pass the quasi-static latchup test [3], it has been reported that external noises coupled into ICs can induce the so-called transient-induced latchup (TLU) [4]. Noisy operating environments of HV ICs further deteriorate the immunity of ESD protection circuits against TLU. For example, system-level ESD events, electromagnetic coupling, or hot plug of ICs, can induce fast transient noises on I/O pins and power supply lines, which can induce TLU of HV ICs. As a result, devising ESD protection circuits with high ESD robustness and high immunity against TLU at the same time is one of the main design targets in HV technologies.

II. SILICON CONTROLLED RECTIFIER IN HIGH VOLTAGE TECHNOLOGIES

With the regenerative feedback of n-p-n and p-n-p bipolar junction transistors (BJTs), silicon controlled rectifier (SCR) is known to have high ESD robustness within small silicon area. As the cross-sectional view shown in Fig. 2, the P–N–P–N structure of traditional HV SCR in a 0.5-µm 16-V Bipolar CMOS DMOS (BCD) process is composed of (P+ anode)–(HVNW)–(PBODY)–(N+ cathode). PSB in Fig. 2 is a p-type implantation, which is a standard process step in this 0.5-µm BCD process.

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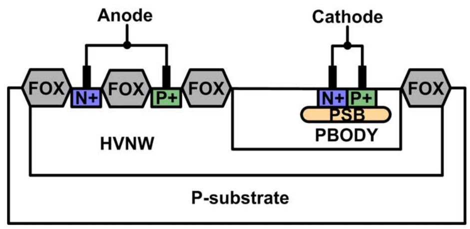


Fig. 2. Device cross-sectional view of a traditional HV SCR device in a 0.5-μm 16-V BCD process.

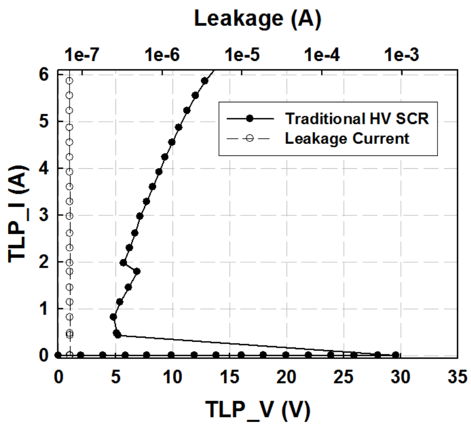


Fig. 3. TLP-measured I-V characteristic of the traditional HV SCR in a 0.5-μm 16-V BCD process.

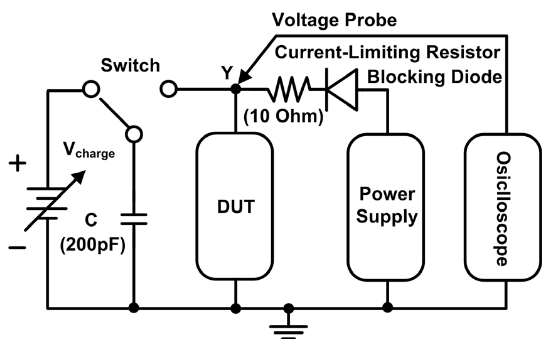


Fig. 4. Measurement setup to evaluate the immunity of device under test against transient-induced latchup.

Though traditional SCR devices can sustain high ESD robustness with small silicon area, it is also known to have low holding voltage. As the TLP measurement results shown in Fig. 3, with the effective width of 100μm, the traditional SCR has TLP-measured secondary breakdown current (I_{t2}) over 6A. However, the traditional HV SCR has low holding voltage of 4.8V. The low holding voltage makes traditional SCR highly susceptible to latchup issue, and has prevented SCR from being a main ESD protection device in HV applications.

III. Transient-Induced Latchup Evaluation

Due to the harsh and noisy operating environments, immunity against TLU is an important design reference to HV ICs. To quantify the TLU immunity of ICs or devices, the TLU measurement setup shown in Fig. 4 has been proposed [5]. In Fig. 4, noise charges Q_{noise} are first stored on the 200-pF capacitor. Q_{noise} equals ($V_{charge} \times C$), where C is the 200-pF capacitor in Fig. 4. By closing the switch, Q_{noise} is injected to the device under test (DUT) biased at the V_{CC} power supply voltage. TLU immunity of the DUT can be decided by the maximum allowable V_{charge} value without inducing latchup of the DUT. The higher V_{charge} level without inducing LU implies that the higher external noise charges are required to mis-trigger the DUT under normal circuit operating conditions.

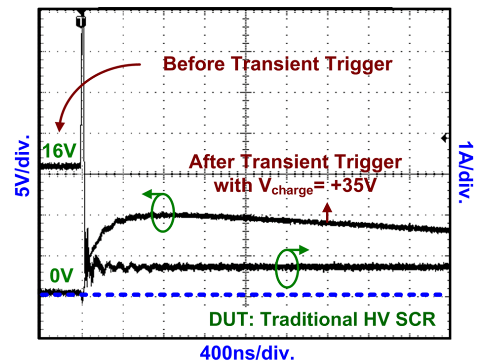


Fig. 5. TLU measurement result of the traditional HV SCR with V_{charge} of +35V.

TLU measurement result of the traditional HV SCR is shown in Fig. 5. With the V_{charge} of +35V, the 16-V power supply voltage was clamped down and a dramatic increase on current was observed after the transient trigger, which shows that latchup was induced by the injected Q_{noise} originally stored on the 200-pF capacitor. The traditional HV SCR was heated up by the latchup induced large current and burned out eventually. With each measurement step of 5V on V_{charge}, traditional HV SCR studied in this work has measured TLU immunity of +30V. Due the poor immunity of traditional HV SCR device against TLU, new techniques are required to improve the TLU immunity of HV SCR devices and to improve the reliability of HV ICs.

IV. New Proposed Silicon Controlled Rectifier With Embedded MOS Transistors

For SCR devices, the holding voltage can be expressed as [6]

$$V_h \cong V_{cep} + V_{ben} \times [1 + \frac{R_{s2}}{(R_{sub} \parallel R_{ext})}] \quad (1)$$

where the V_{cep} is the voltage difference between the collector and emitter of p-n-p BJT inherent in SCR, the V_{ben} is the voltage difference between the base and emitter of n-p-n BJT inherent in SCR. R_{S2} is the parasitic resistance of SCR. Equivalent circuit of SCR devices is shown in Fig. 6. According to (1), introducing an external resistor R_{ext} can effectively increase the holding voltage of SCR, which, in turn, improves the latchup immunity [4]. The smaller the R_{ext} is, the higher the V_h becomes.

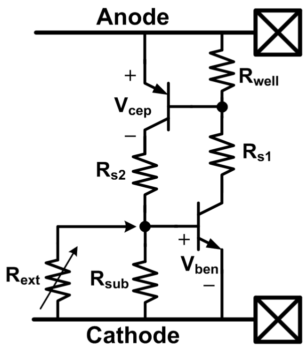


Fig. 6. Equivalent circuit of SCR devices.

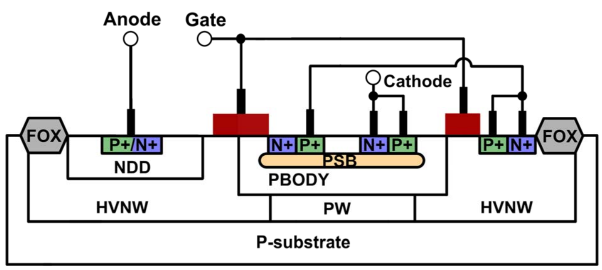


Fig. 7. Device cross-sectional view of the new proposed HVNSCR in this work.

To increase holding voltage of traditional SCR for high immunity against TLU, Fig. 7 shows the new proposed HV SCR structure, the HVNSCR. To fulfill the R_{ext} shown in Fig. 6, a PMOS transistor (M_{P1}) was embedded into the HVNSCR near to its cathode. To reduce the V_{t1} of HVNSCR during ESD stresses, an NMOS transistor was embedded into the HVNSCR near to the anode cathode. Turn-on of the embedded NMOS provides trigger current to lower the V_{t1} of SCR [7]. P+ and N+ anode of the HVNSCR was drawn in interdigitated layout, as the layout diagram of HVNSCR shown in Fig. 8.

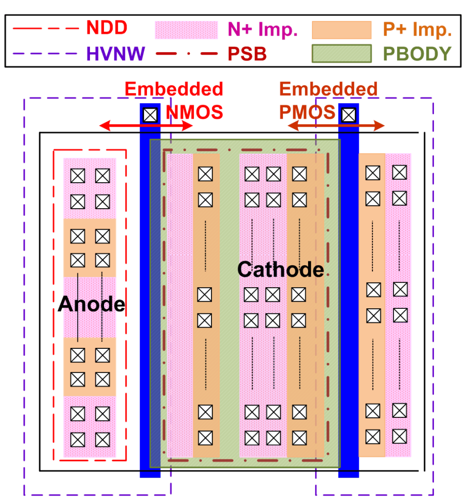


Fig. 8. Layout diagram of the new proposed HVNSCR.

To control gate voltages of embedded MOS transistors in HVNSCR, a CR detection circuit was utilized in the ESD protection circuit as shown in Fig. 9. The new proposed ESD protection circuit has HVNSCR as the main ESD protection element. Capacitance and resistance of CR detection circuit is 2pF and 150kΩ, respectively. During ESD stresses, the CR detection circuit couples high the gate voltage of the embedded NMOS to trigger the HVNSCR. During normal circuit operating conditions, the V_{CC} power on transition has a low voltage rise time (~ms). The gate voltages of the embedded PMOS and NMOS are thereby kept low. Turn-on of embedded PMOS can ensure high holding voltage, *i.e.* high immunity against TLU, during normal circuit operating conditions. By using the embedded PMOS and NMOS transistors, HVNSCR can have a high holding voltage against TLU during normal circuit operating conditions and have reduced trigger voltage to effectively protect internal circuits during ESD stresses.

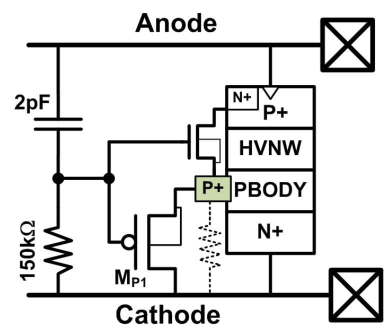


Fig. 9. The new proposed ESD protection circuit in this work, which has a HVNSCR as the main ESD protection element and a CR detection circuit to control gate voltages of embedded MOS transistors in HVNSCR.

V. EXPERIMENTAL RESULTS

The new proposed ESD protection circuit was fabricated together with the traditional SCR in the 0.5-µm 16-V BCD process. HVNSCR in the ESD protection circuit was drawn with 100-µm effective width. TLP-measured I-V characteristic of the new proposed ESD protection circuit is shown in Fig. 10. Though the gate voltage of M_{P1} is coupled high during ESD stresses, M_{P1} can still be partially on and contribute to the R_{ext} to some degree, which increases the TLP-measured holding voltage of HVNSCR to 17.8V. TLP-measured secondary breakdown current (I_{t2}) of the new proposed ESD protection circuit was 3.76A. Compare to the traditional SCR, even though the high holding voltage results in degradation on ESD robustness, the new proposed ESD protection circuit is still area efficient compared to the ESD protection schemes with bipolar or NMOS devices as their main ESD protection elements. Measured HBM and MM ESD robustness of the new proposed ESD protection circuit was 4.5kV and 500V, respectively.

TLU measurement results of the new proposed ESD protection circuit are shown in Figs. 11(a) and 11(b). With the V_{charge} of +220V, closing the switch initially coupled high the gate voltage of M_{P1} through the CR detection circuit. Accordingly, with the embedded PMOS initially in the off

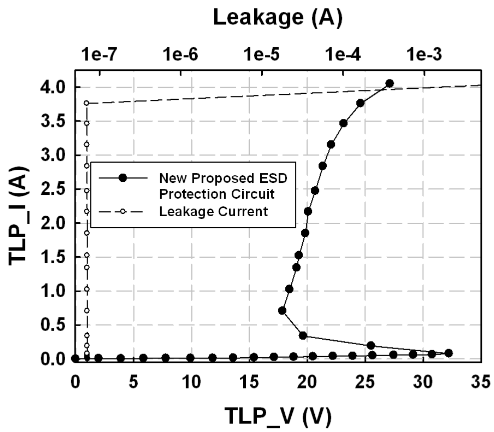
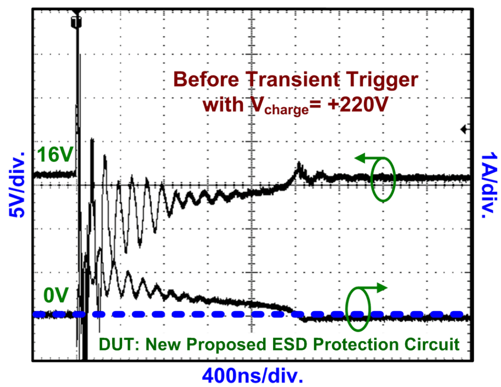
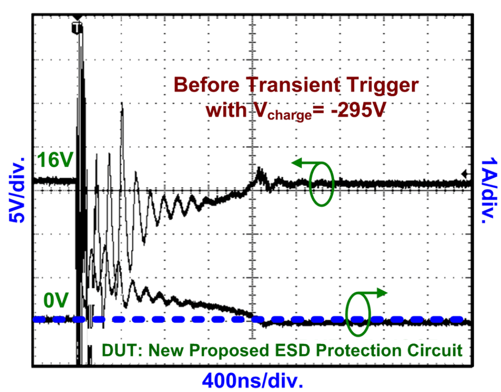


Fig. 10. TLP-measured I-V characteristic of the new proposed ESD protection circuit.



(a)



(b)

Fig. 11. TLU measurement results of the new proposed ESD protection circuit with V_{charge} of (a) +220V, and (b) -295V.

state, a current flowing through the HVNSCR was observed after transient trigger, as shown in Fig. 11(a). However, with the 150-kΩ resistor in the CR detection circuit to discharge the gate voltage of the embedded PMOS, the embedded PMOS was turned on to shut down the HVNSCR. As a result, a gradual decay of the current is observed in Fig. 11(a). After 2µs of the transient trigger, the current drops to zero and the power supply voltage goes back to 16V. The new proposed ESD protection circuit can therefore resist the +220-V TLU test without failure. A similar phenomenon can be observed in Fig. 11(b), where the V_{charge} voltage was -295V. After 1.6µs of the negative transient trigger, current drops to zero and the power supply voltage goes back to 16V, which shows that The new proposed ESD protection circuit can pass the -295-V TLU test without LU failure. For V_{charge} larger than +220V/-295V, TLU tests induced electrical overstress on the new proposed ESD protection circuit and resulted in failure of the ESD protection circuit.

VI. Conclusion

In HV technologies, high ESD robustness and high immunity against TLU are the main design targets for ESD protection circuits. In this work, an ESD protection circuit composed of a new HV SCR structure (HVNSCR) and a CR detection circuit has been proposed. The new proposed ESD protection circuit has been verified in a 0.5-µm 16-V BCD process. Measurement results showed that the new proposed ESD protection circuit has TLU immunity as high as +220V/-295V. Compare to the +30V TLU immunity of traditional HV SCR, a huge improvement has been achieved by using the new proposed ESD protection circuit. With the 100-µm effective width of HVNSCR, the new proposed ESD protection circuit showed satisfactory HBM and MM ESD robustness at the same time, 4.5kV and 500V, respectively. With both the high ESD robustness and the high TLU immunity, the new proposed ESD protection circuit can be safely applied to field applications to provide HV ICs with high reliability within compact layout area.

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