Impact of Layout Pickups to ESD Robustness of MOS Transistors in sub 100-nm CMOS Process

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Abstract — **Electrostatic discharge (ESD) is an inevitable event in CMOS integrated circuits. Layout structure is one of the important factors that affect ESD robustness of MOS transistors. In this work, the impact of inserting additional layout pickups to ESD robustness of both multi-finger NMOS and PMOS transistors has been studied in a 90-nm CMOS process. Measurement results have shown that multi-finger MOS transistors without additional pickup inserted into their source regions can sustain a higher ESD protection level at the same effective device dimension.**

Keywords-electrostatic discharge (ESD), pickup

I. INTRODUCTION

As CMOS technologies keep scaling down, thin oxide thickness of MOS transistors in nano-scale technologies has made integrated circuits (ICs) to be extremely sensitive to electrostatic discharges (ESD). On-chip ESD protection design has therefore become one of the major reliability concerns to CMOS ICs, especially in sub 100-nm technology nodes.

Because ESD is an inevitable event to IC products, input/output (I/O) pins that have NMOS and PMOS transistors have to be provided with enough resistivity against ESD stresses. Moreover, because the average cost of a die in sub 100-nm technologies is expensive, it is important to optimize ESD protection transistors to have a high ESD robustness within limited cell heights and widths.

To discharge the high ESD energy without causing damage to ICs, turn on of parasitic bipolar junction transistors (BJTs) inherent in NMOS or PMOS transistors plays an important role. Moreover, ESD protection transistors are often drawn with multiple fingers to save layout area. Accordingly, layout arrangement substantially affects ESD protection levels of MOS field effect transistors (MOSFETs) [1]. It has been reported in a 130-nm CMOS technology that additional layout pickups degrade ESD protection level of NMOS [2]. This work continues investigating the effect of additional layout pickups to ESD robustness of MOSFETs in sub 100-nm technology nodes. Furthermore, the research scope in this work has been extended to not only the gate-grounded NMOS (GGNMOS) but also the gate-VDD PMOS (GDPMOS), which has been reported to be the bottleneck of high ESD protection level under negative-to-V_{DD} ESD tests at I/O pins [3], [4].

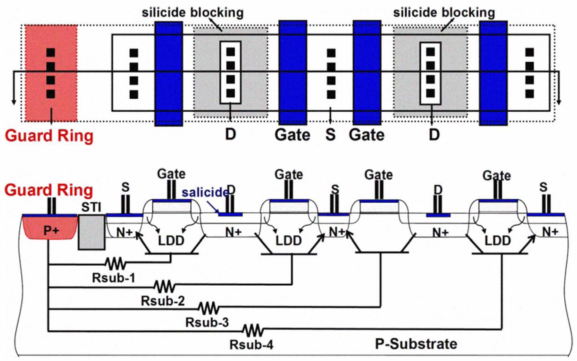

Figure 1. Layout top view and device cross-sectional view of a finger-type NMOS without additional pickup.

II. NMOS WITH DIFFERENT NUMBERS OF PICKUPS

Layout top view and device cross-sectional view of an NMOS with silicide blocking is shown in Fig. 1 [5]. The multi-finger NMOS shown in Fig. 1 does not have an additional pickup but only the P+ guard ring surrounding the whole NMOS device to define the body (substrate) potential. Because the solid ground in the NMOS is the P+ guard ring, parasitic n-p-n BJTs inherent in the NMOS have different substrate resistances (Rsub), as shown in Fig. 1. Asymmetry of Rsub has been reported as an important factor that substantially affects turn-on uniformity of parasitic BJTs [6]. Fig. 2 shows the layout top view and device cross-sectional view of an NMOS with an additional P+ pickup at source of the NMOS. The additional P+ pickup in NMOS is short to source and P+ guard ring of the NMOS. With the additional pickup inserted in source of the NMOS, Rsub between parasitic BJTs can be effectively balanced, as shown in Fig. 2.

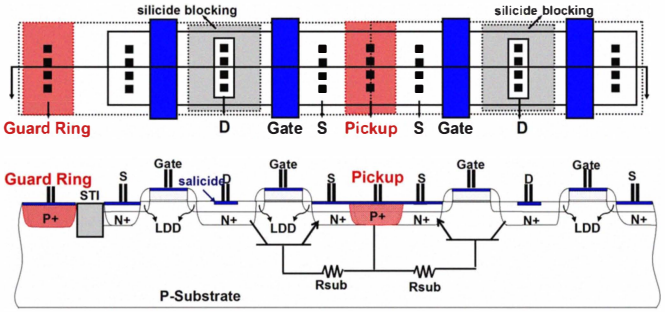

Figure 2. Layout top view and device cross-sectional view of a finger-type NMOS with an additional P+ pickup at source of the NMOS.

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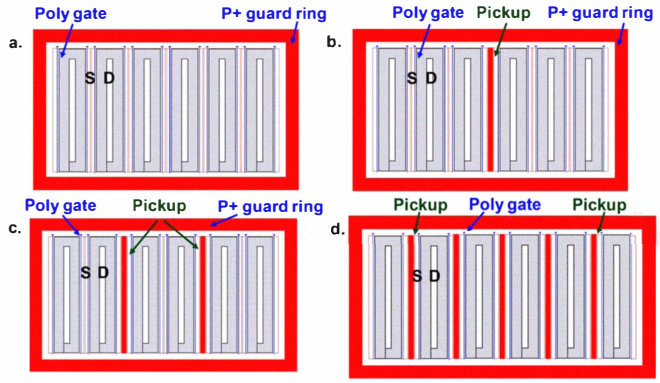
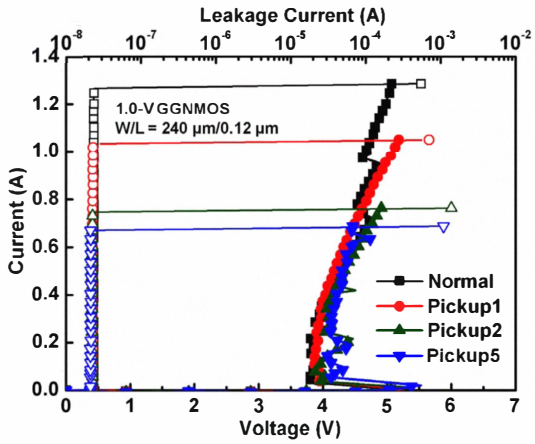
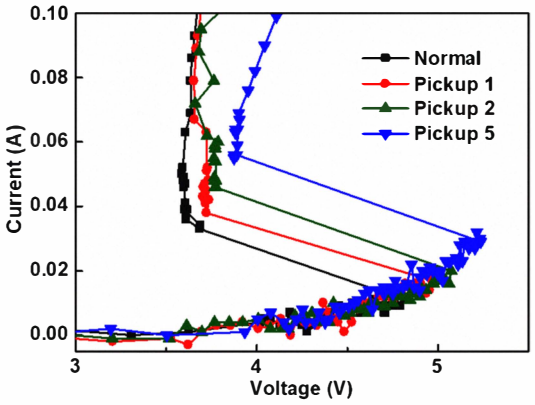


Figure 3. Layout diagrams showing NMOS devices with (a) 0, (b) 1, (c) 2, and (d) 5, P+ pickups inserted in source of NMOS. All tested NMOS devices have the same effective device dimension, 12 fingers with each finger width of 20μm and channel length of 0.12μm.



(a)



(b)

Figure 4. (a) Measured TLP *I-V* curves of 90-nm 1.0-V GGNMOS with different numbers of pickups. (b) Enlarged *I-V* characteristics at low current region, showing the increase in both It1 and Vh when more pickups were inserted into the GGNMOS.

From the viewpoint of Rsub symmetry of parasitic BJTs, inserting additional pickups at source of NMOS can improve turn-on uniformity of NMOS during ESD stresses. However, it is known that low Rsub of parasitic lateral BJTs leads to increase in snapback holding voltage (Vh). As a result, power dissipation during ESD stresses over the NMOS device that has

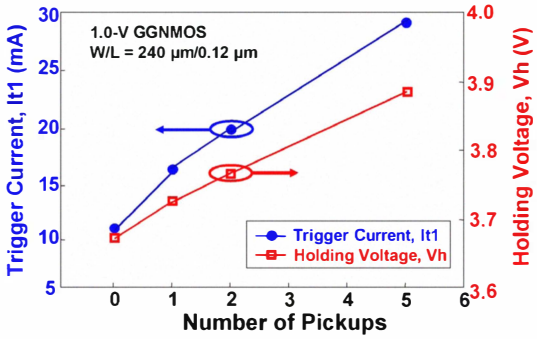


Figure 5. TLP-measured trigger current and holding voltages of GGNMOS with different numbers of pickups.

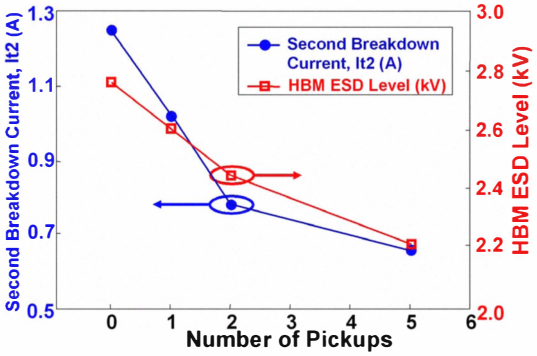


Figure 6. Second breakdown current and HBM ESD protection level of GGNMOS with different numbers of pickups. Measurement results show that inserting additional pickups reduces ESD robustness of 90-nm GGNMOS.

a lower Rsub becomes higher, which can degrade ESD robustness of the NMOS device.

To clarify the effect of additional layout pickups to ESD protection level of NMOS in sub 100-nm technology nodes, different numbers of P+ pickups were inserted into 1.0-V silicide-blocked NMOS devices fabricated in a 90-nm CMOS process. Layout top views of studied NMOS with 0, 1, 2, and 5 additional pickups at source of the NMOS are shown in Figs. 3(a), 3(b), 3(c), and 3(d), respectively. Gate of NMOS devices were internally short to their source, and all tested NMOS devices have the same effective device dimension of 240μm/0.12μm and the same layout style, except for the arrangement of additional pickups.

100-ns transmission line pulsing (TLP) measurement results of the GGNMOS with different numbers of pickups are shown in Fig. 4(a) [7]. The failure criterion of TLP tests is 1-μA leakage current under 1.0-V drain bias. The device without additional pickup is labeled as Normal. From Fig. 4(a), it can be observed that the higher the number of additional pickup is, the lower the measured second breakdown current (It2) becomes. Low current region of Fig. 4(a) is enlarged and shown in Fig. 4(b). Among the measured devices in Fig. 4(b), because the GGNMOS with 5 pickups has the smallest effective Rsub of parasitic BJTs, a higher bipolar trigger current (It1) is required to forward bias the base-emitter (P-substrate/N+ source) junction and to trigger on parasitic BJTs. It can also be observed that the GGNMOS with 5 pickups

shows the highest snapback holding voltage. TLP-measured It1 and Vh of GGNMOS devices with different numbers of pickups are summarized in Fig. 5. TLP-measured second breakdown current and measured human-body model (HBM) ESD protection levels are summarized in Fig. 6. It2 (HBM ESD protection level) of GGNMOS without pickup was degraded from ~1.3A (~2.8kV) to ~0.7A (~2.2kV) when 5 pickups were inserted into the layout structure. From these experimental results, it is clear that inserting additional layout pickups results in degradation on ESD performance of 90-nm ESD protection NMOS.

III. PMOS WITH DIFFERENT NUMBERS OF PICKUPS

Though PMOS in ESD protection schemes are often used to provide a current discharging path from I/O pads to the power supply line through the parasitic body diode [8], PMOS are susceptible to ESD failure under high ESD stress voltages [4]. As the layout top view and device cross-sectional view of a PMOS with an additional N+ pickup shown in Fig. 7, parasitic p-n-p BJTs inherent in PMOS can be triggered on when voltage across the PMOS is high enough, *i.e.* at high ESD stress voltages.

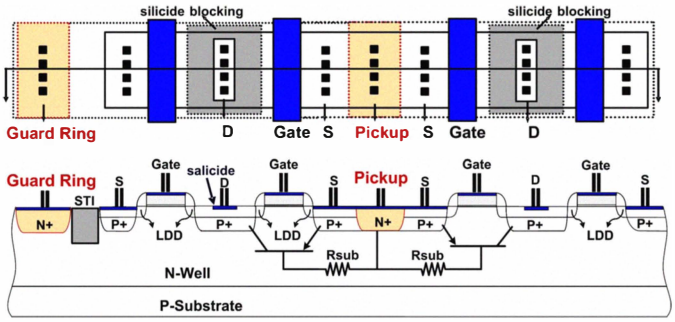


Figure 7. Layout top view and device cross-sectional view of a finger-type PMOS with an additional N+ pickup at source of the PMOS.

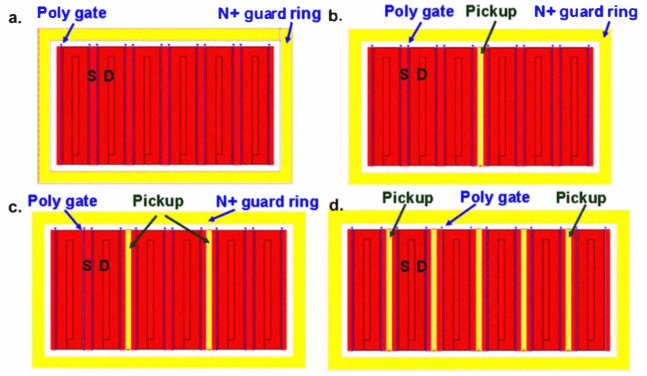
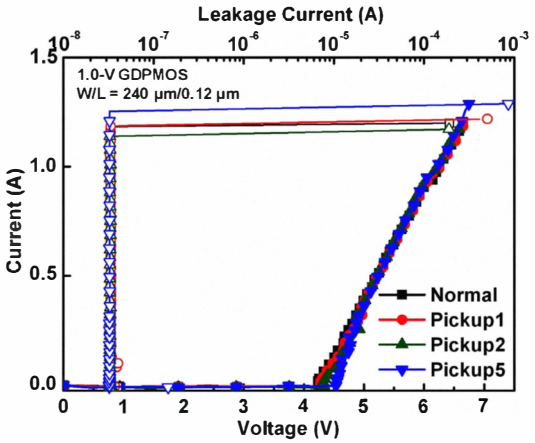
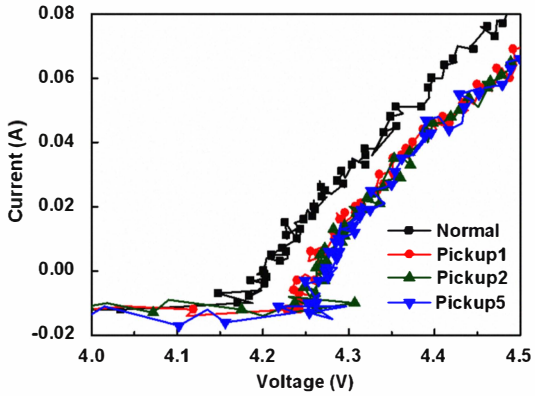


Figure 8. Layout diagrams showing PMOS devices with (a) 0, (b) 1, (c) 2, and (d) 5, N+ pickups inserted in source of PMOS. All tested PMOS devices have the same effective device dimension, 12 fingers with each finger width of 20μm and channel length of 0.12μm.

To study the effect of pickups to the ESD robustness of GDPMOS, different numbers of N+ pickups were inserted to source of 1.0-V silicide-blocked PMOS devices fabricated in



(a)



(b)

Figure 9. (a) Measured TLP *I-V* curves of 90-nm 1.0-V GDPMOS with different numbers of pickups. (b) Enlarged *I-V* characteristics at low current region, showing that inserting pickups in GDPMOS barely affects trigger voltage of GDPMOS.

the 90-nm CMOS process. Figs. 8(a) to 8(d) respectively show layout diagrams of the studied PMOS devices with 0, 1, 2, and 5 pickups. N+ guard ring, N+ pickups, and gate were internally short to source of PMOS.

100-ns TLP measurement results of the GDPMOS with different numbers of pickups are shown in Fig. 9(a). The failure criterion is 1-μA leakage current under 1.0-V source bias. Because of the small bipolar beta gain (β) of parasitic p-n-p BJTs in PMOS, all the measured TLP *I-V* curves in Fig. 9(a) barely show snapback phenomenon [9]. Measurement results in Fig. 9(a) also show that the insertion of N+ pickups to PMOS has little effect on second breakdown current. Low current characteristics of Fig. 9(a) are enlarged and shown in Fig. 9(b). Without the snapback phenomenon, bipolar trigger voltage (Vt1) instead of It1 was used as the benchmark to analyze the effect of pickups to the turn on of parasitic BJTs inherent in PMOS. From Fig. 9(b), Vt1 of PMOS without additional pickup is slightly smaller than those of PMOS with additional pickups. However, the Vt1 difference is trivial, which can come from the fact that body (N-Well) of PMOS has an inherent high sheet resistance, so that a small amount of body current due to avalanche generation during ESD stresses can easily forward bias the collector-base junction. As a result,

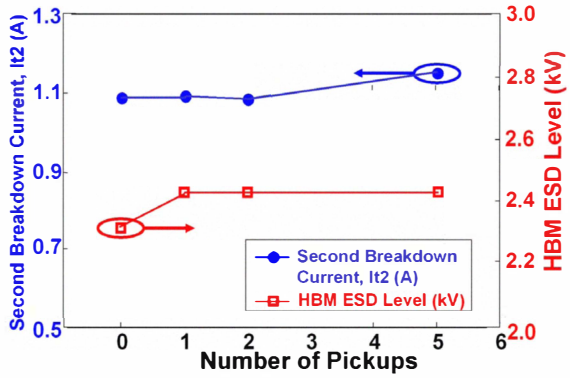


Figure 10. Second breakdown current and HBM ESD protection level of GDPMOS with different numbers of pickups. Measurement results show that inserting additional pickups has little effect on ESD robustness of GDPMOS in sub 100-nm technology.

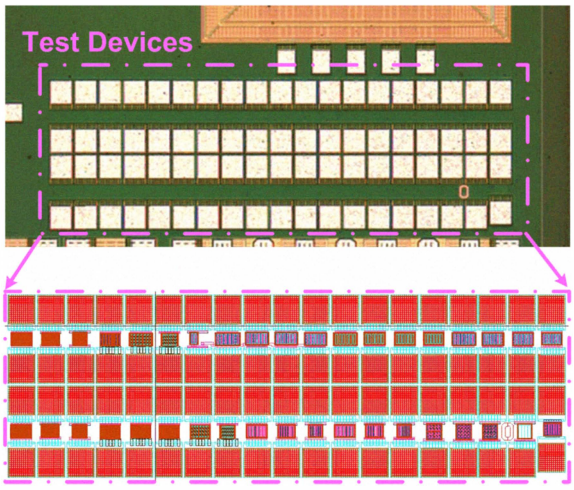


Figure 11. Chip microphotograph and layout of test devices studied in this work.

inserting pickups to PMOS has a trivial effect on turn-on of parasitic p-n-p BJTs. Measurement results in Fig. 9(a) also show that inserting N+ pickups to PMOS has little effect on turn-on resistance of TLP-measured *I-V* curves. Moreover, for lack of snapback during ESD stresses, PMOS does not suffer from the non-uniform turn on effect. As a result, inserting pickups showed trivial impact on It2 of PMOS devices.

Measured second breakdown current and HBM ESD protection levels of PMOS devices with different numbers of pickups are summarized in Fig. 10. It2 (HBM ESD protection level) of GDPMOS without pickup in Fig. 10 is ~1.1A (~2.3kV), and It2 (HBM ESD protection level) of GDPMOS with 5 pickups is ~1.15A (~2.4kV). Layout area of GDPMOS without pickup and that of GDPMOS with 5 pickups are 1127μm^2 and 1300μm^2, respectively. Therefore, from the viewpoint of ESD protection efficiency per layout area, inserting inner pickups is negative to either GGNMOS or GDPMOS in sub 100-nm CMOS technologies. Chip microphotograph and layout of the studied devices in this work are shown in Fig. 11.

IV. Conclusion

Effect of additional layout pickups to the ESD robustness of NMOS and PMOS transistors in sub 100-nm technology nodes has been studied in this work. Test devices were fabricated in a 90-nm 1.0-V CMOS process with silicide blocking. Experimental results show that inserting additional pickups has negative impact to the ESD protection level of NMOS, and barely affects the ESD protection level of PMOS. However, layout area of MOS transistors expands due to the insertion of additional pickups. It is therefore from the ESD protection point of view that additional pickups are not suggested for both NMOS and PMOS transistors in sub 100-nm CMOS technologies.

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