Modeling the Parasitic Capacitance of ESD Protection SCR to Co-Design Matching Network in RF ICs

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***Abstract* — Silicon-controlled rectifier (SCR) has been reported with the good electrostatic discharge (ESD) robustness under the lower parasitic capacitance among ESD devices in CMOS technology. To correctly predict the performances of SCR-based ESD-protected RF circuit, it is essential for RF circuit design with accurate model of SCR device. The small-signal model of SCR in RF frequency band is proposed in this work. The measured parasitic capacitances well agree with the simulated capacitances. With the proposed small-signal model, on-chip ESD protection can be co-designed with RF circuits to eliminate the negative impacts caused by ESD protection SCR on RF performances.**

***Index Terms* — Electrostatic discharges (ESD), low-capacitance (low-C), modeling, radio-frequency (RF), silicon-controlled rectifier (SCR).**

I. Introduction

Nanoscale CMOS technologies are attractive to implement radio-frequency (RF) circuits due to the advantages of high integration capability and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS processes seriously degrades the electrostatic discharge (ESD) robustness of IC products. Against ESD damages, ESD protection devices must be provided at each I/O port of RF circuits [1].

The parasitic capacitance of ESD protection device is an important design consideration for RF circuits [2]. The parasitic capacitance of ESD protection device will disturb the high frequency signals, induce RC delay in the signal path, and cause other serious degradation on the RF circuit performances. Reducing the negative impacts from ESD protection device on RF performance, the solution is to lower the parasitic capacitance and to co-design ESD protection device with RF circuits. Thus, the circuit simulation models of ESD protection devices have strongly requested by IC industry [3].

Silicon-controlled rectifier (SCR) has been reported as the useful ESD protection device in RF circuits due to its less parasitic capacitance. Moreover, SCR with waffle layout structure has also been proposed to reduce the parasitic capacitance [4]. The macro model of SCR has been reported to simulate its turn-on mechanism during ESD stress [5], [6]. However, the small-signal model of SCR in RF circuit operation condition is still scarce. In this work, the small-signal model of SCR in RF frequency band is investigated in a 0.18-μm CMOS process. With such a small-signal model, the parasitic capacitance from ESD protection device can be well co-designed with RF circuits.

II. Design of Ultra Low-Capacitance Waffle SCR

The layout top view of the waffle SCR is shown in Fig. 1(a). The anode of the waffle SCR was electrically connected to the inside N+ diffusion and P+ diffusion, which were formed in the N-well. On the contrary, the cathode of the waffle SCR was electrically connected to the outside N+ diffusion and P+ diffusion, which were formed in the P-well. The dimension of the inside P+ that is labeled as S_A is kept at 29.12 μm. The spacing between the inside P+ and the outside N+ is labeled as S_{AC}, which has the significant effects on the performance of the waffle SCR. The size of the outside N+ and P+ that is labeled as S_C is kept at 14.25 μm. When a normally positive potential is applied between the anode and the cathode, the N-well / P-well junction is reverse-biased, so the waffle SCR is kept off under normal circuit operating conditions. When an ESD stress is zapped to the anode with cathode grounded, the waffle SCR will be highly conductive to quickly discharge ESD current. The discharging path of the waffle SCR from anode to cathode is P+ / N-well / P-well / N+.

The device cross-sectional view and the small-signal model of the waffle SCR is shown in Fig. 1(b). The parasitic capacitance of the inside P+ / N-well junction is labeled as C_A. The resistances from the anode to the fringe of the N-well are labeled as R_A and R_{AS}. The resistances from the fringe of the N-well to the cathode are labeled as R_{CS} and R_C. The parasitic capacitance of the outside P-well / N+ junction is labeled as C_C. The impedance from anode to cathode of the waffle SCR is

$$Z_{SCR} = \frac{1}{2}\left(\frac{R_A}{1+j\omega C_A R_A} + R_{AS} + \frac{1}{j\omega C_S} + R_{CS} + \frac{R_C}{1+j\omega C_C R_C}\right) \quad (1)$$

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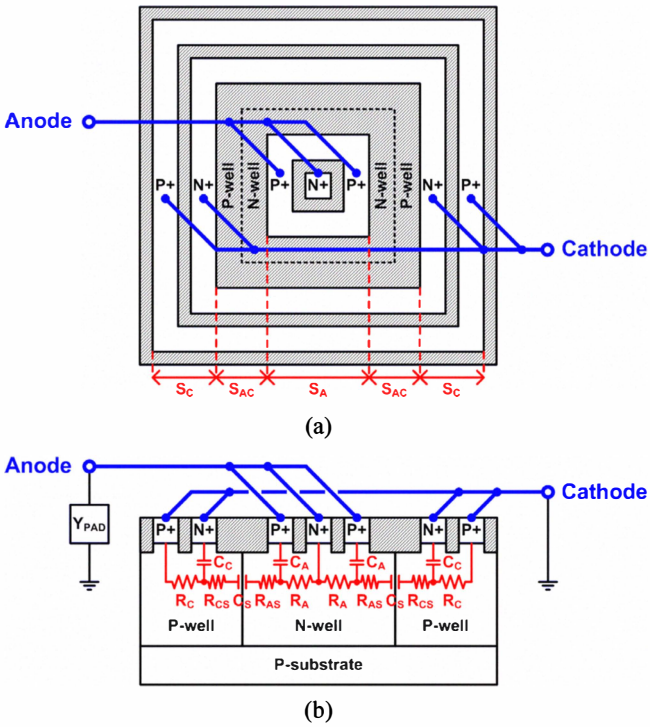
where ω is the angle frequency (2πf, f is the operation frequency). In general, the resistances of R_A, R_{AS}, R_{CS}, and R_C have the same order of 100 Ω, and the capacitances of C_A, C_S, and C_C have the same order of 100 fF. To simplify the calculation, the resistances and the capacitances are replaced by the symbols of R and C. The admittance from anode to cathode of the waffle SCR can be expressed as

$$Y_{SCR} = \frac{8\omega^2C^2R + 4\omega^4C^4R^3}{1+21\omega^2C^2R^2+4\omega^4C^4R^4} + j\omega\left(\frac{2C+6\omega^2C^3R^2}{1+21\omega^2C^2R^2+4\omega^4C^4R^4}\right) \quad (2)$$

The parasitic capacitance of the waffle SCR in high frequency is

$$C_{SCR} = \frac{2C+6\omega^2C^3R^2}{1+21\omega^2C^2R^2+4\omega^4C^4R^4} \approx \frac{3}{2\omega^2CR^2} \quad (3)$$

To further reduce the parasitic capacitance of the waffle SCR, increasing R and the spacing between the anode and the cathode (S_{AC}) is a solution. The dimensions of components used in the waffle SCR model are listed in Table I.



(a)

(b)

Fig. 1. (a) Layout top view and (b) device cross-sectional view and small-signal model of waffle SCR.

III. Experimental Results

A. RF Measurement

The high-frequency characteristics of the waffle SCR were obtained from the measurement of S-parameters by using the vector network analyzer HP 8510C. During the S-parameter measurement, the anode of the waffle SCR was biased at 0.9 V, which is $V_{DD}/2$ in the given 0.18-μm CMOS process. Then the Y_{11}-parameter can be obtained from the measured two-port S-parameters by using

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_0\left((1+S_{11})(1+S_{22})-S_{12}S_{21}\right)} \quad (4)$$

where Z_0 is the termination resistance and equals to 50 Ω.

To facilitate on-wafer measurement, the waffle SCR were arranged with ground-signal-ground (G-S-G) pads. The parasitic effects of the bond pads (Y_{PAD} in Fig. 1(b)) must be removed to extract the intrinsic device characteristics. The test patterns, one was the waffle SCR with G-S-G pads and the other was the stand-alone G-S-G pads, were fabricated in the same experimental test chip. Then the intrinsic device characteristics (Y_{SCR}) can be obtained by subtracting these two measured Y-parameters. Finally, the parasitic capacitance of the waffle SCR can be extracted.

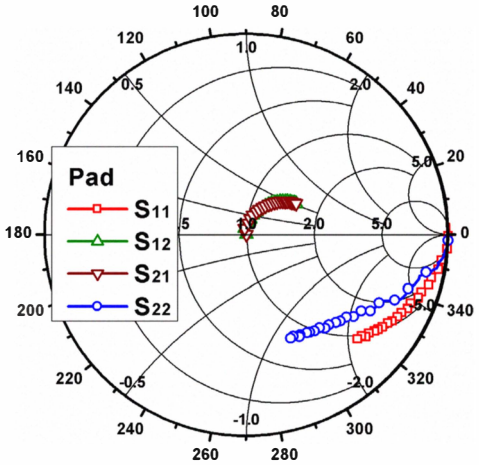
Fig. 2 shows the measured S-parameters within 0~20 GHz of the stand-alone pads, and the waffle SCR with different device spacing. The extracted capacitances and the simulated results within 0~20 GHz of the waffle SCR with shorter and longer spacing are shown in Figs. 3(a) and 3(b), respectively. The measured capacitances agree with the simulated capacitances. Thus, the small-signal model of the waffle SCR is appropriate to model the capacitance of the waffle SCR. The parasitic capacitances of the waffle SCR at 2.4 GHz and 5 GHz are decreased with the increased S_{AC}, which are summarized in Table II.

B. ESD Robustness and Comparison

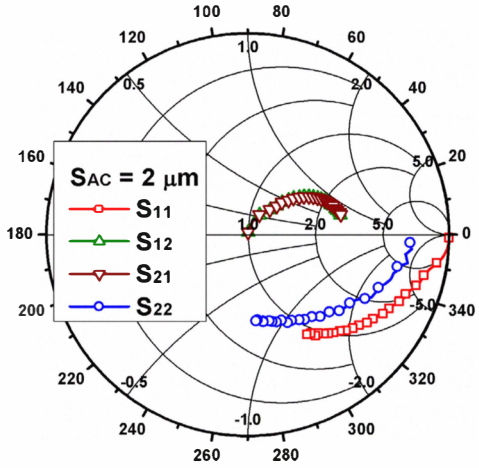
Human-body-model (HBM) and machine-model (MM) ESD robustness of each waffle SCR have been evaluated by the ESD tester. The HBM ESD level of each waffle SCR exceed 8 kV (8-kV is the maximum limitation of ESD tester), and MM ESD level are increased from 1.30 kV to 1.53 kV with the increased S_{AC}.

Fig. 4 shows the ratio of the parasitic capacitance to MM ESD robustness (C_{SCR}/V_{MM}). The parasitic capacitances of the waffle SCR under the ESD robustness has a decrease of about 20 %, as the S_{AC} was increased.

Fig. 5 shows the I-V characteristics of the waffle SCR, which were measured by the transmission-line-pulsing (TLP) system. The turn-on voltage (V_{t1}), secondary breakdown current (I_{t2}), and turn-on resistance (R_{on}) in the holding region of the waffle SCR can be obtained by the I-V curves and listed in Table II. The dependence of C_{SCR}/V_{MM} and the V_{t1} on S_{AC} of the waffle SCR are shown in Fig. 6. Even if the V_{t1} is slightly increased with the increased S_{AC}, it can be reduced by the trigger skill without adding the I/O loading.



(a)



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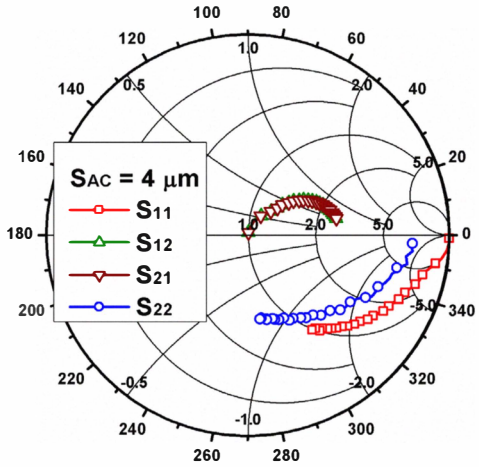
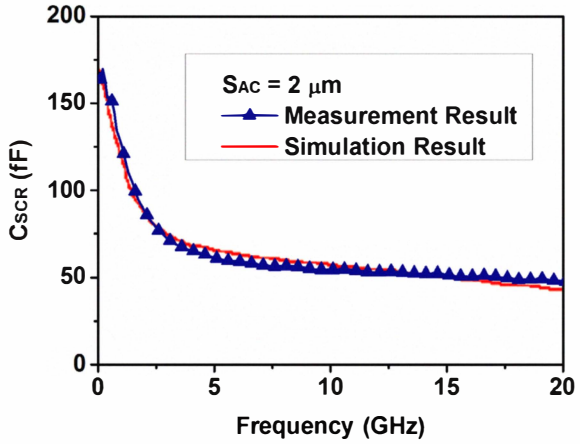
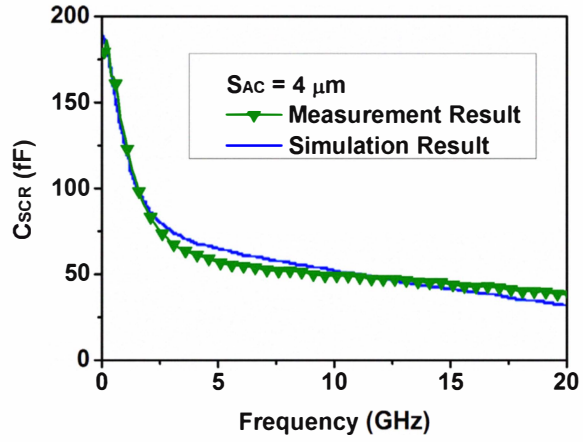


(c)

Fig. 2. Measured S-parameters within 0~20 GHz of (a) stand-alone pads, (b) waffle SCR with shorter spacing, and (c) waffle SCR with longer spacing.



(a)



(b)

Fig. 3. Measured and simulated parasitic capacitance (C_{SCR}) of waffle SCR with (a) shorter spacing and (b) longer spacing.

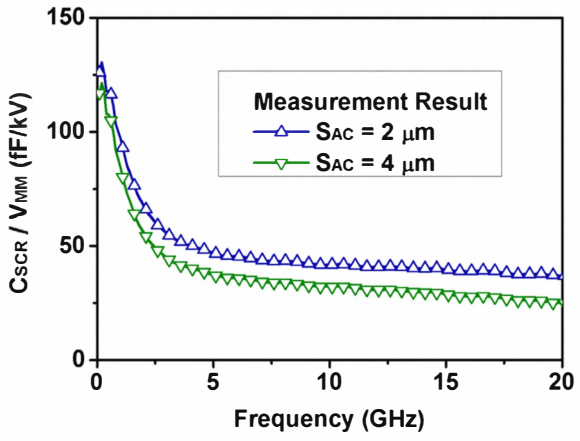


Fig. 4. Ratio of parasitic capacitance to MM ESD robustness (C_{SCR}/V_{MM}) of waffle SCR under different device spacing (S_{AC}).

TABLE I

DIMENSION OF COMPONENTS USED IN WAFFLE SCR MODEL UNDER DIFFERENT DEVICE SPACING

S_{AC}	C_S	C_A	C_C	R_A	R_C	R_{AS}	R_{CS}
2 μm	85 fF	100 fF	150 fF	500 Ω	450 Ω	90 Ω	70 Ω
4 μm	95 fF	100 fF	180 fF	500 Ω	420 Ω	120 Ω	100 Ω

TABLE II

Comparison on Measured Characteristics of Waffle SCR Under Different Device Spacing

S_{AC}	C_{SCR}@ 2.4GHz	C_{SCR}@ 5GHz	V_{HBM}	V_{MM}	V_{t1}	R_{on}	I_{t2}
2 μm	80.23 fF	61.19 fF	> 8 kV	1.30 kV	15.15 V	0.8 Ω	> 6 A
4 μm	77.17 fF	57.22 fF	> 8 kV	1.53 kV	16.16 V	1.0 Ω	> 6 A

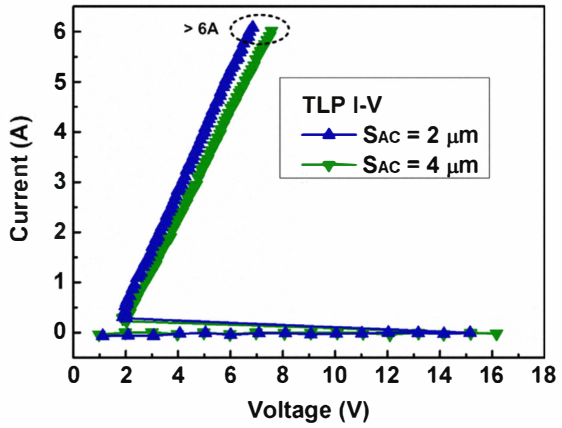


Fig. 5. TLP-measured I-V characteristics of waffle SCR under different device spacing (S_{AC}).

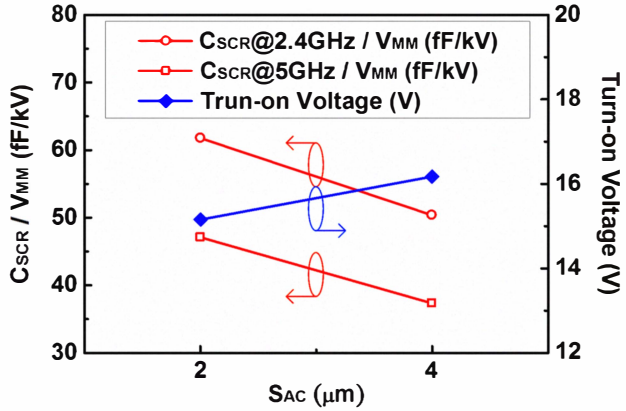


Fig. 6. Dependence of C_{SCR}/V_{MM} and turn-on voltage (V_{t1}) on device spacing (S_{AC}) of waffle SCR.

IV. CONCLUSION

The small-signal circuit model of the waffle-structured SCR has been proposed and proved in silicon. The measured parasitic capacitances well agree with the simulated capacitances. Using the proposed small-signal model, the waffle-structured SCR with a larger anode-to-cathode spacing results in a lower parasitic capacitance in RF frequency band. The waffle-structured SCR with the low enough capacitance is very suitable for ESD protection in RF ICs. Moreover, the RF circuits can be well co-designed with the proposed small-signal model to eliminate the negative impacts from ESD protection SCR on RF performances.

ACKNOWLEDGEMENT

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REFERENCES

[1] S. Voldman, *ESD: RF Technology and Circuits*. John Wiley & Sons, 2006.

[2] M.-D. Ker and C.-M. Lee, "Interference of ESD protection diodes on RF performance in giga-Hz RF circuits," in *Proc. IEEE International Circuits and Systems Symp.*, 2003, pp. 297-300.

[3] C.-Y. Lin, M.-D. Ker, and Y.-W. Hsiao, "Design of differential low-noise amplifier with cross-coupled-SCR ESD protection scheme," *Microelectronics Reliability*, vol. 50, no. 6, pp. 831-838, Jun. 2010.

[4] M.-D. Ker and C.-Y. Lin, "Low-capacitance SCR with waffle layout structure for on-chip ESD protection in RF ICs," *IEEE Trans. Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1286-1294, May 2008.

[5] L. Lou and J. Liou, "An improved compact model of silicon-controlled rectifier (SCR) for electrostatic discharge (ESD) applications," *IEEE Trans. Electron Devices*, vol. 55, no. 12, pp. 3517-3524, Dec. 2008.

[6] J. Sarro and E. Rosenbaum, "A scalable SCR compact model for ESD circuit simulation," in *Proc. IEEE International Reliability Physics Symp.*, 2008, pp. 254-261.