P-40: Design of Analog Pixel Memory Circuit with Low Temperature Polycrystalline Silicon TFTs for Low Power Application

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Abstract

A new analog pixel memory cell realized in a 3-μm LTPS technology is proposed to achieve low-power consumption for TFT-LCDs. By employing the inversion data in storage capacitor with complementary source follower, the frame rate to refresh the static image can be reduced from 60Hz to 3Hz with output decay only less than 0.075V under the input data from 1V to 4V.

1. Introduction

Recently, Thin Film Transistor Liquid Crystal Displays (TFT-LCDs) become a mainstream for displays because of high contrast ratio and fast response time. However, since the TFT-LCDs are not emissive display, high power consumption is a serious problem for TFT-LCDs. Most research reports had mentioned that the power consumption almost comes from the backlight system with AC power supplying to the LCs. In order to reduce the power wastage on AC power for displays [1], the Memory-In-Pixel (MIP) circuit was used to implement a low-power standby mode for continuous display of static images.

Memory-in-pixel circuit has attracted lots of interests for low-power application [2]-[8]. By refreshing the voltage level of scan line, polarity inversion can be easily produced even though the data is no longer furnished. So far, most of literatures used the digital MIP circuits [2]-[5], but the digital MIP requires suitable scan lines and capacitors to reach the action of polarity inversion. On the contrary, integrating analog MIP circuit would achieve high image quality and resolution. But, the analog memory has a shortcoming that the output voltage may have inaccuracy with corresponding data voltage, which means that the static image may be distorted with asymmetry of inversion voltage.

In this work, an analog memory cell with the function of self voltage inversion for MIP application is proposed. The memory cell is realized in conventional LTPS process without additional process modification. Employing the proposed circuit, the operating rate to refresh static image can be reduced from 60Hz to 3Hz and providing inversion voltage through the analog memory. The analog MIP circuit can be operated with two row lines only, which can decrease the asymmetric inversion voltage by adding a reference voltage to the proposed circuit.

2. LTPS Process

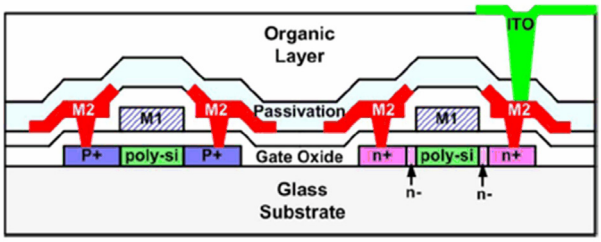

Figure 1. Cross-sectional view of LTPS TFT technology.

Figure 1 shows the cross-sectional view of LTPS TFT technology [9]. Fabrication process starts from the buffer layer which was deposited on the glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density varied from 340mJ/cm^2 to 420mJ/cm^2. The recrystallized poly-Si films were patterned into the active islands. Afterward, a 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick molybdenum was deposited and patterned as the gate electrode. The n^- doping was direct self-aligned to the gate electrode without additional mask process. The n^+ source/drain regions were defined by one mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick titanium/aluminum/titanium tri-layer metal was deposited and patterned to be the metal pads. For the analog pixel memory circuit verification, the channel length of all devices is kept as 5μm, while the channel width is varied from 30μm to 3μm in the circuit.

3. Circuit Schematic and Operations

Figure 2 shows the cooperation and connection between the proposed analog memory cell and the original pixel of LCD. During the standby mode, the scan driver switches input from row signal (Row [N]) to control signals. Source driver provides Vdata (Vdata=|Vp|+|Vt|) to the data line where Vp is the original pixel data and Vt is the threshold voltage of Poly-Si TFT. Then, the analog memory cell samples Vdata and cooperates with control signals to supply the capacitive loading (C_{LC}) at Vout. Through this arrangement, the memory cell can self generate inversion voltage for C_{LC}. Therefore, the source driver can be turned off at this duration until the specific frame

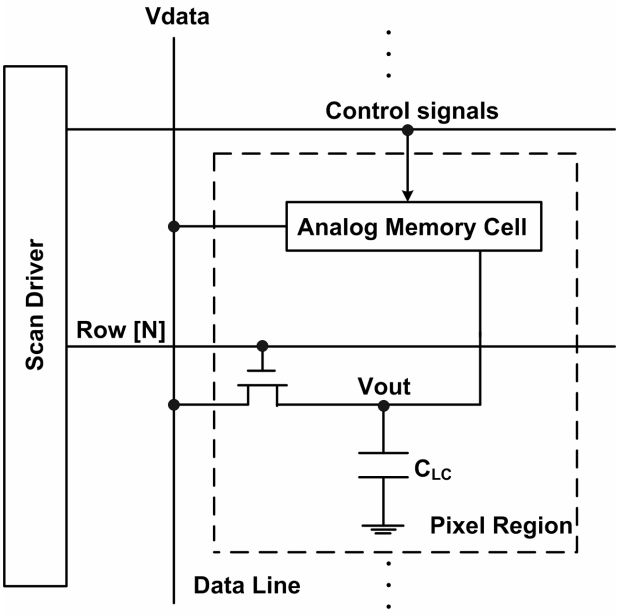

Figure 2. New proposed analog memory cell connected to the original pixel.

time is arrived. For example, if the frame time is 33.2ms, the source driver can be operated from 60Hz down to 30Hz for refreshing static image. The conventional frame time of TFT-LCDs is about 16.6ms (60Hz).

Figure 3 depicts the proposed circuit and the corresponding waveforms of scan lines. The circuit is composed of two driving transistors (M1, M2) and five switch transistors (M3, M4, M5, M6, and M7). The operation is divided into three periods, including the data voltage pre-charging (T1), positive (T2), and negative (T3) voltage holding periods. In the T1 period, Scan2 and Scan3 are set to turn off the transistors M3 and M6. The driving transistor M1 is operated as a source follower and Vout becomes Vdata–Vtn at the end of this period, where Vtn is the threshold voltage of M1. In the meanwhile, the storage capacitor (Cst) is set to the voltage of Vdata-Vref (where V_A=Vdata and V_B=Vref). In the T2 period, Scan1 becomes low to turn off M7. Except for M7, other transistors are all kept at the previous states. The gate voltages of M1 and M2 are Vdata and Vref, respectively. Vout remains Vdata-Vtn at the positive data holding period (T2). At the T3 period, Scan2 and Scan3 are set to turn off M4 and M5. Because M3 is turned on, Vref is applied to the node A. The voltage of node B goes to 2Vref-Vdata because Cst is boosted by the voltage at node A (V_A). Figure 4 shows the conceptual diagram of the operation principle to the proposed analog pixel memory cell. At the beginning of T3 period, M2 is operated as a source follower and the output voltage goes to 2Vref-Vdata+|Vtp| and then holds this voltage level until the next period comes, where |Vtp| is the absolute threshold voltage of M2.

In the standby mode, Vout is varied by the M1 and M2 source followers, respectively. The threshold voltage difference between Vtn and |Vtp| will cause non-symmetric output waveforms, so liquid crystal can't present equal transmittance.

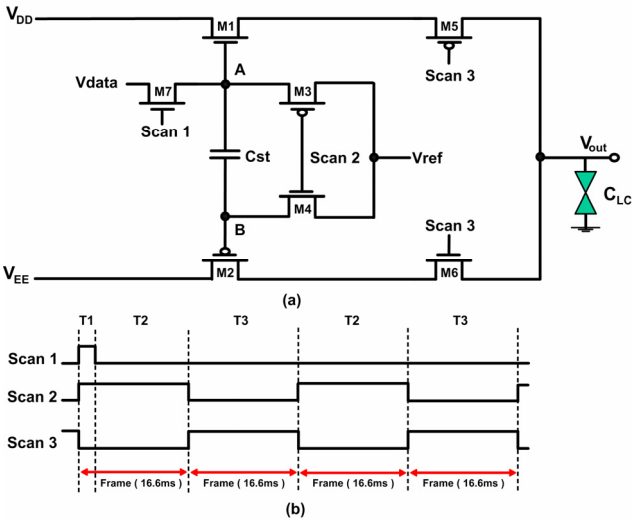

Figure 3. Schematic of (a) the proposed memory circuit and (b) the corresponding control signals. The circuit is composed of two driving transistors (M1, M2) and five switch transistors (M3, M4, M5, M6, and M7).

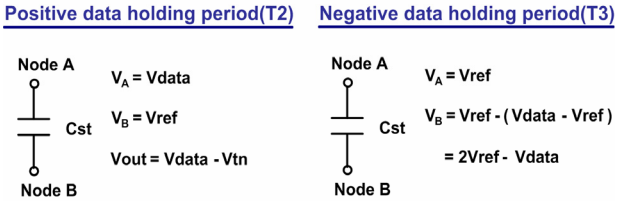

Figure 4. Conceptual diagram of the operation principle.

In order to solve this issue, it sets

$$\Delta V = Vtn - |Vtp|, \quad (1)$$

and the request for negative data holding period (T3) is to generate opposite sign voltage (-Vout) in the positive data holding period (T2). Vout wll become - (Vdata -Vtn), which gives

$$-(Vdata - Vtn) = V_B + |Vtp| = 2Vref - Vdata + |Vtp|. \quad (2)$$

Derived from Eq. (2), the optimized reference voltage (Vref) can be set to achieve the cancellation of threshold voltage difference between M1 and M2. The reference voltage is shown as

$$2Vref = Vtn - |Vtp| = \Delta V. \quad (3)$$

In other words, by adjusting the reference voltage, the problem of asymmetric inversion voltage for analog MIP cell can be solved by the design method. This work develops a robust analog memory cell with the function of self voltage inversion, which requires fewer scan lines than conventional digital memory. Therefore, the proposed analog pixel memory cell is suitable for high resolution MIP application.

4. Experimental Verification

A. Simulation

The proposed analog pixel memory circuit has been designed and verified by the HSPICE software with the RPI model (Level=62) in a 3-μm LTPS process. The device dimensions of the proposed circuit are shown in Table 1. The ratio of channel width (W) to channel length (L) for driving transistors M1 and M2 are 30μm/5μm, and those for switch transistors (M3, M4) and (M5, M6, M7) are 3μm/5μm and 5μm/5μm, respectively. Furthermore, the storage capacitor (Cst) is 5pF and the DC voltage supplies are 5V and -5V. Figure 5(a) depicts the simulation results of the output (Vout) voltage under Vdata inputs of 1.5V, 2.5V, 3.5V, and 4.5V, respectively. With the power saving concept, Figure 5(a) shows twenty frame time (16.6ms×20=332ms) per Scan1 pulse which is equivalent to a frame rate of 3Hz for refreshing static image. The power consumption comes from source driver only when Vdata is sampled by the proposed analog memory cell. Afterward, the cell works between the positive and negative data holding periods to generate positive and negative pixel voltages at Vout only by the control signals. Figure 5(a) also shows the output inversion voltage is symmetric no matter how the input data changes. Besides, the high and low voltage level is decreased approximately a threshold voltage due to the operation of source followers.

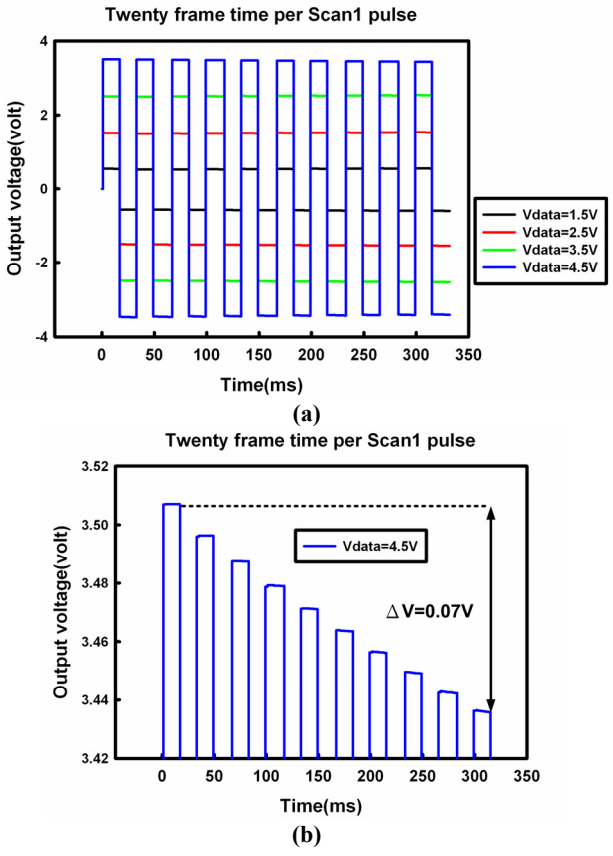

Figure 5. (a)The simulated output inversion voltage when Vdata=1.5V, 2.5V, 3.5V, and 4.5V in twenty frame time per Scan1 pulse. (b)The partial enlarged plot of (a) when Vdata is 4.5V.

Figure 5(b) gives the partial enlarged plot of Fig. 5(a) when Vdata is 4.5V. After twenty frame time, the simulation result shows the output voltage difference from initial Vdata is only 0.07V. This result represents that the proposed circuit could be effectively operated higher than 5-bit (data range/one gray scale=3.5/0.07=50) digital memory at the frame rate of 3Hz.

B. Measurement

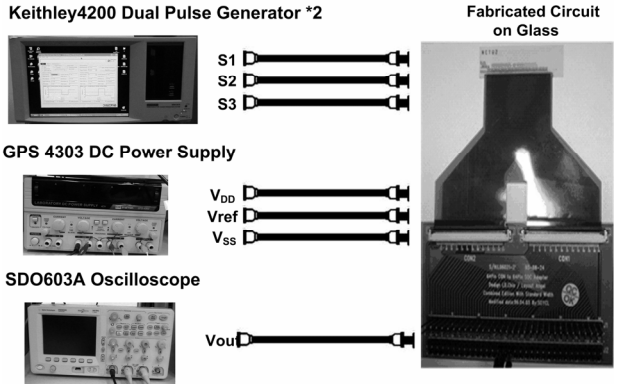

Figure 6. The fabricated on-panel circuit for analog pixel memory and the corresponding measurement setup.

For measurement setup, synchronous signals are generated by pulse card of Keithly 4200-scs. Input range of Scan1 and (Scan2, Scan3) are set as 0V to 10V and -5V to 5V, respectively. Digital oscilloscope is utilized to observe output waveforms as shown in Figure 6. For circuit verification, twenty frame time per Scan1 is used to verify the output waveforms whether it could realize the design function.

Figure 7 shows that when Vdata varied from 1V to 4V with the step of 1V, the output inversion signal was 0V to 0V, 1V to -0.998V, 2V to -2.015V, and 3V to -2.975V, when Vref is 0.2V (ΔV is about 0.4V). It shows that the inaccuracy for polarity inversion difference is no more than 0.025V because of Vref feeding.

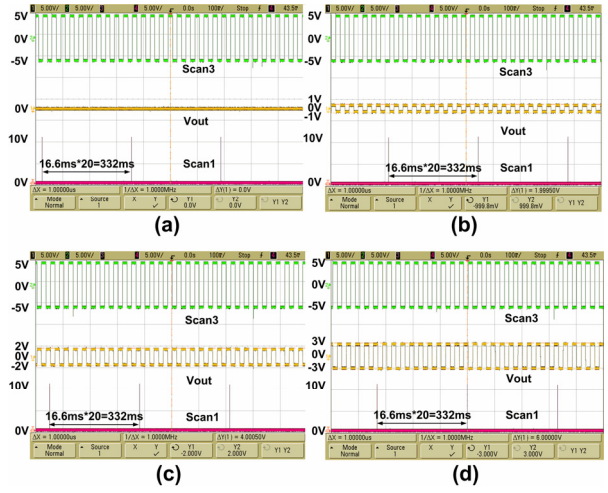

Figure 7. Measured results under (a)Vdata=1V, (b)Vdata =2V, (c)Vdata=3V, and (d)Vdata=4V in twenty frame time per Scan1 pulse.

Table 1. Device dimensions of analog memory cell.

	M1 ~ M2	M3~M4	M5~M7
Size (W/L)	30μm / 5μm	3μm / 5μm	5μm / 5μm

Besides, the maximum output decay voltage is less than 0.075V during twenty frame time when Vdata is 4V, which is consistent with the simulation results. The decay error comes from the parasitic effect of transistors. During the T2 and T3 alternative changing periods, node B (V_B) and node A (V_A) are coupled by the parasitic capacitance and storage capacitance in Fig. 3(a). Because Vout is followed by V_A and V_B, the coupling decay value will directly affect output voltage. For example, from positive data holding period changing to negative data holding period, the voltage at storage capacitor can be shown in the following [10]

$$V_B = Vref - \frac{Cst}{Cgs2 + Cgd2 + Cst + Cgs4}(Vdata - Vref). \quad (4)$$

The second term of Eq. (4) is reduced because of capacitive voltage division, where Cgs2, Cgd2, and Cgs4 are the parasitic capacitance of M2 and M4. Moreover, this effect is taken place per polarization inversion since there is no data refreshing to cause output decay errors. In other words, after more frame time, the holding voltage is smaller than the front one. In order to decrease the non-ideal effect, storage capacitor (Cst) has to be designed as large as possible to meet the ideal case in Eq. (2). However, it limits the LCD's aperture ratio. For measurement consideration, the capacitive ratio of oscilloscope and liquid crystal is about thirty times. The size of M1 and M2 has to be designed larger (30μm/5μm). Therefore, larger storage capacitor (Cst=5pF) is needed to verify the functionality of the proposed circuit.

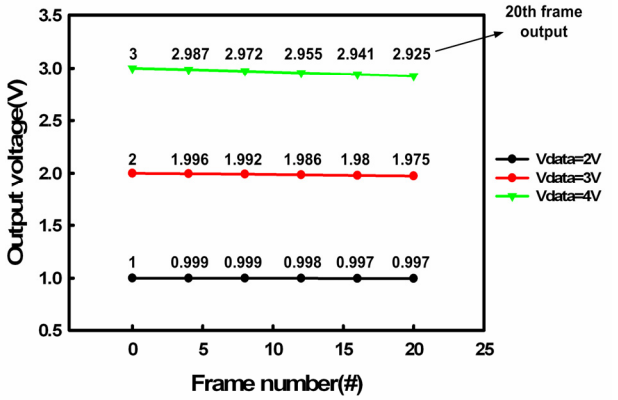

Figure 8. The output voltage decay under different frame number with different Vdata.

Figure 8 shows the output voltage decay under different frame number with different Vdata. The maximum decay value is no more than 0.075V when Vdata is 2V, 3V, and 4V. It means that the operating of source driver can be reduced from 60Hz to 3Hz. Power consumption is reduced to about twenty times from the normal operation at standby mode. Besides, frame number is chosen by the tolerance of specified output decay for higher resolution. By integrating the proposed MIP circuit on the pixel, better image quality can be obtained.

5. Conclusion

The proposed analog pixel memory circuit can achieve the power saving purpose for LCD panel applications, which has been successfully verified in a 3-μm LTPS process. It can reduce the frame rate from 60Hz to 3Hz to refresh static image. The maximum voltage decay is less than 0.075V under the input data from 1V to 4V in the experimental results.

6. Acknowledgment

The authors would like to thank the support from AU Optronics Corporation, Hsinchu, Taiwan, for fabrication of the proposed circuit on glass substrate in LTPS technology.

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