Layout Optimization on ESD Diodes for Giga-Hz RF and High-Speed I/O Circuits

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***Abstract* -- The diode operated in forward-biased condition has been widely used as an effective on-chip ESD protection device at GHz RF and high-speed I/O pads due to the small parasitic loading effect and high ESD robustness in CMOS integrated circuits (ICs). This work presents new ESD protection diodes realized in the octagon, waffle-hollow, and octagon-hollow layout styles to improve the efficiency of ESD current distribution and to reduce the parasitic capacitance. The new ESD protection diodes can achieve smaller parasitic capacitance under the same ESD robustness level as compared to the waffle diode. Therefore, the signal degradation of GHz RF and high-speed transmission can be reduced due to smaller parasitic capacitance from the new proposed diodes.**

I. Introduction

Electrostatic discharge (ESD) has become the major concern of reliability for integrated circuits (ICs) in nanoscale CMOS technology. The thinner gate oxide and shallower diffusion junction seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [1]-[3]. In order to sustain the required ESD robustness, the on-chip ESD protection devices must be drawn with large enough device dimension. However, the parasitic loading effects of the ESD protection devices with large device dimension will obviously degrade the circuit performance of signal transmission [4]-[5]. In order to reduce the circuit performance degradation, the parasitic capacitance (C_{ESD}) of the ESD protection devices must be minimized but the ESD robustness is still kept at the reasonable level [6]. ESD protection designs for GHz RF and high-speed I/O interface circuits must be optimized with consideration of parasitic capacitance and ESD protection capability.

A typical on-chip ESD protection scheme for GHz RF or high-speed I/O applications is shown in Fig. 1, where two ESD diodes at I/O pad are cooperated with the turn-on efficient power-rail ESD clamp circuit to discharge ESD current in the forward-biased condition. In order to minimize the parasitic capacitance caused by the ESD protection diodes and to achieve satisfactory ESD robustness, the high frequency characteristics and the ESD levels of the ESD protection diodes in a 90-nm CMOS process were evaluated in this work to obtain the dependence of device size on ESD robustness and parasitic capacitance. Furthermore, the layout style of ESD protection diode will also directly affect its ESD robustness and parasitic capacitance. In previous studies [7]-[8], the ESD protection diodes realized in the waffle layout style have been verified to achieve better figure-of-merit (FOM), which is suitable to GHz RF and high-speed I/O applications.

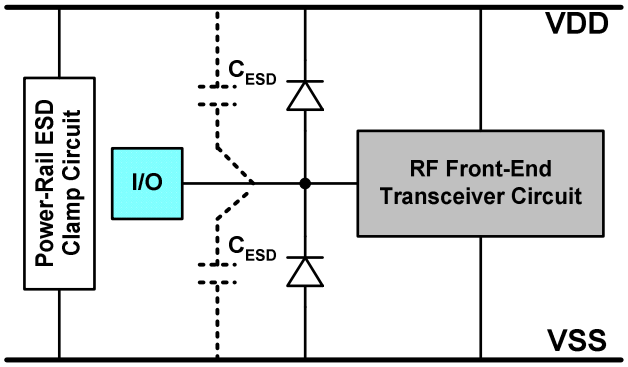


Fig. 1. Typical ESD protection scheme with double diodes for RF front-end or high-speed I/O applications.

Generally, the most important FOM used to evaluate the performance of the ESD protection diode is I_{CP}/C_{ESD}, where I_{CP} is the current level at which the measured I-V curve deviates from its linearly extrapolated value by 20% [7]. Consequently, it is desired to implement the ESD protection diode with a large ratio of I_{CP}/C_{ESD}. It is better for the ESD protection diode to achieve higher I_{CP} and lower C_{ESD} at the specific layout area.

In order to further improve the I_{CP}/C_{ESD}, the area of active junction region in ESD protection diode must be minimized to attain low parasitic capacitance, but its junction perimeter must be maximized to enhance the ESD robustness. In this work, the ESD protection diodes realized in waffle, octagon, waffle-hollow, and octagon-hollow layout styles are fabricated in a 90-nm CMOS process. According to the measured results, the ESD protection diodes with octagon and hollow layout styles can successfully boost the I_{CP}/C_{ESD} to make the diodes more profitable to GHz RF and high-speed I/O applications.

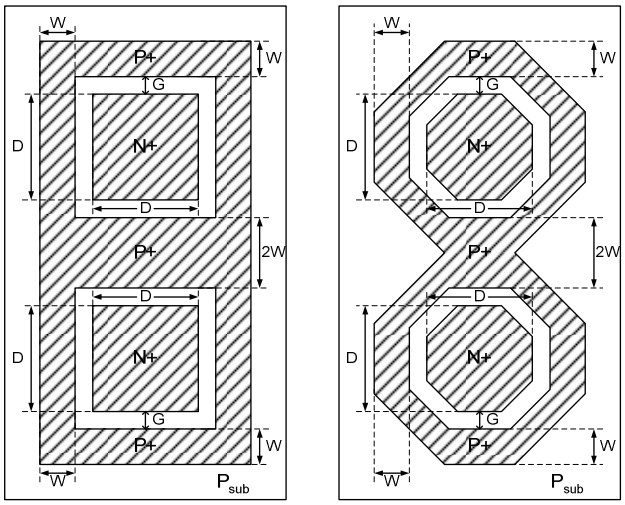
II. ESD Protection Diodes

For the $N+/P_{sub}$ diode, the GND and I/O nodes are electrically connected to P+ diffusion and N+ diffusion, respectively. Under normal circuit operation, the diode is kept off due to the reverse-biased condition between the P_{sub} and N+ diffusion regions. Although the diode is turned off, there is still an intrinsic junction capacitance of the diode seen by the signals at the I/O pad. On the other hand, the diode should be turned

on to conduct ESD current at forward-biased condition under ESD stresses. Therefore, the junction capacitance of diode at reverse-biased condition and the ESD protection capability of diode at forward-biased condition are the important parameters to be investigated in the following.

A. Waffle and Octagon Layout Styles

The device layout top views of the ESD protection diodes with waffle and octagon layout styles are shown in Figs. 2(a) and 2(b), respectively. The octagon layout style is formed from waffle layout style but the four corners are cut off. When the junction area of waffle and octagon diodes is reduced, they can achieve lower parasitic capacitance. Compared to the waffle diode, the junction perimeter and junction area of the octagon diode are simultaneously smaller than those of the waffle diode by 17%. Fortunately, the risk of damages located at the corner can be reduced by forming octagon layout style because the corner angle of octagon diode is larger than that of waffle diode. Therefore, the octagon diode can be supposed to have better ESD level than waffle diode.



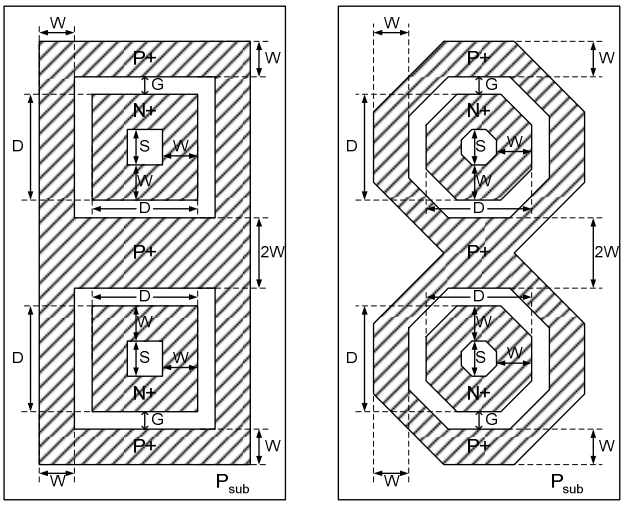
(a) (b)

Fig. 2. Device layout top view of the ESD protection diodes with (a) waffle layout style and (b) octagon layout style.

B. Waffle-Hollow and Octagon-Hollow Layout Styles

The two new proposed diodes investigated in this study are illustrated in Figs. 3(a) and 3(b), which are called as the waffle-hollow and octagon-hollow layout styles, respectively. For GHz RF and high-speed I/O applications, the parasitic capacitance of the ESD protection diode is the key factor to directly affect the performance of GHz RF and high-speed I/O circuits. The purpose of forming the hollow layout is to reduce the active junction area and to keep the active junction perimeter at the same time by removing the N+ central diffusion region off. The diodes with hollow layout style can be expected to attain a great reduction of parasitic capacitance without degrading ESD robustness severely at the same time.

Based on the waffle layout style studied in previous work [7]-[8], the octagon, waffle-hollow, and octagon-hollow layout styles are proposed and fabricated in a 90-nm CMOS process to investigate the dependence between ESD robustness and parasitic capacitance on diode layout styles. The important layout parameters of those investigated diodes are listed in Table I, where the different spacings are also marked in Fig. 2 and Fig. 3, respectively.



(a) (b)

Fig. 3. Device layout top view of the ESD protection diodes with (a) waffle-hollow layout style and (b) octagon-hollow layout style. The center region is drawn with the STI region to effectively reduce the parasitic capacitance.

TABLE I
THE MEASURED DEVICE CHARACTERISTICS OF DIODE UNDER DIFFERENT TEST STYLES

Layout Style	Waffle			Octagon			Waffle-hollow			Octagon-hollow		
	A	B	C	A	B	C	A	B	C	A	B	C
Sizes of Device (μm)	W=1 G=0.5 D=3	W=1 G=0.5 D=4	W=1 G=0.5 D=5	W=1 G=0.5 D=3	W=1 G=0.5 D=4	W=1 G=0.5 D=5	W=1 G=0.5 D=3 S=1	W=1 G=0.5 D=4 S=2	W=1 G=0.5 D=5 S=3	W=1 G=0.5 D=3 S=1	W=1 G=0.5 D=4 S=2	W=1 G=0.5 D=5 S=3
N+ Junction Perimeter (μm)	24	32	40	19.92	26.56	33.20	24	32	40	19.92	26.56	33.20
Layout Area (μm^2)	72	98	128	59.76	81.34	106.24	72	98	128	59.76	81.34	106.24
N+ Occupied Area (μm^2)	18	32	50	14.94	26.56	41.50	18	32	50	14.94	26.56	41.50
Total N+ Junction Area (μm^2)	18	32	50	14.94	26.56	41.50	16	24	32	13.28	19.92	26.56

III. EXPERIMENTAL RESULTS

The testchips of diodes with the waffle layout style and the new proposed layout styles have been fabricated in a 90-nm CMOS process. These diodes are prepared with the consideration of two-port *S*-parameter measurement, TLP measurement, and HBM ESD robustness measurement.

A. Parasitic Capacitance

The diode devices are arranged with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port *S*-parameter measurement. During the S-parameter measurement, the P+ and N+ diffusion regions of the diode devices are connected to port 1 and port 2, respectively, and they are both biased at 0V.

In order to extract the characteristics of the intrinsic device at high frequency, the parasitic effects of the pad must be de-embedded [9]-[11]. The test structures, one including the DUT

and the other excluding the DUT, as shown in Figs. 4(a) and 4(b), were implemented in the same test chip [9]-[10]. The Y_{22}-parameter can be obtained from the measured two-port *S*-parameters by

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{Z_0((1+S_{11})(1+S_{22})-S_{12}S_{21})}, \quad (1)$$

where Z_0 is the termination resistance of 50Ω. The measured *Y*-parameter of the including-DUT pattern is labeled as $Y_{22\text{-meas}}$, and the measured *Y*-parameter of the excluding-DUT pattern is labeled as $Y_{22\text{-open}}$. The intrinsic device characteristics, $Y_{22\text{-DUT}}$, can be obtained by subtracting $Y_{22\text{-open}}$ from $Y_{22\text{-meas}}$. The parasitic capacitance (C_{ESD}) of each diode can be extracted from the *Y*-parameter of the intrinsic device by

$$C_{ESD} = \frac{\mathrm{Im}(Y_{22-DUT})}{2\pi f}, \quad (2)$$

where *f* is the operating frequency. The extracted parasitic capacitances of the fabricated diode devices at 2.5GHz under zero DC bias are listed in Table II and shown in Fig. 5.

From the measured results of the diode devices with waffle and octagon layout styles, the extracted parasitic capacitances are obviously proportional to the N+ occupied area. Meanwhile, the reductions of parasitic capacitances can achieve 16%, 26%, and 39% by modifying the diodes in size A, size B, and size C from waffle to waffle-hollow layout styles, respectively. Similarly, it can achieve the reductions of parasitic capacitance of 13%, 25%, and 38% by modifying the diodes from octagon to octagon-hollow layout styles. This great reduction of parasitic capacitance is the key factor to significantly improve the FOM of the diodes with hollow layout style.

B. Transmission Line Pulsing (TLP) Measurement

In order to investigate the device behavior during high ESD current stress, transmission line pulsing (TLP) generator with a pulse width of 100ns and a rise time of ~10ns is used to measure the second breakdown current (It_2) of the device [12]. For the ESD protection diode, it is suggested that an appropriate upper-bound current level, I_{CP}, is utilized because the ESD protection diode should never be designed to discharge ESD current near its failure level [7]-[8]. By using TLP, the on-resistance (R_{ON}), It_2, and I_{CP} of the diode devices under positive stresses at the P+ diffusion region with grounded N+ diffusion region are measured and listed in Table II. Apparently, the R_{ON} is decreased and the I_{CP} is increased with the increased N+ junction perimeter.

Fig. 6 shows the measured TLP I-V curves of ESD protection diodes with different layout styles in size A. The operation of ESD diodes is in the forward-biased condition with the cooperation of active power-rail ESD clamp circuit. The definition of I_{CP} is also marked clearly in Fig. 6. According to the measured results, the reductions of I_{CP} are 0.4%, 9.6%, and 11.5% for the waffle diodes in size A, size B, and size C, respectively. Also, they are 2.5%, 5.1%, and 9.5% for the octagon diodes in size A, size B, and size C, respectively. Compared with the reductions of parasitic capacitance, the removed N+ central diffusion region is originally flowed by a small part of total ESD discharging current. Consequently, removing the N+ central diffusion region of the diodes can greatly reduce the parasitic capacitance without degrading the ESD protection capability.

TABLE II
THE MEASURED RESULTS AND FIGURE-OF-MERIT OF DIODE DEVICES WITH DIFFERENT LAYOUT STYLES

Layout Style	Waffle			Octagon			Waffle-hollow			Octagon-hollow		
	A	B	C	A	B	C	A	B	C	A	B	C
C_{ESD} (fF)	16.70	31.18	47.64	13.65	26.44	41.39	13.92	22.95	28.95	11.85	19.89	25.61
It_2 (A)	0.948	1.418	1.851	0.861	1.241	1.636	0.944	1.281	1.639	0.840	1.178	1.481
I_{CP} (A)	0.755	1.192	1.675	0.664	1.026	1.434	0.737	1.118	1.428	0.656	0.981	1.282
R_{ON} (Ω)	1.690	1.280	1.074	1.912	1.460	1.156	1.693	1.314	1.093	1.967	1.509	1.299
V_{HBM} (kV)	1.7	2.6	3.5	1.4	2.2	2.9	1.7	2.3	3.1	1.4	2.0	2.7
I_{CP} / C_{ESD} (mA/fF)	45.21	38.23	35.16	48.64	38.80	34.65	52.95	48.71	49.33	55.36	49.32	50.06

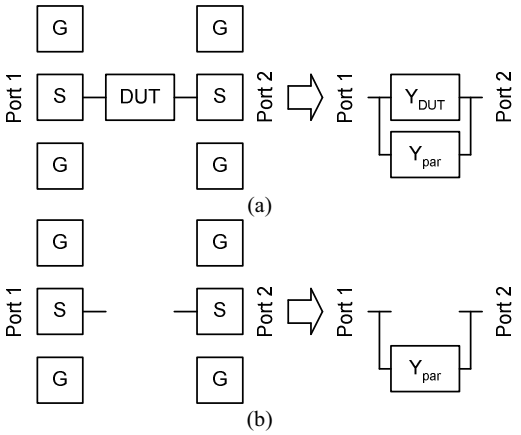


Fig. 4. Layout top views for de-embedded calculation to extract the parasitic capacitance of the fabricated ESD diodes with (a) including-DUT pattern and (b) excluding-DUT pattern.

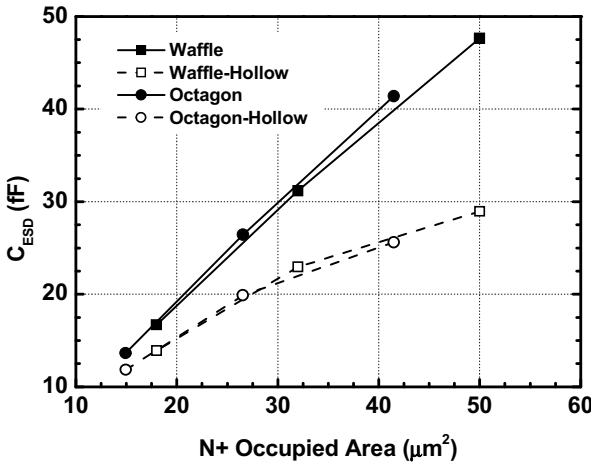


Fig. 5. Dependence of C_{ESD} extracted from S-parameter at 2.5GHz under zero DC bias on the N+ occupied area of diode devices with different layout styles.

C. ESD Robustness

The human-body-model (HBM) ESD robustness of the fabricated diodes is also listed in Table II. The relationship between the HBM ESD level (V_{HBM}) and the It_2 based on the measured results in this work is about

$$V_{HBM} \approx (1800 + R_{ON}) \times It_2, \quad (3)$$

where R_{ON} is the turn-on resistance of the diode. The HBM ESD levels of all ESD protection diodes are within the range of 1.4-3.5kV.

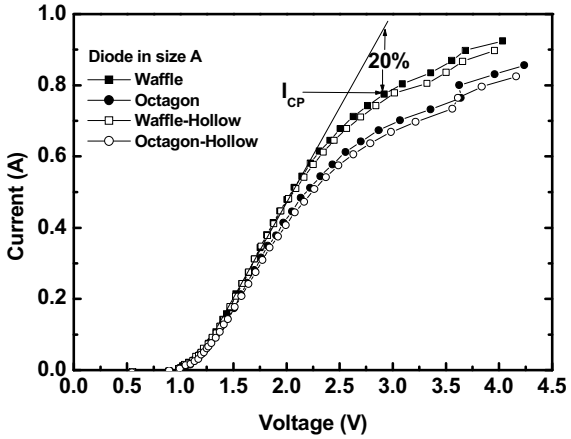


Fig. 6. The measured TLP I-V curves of ESD protection diodes with different layout styles in size A under forward-biased condition.

D. FOM Comparison and Discussion

The most important FOM, I_{CP}/C_{ESD}, among the diodes is listed in Table II and illustrated in Fig. 7. The trend of I_{CP}/C_{ESD} is apparently increasing from non-hollow to hollow layout style due to the reduction of parasitic capacitance, and the results exactly meet the expectation of layout design. According to the experimental results of diodes with different layout styles, the diodes with hollow layout styles can apparently achieve higher ESD robustness under the same parasitic capacitance. Besides, the I_{CP}/C_{ESD} can also be slightly improved from waffle (or waffle-hollow) diode to octagon (or octagon-hollow) diode due to the relaxation of current distribution located at the smoother corners.

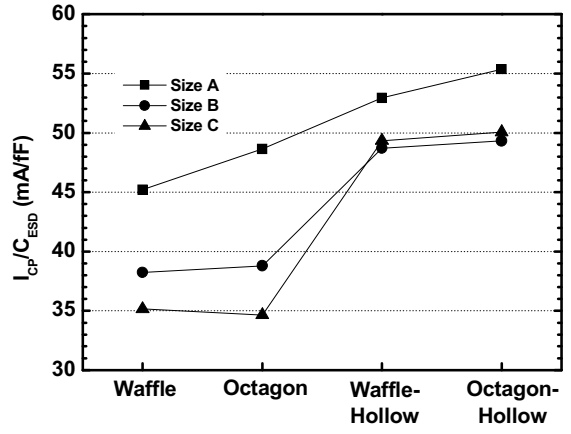


Fig. 7. The I_{CP}/C_{ESD} of ESD protection diodes with different layout styles.

The I_{CP}/C_{ESD} values of waffle-hollow and octagon-hollow diodes in size B and size C can achieve almost the same level as that of waffle diode in size A. It represents that the diode with hollow layout style in large size still can sustain I_{CP} as high as that of the diode with waffle layout style in small size under the same parasitic capacitance. Although the waffle diode in small size theoretically has larger ratio of N+ junction perimeter to N+ junction area, carefully optimizing the size of waffle diode is still required to avoid any capacitance penalty from junction perimeter [7]-[8]. Therefore, it is not necessary to simply shrink the device size of waffle diode to achieve high value of I_{CP}/C_{ESD}. In this work, it has been verified that there are two methods, forming octagon and hollow layout styles, to effectively improve the I_{CP}/C_{ESD} of the diodes.

IV. CONCLUSION

The new proposed diodes with octagon and hollow layout styles have been successfully verified in a 90-nm CMOS process. The layout optimization is the essential element to minimize the parasitic capacitance and to improve ESD robustness of the ESD protection diodes for GHz RF and high-speed I/O applications. As compared to the diodes with waffle layout style, the new proposed diodes with hollow layout styles have been demonstrated to significantly improve ESD robustness under the same parasitic capacitance. Therefore, the proposed waffle-hollow and octagon-hollow diodes are more suitable to be implemented to GHz RF and high-speed I/O circuits.

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