New Transient Detection Circuit to Detect ESD-Induced Disturbance for Automatic Recovery Design in Display Panels

Cheng-Cheng Yen[1], Wan-Yen Lin[1], Ming-Dou Ker [1, 2], Che-Ming Yang[3], Shih-Fan Chen[3], and Tung-Yang Chen[3]

[1]Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
[2]Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan
[3]Research and Development Center, Himax Technologies, Inc., Tainan, Taiwan

***Abstract*- A new transient detection circuit against system-level electrostatic discharge (ESD) transient disturbance is proposed for display panel protection. The circuit function to detect positive or negative electrical transients under system-level ESD tests has been evaluated in HSPICE simulation and verified in 0.13-μm silicon chip. The output signal of the proposed transient detection circuit can be used as a firmware index to execute system automatic recovery operation. With hardware/firmware system co-design, the immunity of display panels against transient disturbance under system-level ESD tests can be enhanced.**

Keywords- detection circuit; electrostatic discharge (ESD); system-level ESD test.

I. INTRODUCTION

Recently, the transient disturbance events due to system-level electrostatic discharge (ESD) tests have attracted more attention in microelectronic circuits and display systems [1]-[14]. This tendency results from not only the progress of more integrated functions into a single chip, such as mixed-signal, mixed-voltage, system-on-chip (SOC), etc., but also from the strict requirements of reliability test standards, such as the system-level ESD test standard of IEC 61000-4-2 [15]. Typically, if microelectronic products are required to achieve the immunity of "level 4" in the IEC 61000-4-2 standard, the equipment under test (EUT) should sustain the ESD stress level of as high as ±8 kV (±15 kV) under contact-discharge (air-discharge) test mode. Such ESD-generated transient voltage acts as underdamped sinusoidal voltage waveform with large amplitude and randomly exists on power, ground, or input/output (I/O) pins of integrated circuits (ICs) inside the microelectronic system. With the scaled clearance between PMOS and NMOS devices in advanced semiconductor technology, it has been proven that such ESD-induced electrical transient disturbance can cause transient-induced latchup (TLU) failure on the inevitable parasitic silicon controlled rectifier (SCR) inside CMOS ICs. It has been also reported that some CMOS ICs are very susceptible to system-level ESD stress, even though they have passed the component-level ESD qualifications such as the human-body-model (HBM) of ±2 kV, the machine-model (MM) of ±200 V, and the charged-device-model (CDM) of ±1 kV.

Component-level ESD tests often cause physical or hardware damage in a chip. However, for microelectronic systems with CMOS ICs, system-level ESD tests often cause soft errors, including frozen or locked states in the display panels. For consumer applications, most microelectronic products are required to automatically recover all electrical system functions without operator intervention when these ESD-induced soft errors happen. Typical on-chip ESD protection circuits in CMOS ICs can protect the internal circuits against component-level ESD damage, but they can not release the upset or frozen states generated by system-level ESD tests.

To solve these ESD-induced reliability events on microelectronic systems, one effective method is to add some discrete noise-decoupling components on the printed circuit board (PCB) to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD tests, as shown in Fig. 1. Different types of noise filter networks can be used to improve the system-level ESD immunity, including capacitor filter, ferrite bead, and several high-order noise filters. Therefore, for the IC industry, the chip-level solutions which can help the microelectronic system to execute automatic recovery operation without additional discrete components are highly desired.

In this work, an on-chip transient detection circuit is designed to detect fast electrical transients and verified in a 0.13-μm CMOS process. The system-level ESD gun operated in air-discharge test mode is used to evaluate the circuit performance of the proposed detection circuit. The proposed circuit can perform a hardware/firmware co-design solution to enhance the immunity of microelectronic display systems against ESD-induced electrical transient disturbance.

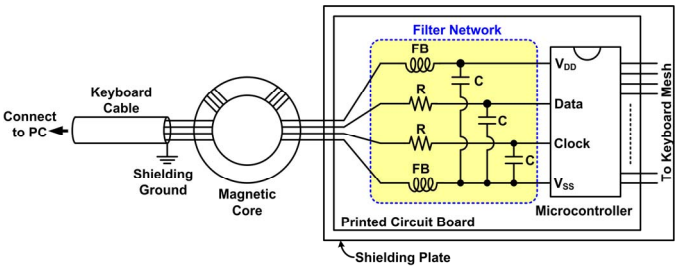


Fig. 1. The traditional solution to overcome the system-level ESD events in keyboard product by adding extra discrete components.

II. Proposed Transient Detection Circuit

In the previous works, some on-chip transient detection circuit designs have been proposed to detect transient noise [14]. However, the detection sensitivity may be influenced by some additional capacitors located between the input/output nodes of latch circuit or VDD/VSS power lines. In this work, an on-chip transient detection circuit without latch structure is proposed to detect the fast electrical transients generated from system-level ESD events.

A. Circuit Implementation

Fig. 2 shows the circuit structure of proposed on-chip transient detection circuit. The RC-based structure is designed to realize the transient detection function. The NMOS (M_{nr}) is used to provide the reset function to set the initial output voltage (V_{OUT}) as 1.8 V with the V_{DD} of 1.8 V in a 0.13-μm 1P5M CMOS process. With the feedback loop connected between the output node of inverter1 (inv1) and the gate of NMOS device (M_{n1}), the node V_A can be kept at V_{SS} of 0 V after initial reset operation. Under the system-level ESD stress, the ESD voltage has a fast rise time in the order of nanosecond (ns). In Fig. 2, the node V_X is biased at V_{DD} during the normal operating condition. When electrical transient disturbance happen, the voltage level of V_X has much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant in the order of microsecond (μs). Due to the longer delay of the voltage increase at the node V_X, the PMOS device (M_{p1}) can be turned on by the overshooting ESD voltage (coupled to V_{DD}) to pull up the voltage level at the node V_A from 0 V to 1.8 V. With the 3-stage buffer inverters, the output voltage of the proposed detection circuit finally transits from logic "1" to logic "0" to detect and memorize the occurrence of system-level ESD events.

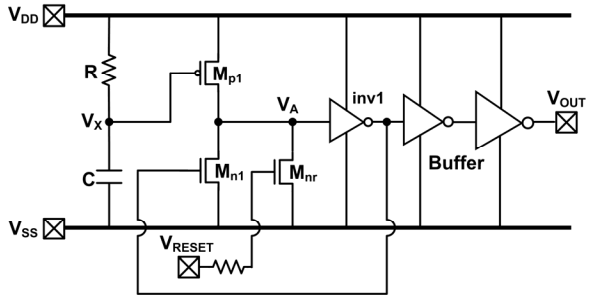


Fig. 2. The proposed on-chip transient detection circuit.

B. HSPICE Simulation for System-Level ESD Tests

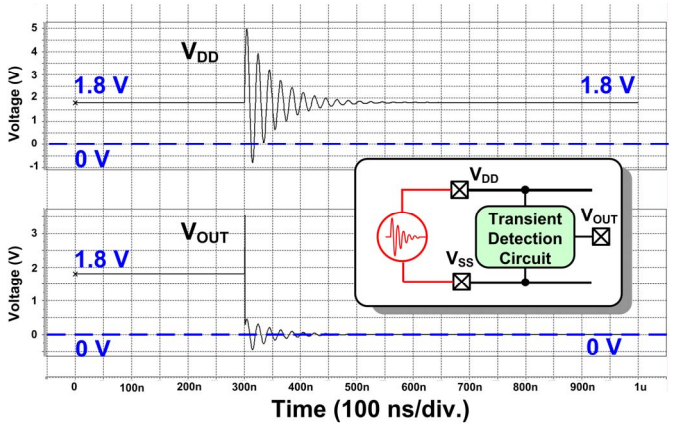
From the measured electrical transient waveforms, the approximate underdamped sinusoidal voltage waveform on power lines of CMOS IC during the system-level ESD tests has been observed. Therefore, a sinusoidal time-dependent voltage source with damping factor parameter, given by

$$V(t) = V_0 + V_a \cdot \sin(2\pi f(t - t_d)) \cdot \exp(-(t - t_d)D_a), \quad (1)$$

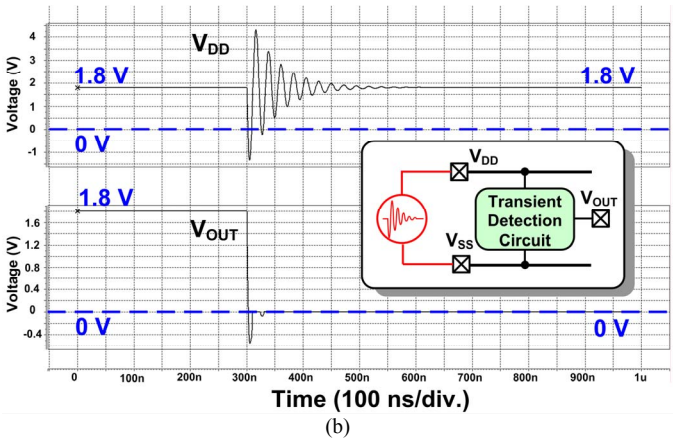
is used to simulate the coupling transient voltage during the system-level ESD event. With the proper parameters (including the voltage amplitude V_a, initial dc voltage V_0, damping factor D_a, frequency f, and time delay t_d), the underdamped sinusoidal voltage can be used to simulate the electrical transient voltage waveforms under system-level ESD tests. For positive-going or negative-going ESD voltage waveforms, the same parameters of V_0=1.8 V, $D_a = 2\text{x}10^7$ s^{-1}, f = 50 MHz, and t_d = 300 ns are used.

The simulated V_{DD} and V_{OUT} waveforms of the proposed detection circuit with positive-going and negative-going underdamped sinusoidal voltages coupled on V_{DD} power lines are shown in Figs. 3(a) and 3(b), respectively. Under the simulated positive-going underdamped sinusoidal ESD stress condition, V_{DD} begins to increase rapidly from 1.8 V. V_{OUT} is disturbed simultaneously during the V_{DD} disturbance. As a result, after V_{DD} finally returns to its normal voltage level of 1.8 V, V_{OUT} will be changed from 1.8 V to 0 V, as shown in Fig. 3(a).

Under the simulated negative-going underdamped sinusoidal voltage zapping condition, the V_{OUT} is influenced by the V_{DD} disturbance through the coupling paths. Finally, the output (V_{OUT}) of the proposed detection circuit is changed from 1.8 V to 0 V, as shown in Fig. 3(b). Therefore, in HSPICE simulation, the proposed transient detection circuit can detect and memorize the occurrence of ESD-induced underdamped sinusoidal transient disturbance.



(a)



(b)

Fig. 3. Simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip transient detection circuit under system-level ESD test with (a) positive-going, and (b) negative-going, underdamped sinusoidal voltages.

III. Experimental Results

The proposed circuit has been designed and fabricated in a 0.13-μm CMOS process. The chip area is 245μm x 155μm, as shown in Fig. 4.

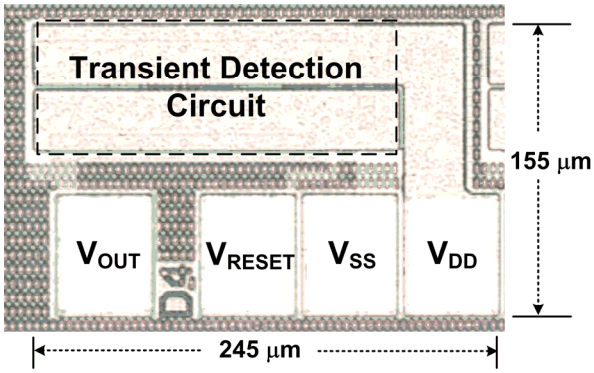


Fig. 4. Chip photo of the proposed on-chip transient detection circuit fabricated in a 0.13-μm CMOS process with 1.8-V devices.

In the IEC 61000-4-2 standard [15], the equipment specifications for different testing modes have been defined. For table-top equipment, the measurement setup should consist of a wooden table, standing on the ground reference plane (GRP). An insulating plane should be inserted between the EUT/cables and horizontal coupling plane (HCP).

Furthermore, in the IEC 61000-4-2 standard, two test modes have been also specified, which are the air-discharge test mode and the contact-discharge test mode. Under system-level ESD tests, the ESD energy is released from ESD gun. Different discharge tips are used for two different test modes. The round tip of ESD gun is used for air-discharge test and brought close to the EUT. The sharp tip of ESD gun is used for contact-discharge test modes and held in contact with the EUT. The measurement setup of system-level ESD test with the air-discharge test mode in IEC 61000-4-2 standard is shown in Fig. 5. The round discharge tip should be approached as fast as possible to the EUT. The air discharge is actuated by a spark to the EUT and the ESD energy holding time is at least 5 seconds. Under system-level ESD zapping conditions, the transient voltage coming from ESD will be coupled into all CMOS ICs inside EUT. The operations of CMOS ICs inside EUT would be disturbed by the system-level ESD-coupled energy.

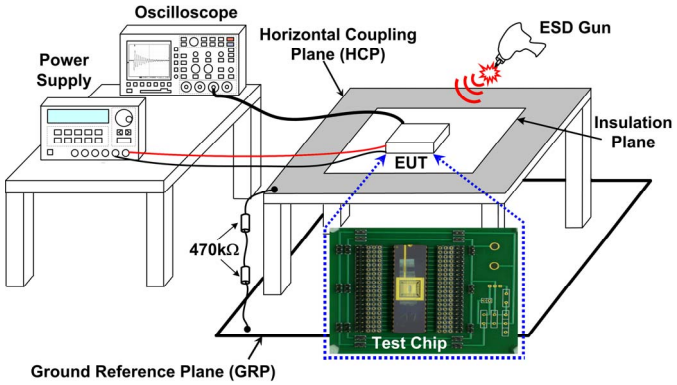
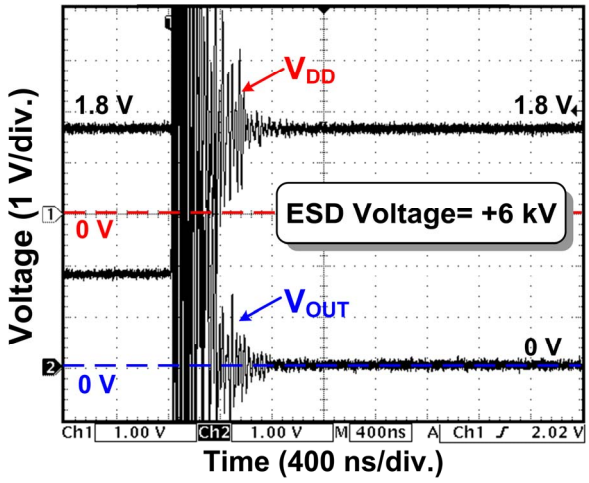


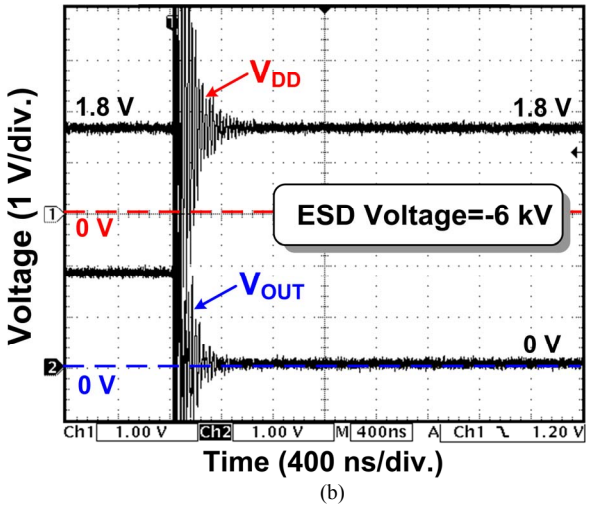
Fig. 5 Measurement setup for a system-level ESD test with air-discharge test mode according to IEC 61000-4-2 standard [15].

The measurement setup shown in Fig. 5 can verify the circuit performance of proposed transient detection circuit under system-level ESD test with air-discharge mode. The measured V_{DD} and V_{OUT} waveforms of the detection circuit under a system-level ESD test with the ESD voltage of +6 kV zapping are shown in Fig. 6(a). V_{DD} begins to increase rapidly from the normal bias voltage level of 1.8 V. Meanwhile, V_{OUT} begins to change under +6-kV system-level ESD stress. During the fast transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, the output voltage of the detection circuit has been changed from 1.8 V to 0 V.

The measured V_{DD} and V_{OUT} transient waveforms of the transient detection circuit under system-level ESD test with an ESD voltage of -6 kV zapping are shown in Fig. 6(b). During the ESD-induced transient disturbance, V_{DD} begins to decrease rapidly from the original bias voltage of 1.8 V and V_{OUT} is disturbed simultaneously. Finally, V_{OUT} is pulled down from 1.8V to 0 V after the system-level ESD test. Therefore, the detection circuit can memorize the occurrence of electrical transient under system-level ESD test with negative ESD voltage.



(a)



(b)

Fig. 6. Measured V_{DD} and V_{OUT} transient responses with ESD voltages of (a) +6 kV, and (b) -6 kV, zapping to the fabricated transient detection circuit inside an IC package.

IV. Application in Display Panel

For display system with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power supplies are needed for electrical display functions, as shown in Fig. 7. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and digital power line (VDDD) is used for shifter register and memory units. In the hardware/firmware system co-design, the transient detection circuit can connect with 1.8-V VDDD power line to detect and memorize the occurrence of ESD-induced transient disturbance coupled on digital subsystems of display panels. The detection results can be temporarily stored as ESD index for firmware check, as shown in Fig. 8. In the beginning, the output (V_{OUT}) state of the detection circuit is set to logic "1" by the power-on reset circuit or start-up procedures. When the electrical transients happen, the transient detection circuit can detect the occurrence of system-level ESD-induced disturbance and pull down the output state (V_{OUT}) from logic "1" to logic "0." At this moment, the system recovery index is also changed to logic "0" to initiate automatic recovery operation to restore the microelectronic display system to a desired stable state as soon as possible.

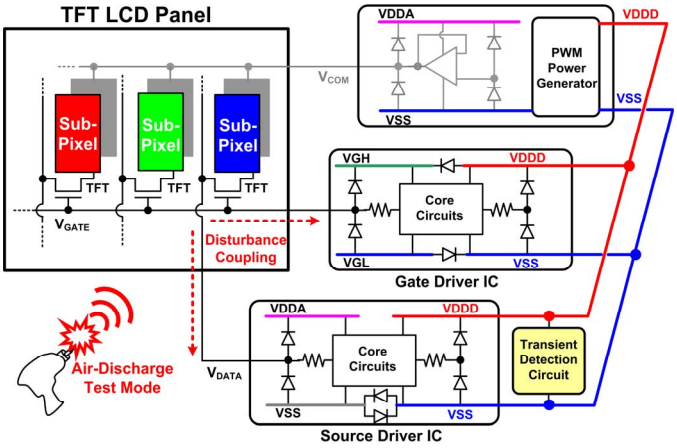


Fig. 7. Hardware/firmware system co-design on display system with TFT-LCD panel and the proposed transient detection circuit.

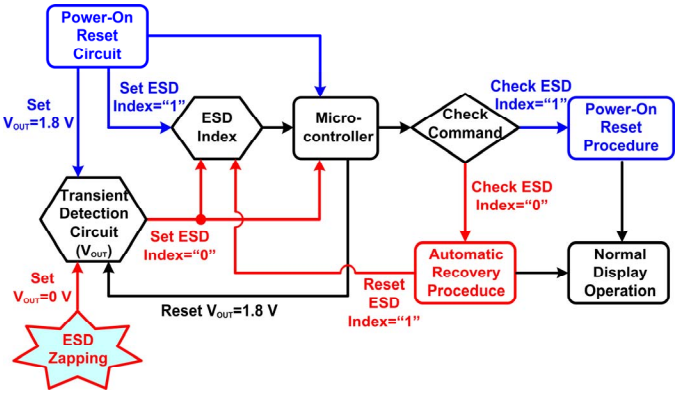


Fig. 8. Firmware flowchart to recover display system when system-level ESD electrical tansients happen.

V. Conclusion

An on-chip transient detection circuit to detect system-level ESD events has been proposed and successfully verified in a CMOS 0.13-µm process. The circuit performance under different positive and negative ESD-induced transient disturbance has been investigated in HSPICE simulation. The experimental results in silicon chip have confirmed that the proposed transient detection circuit can successfully detect and memorize the occurrence of fast electrical transients under system-level ESD tests. For microelectronic display panels, the proposed detection circuit can further cooperate with firmware design to provide an effective solution against the upset or frozen states caused by system-level ESD-induced electrical transient disturbance.

Acknowledgment

This work was partially supported by National Science Council, Taiwan, under Contract NSC 99-2811-E-009-051; and by Himax Technologies Inc., Taiwan.

References

[1] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*, John Wiley & Sons, 2009.

[2] W. Huang, and J. Dunnihoo, and D. Pommerenke, "Effects of TVS integration on system level ESD robustness," in *Proc. EOS/ESD Symp.*, 2010, pp. 145–149.

[3] L. Lou, C. Duvvury, A. Jahanzeb, and J. Park, "SPICE simulation methodology for system level ESD design," in *Proc. EOS/ESD Symp.*, 2010, pp. 65–73.

[4] G. Boselli, A. Salman, J. Brodsky, and H. Kunz, "The relevance of long-duration TLP stress on system level ESD design," in *Proc. EOS/ESD Symp.*, 2010, pp. 31–39.

[5] T. Brodbeck, W. Stadler, C. Baumann, K. Esmark, and K. Domanski, "Triggering of transient latch-up (TLU) by system level ESD," in *Proc. EOS/ESD Symp.*, 2010, pp. 49–57.

[6] G. Notermans, D. Maksimovic, G. Vermont, M. Maasakkers, F. Pusa, and T. Smedes, "On-chip system level protection of FM antenna pin," in *Proc. EOS/ESD Symp.*, 2010, pp. 83–90.

[7] K. Muhonen, P. Erie, N. Peachey, and A. Testin, "Human metal model (HMM) testing, challenges to using ESD guns," in *Proc. EOS/ESD Symp.*, 2009, pp. 387–395.

[8] E. Grund, K. Muhonen, P. Erie, and N. Peachey, "Delivering IEC 61000-4-2 current pulses through transmission lines at 100 and 330 ohm system impedances," in *Proc. EOS/ESD Symp.*, 2008, pp. 132–141.

[9] E. Grund, K. Muhonen, P. Erie, and N. Peachey, "Delivering IEC 61000-4-2 current pulses through transmission lines at 100 and 330 ohm system impedances," in *Proc. EOS/ESD Symp.*, 2008, pp. 132–141.

[10] M. Honda, "Measurement of ESD-gun radiated fields," in *Proc. EOS/ESD Symp.*, 2007, pp. 323–327.

[11] T. Smedes, J. Zwol, G. Raad, T. Brodbeck, and H. Wolf, "Relations between system level ESD and (vf-) TLP," in *Proc. EOS/ESD Symp.*, 2006, pp. 136–143.

[12] T.-H. Wang, W.-H. Ho, and L.-C. Chen, "On-chip system ESD protection design for STN LCD drivers," in *Proc. EOS/ESD Symp.*, 2005, pp. 316–322.

[13] N. Shimoyama, M. Tanno, S. Shigematsu, H. Morimura, Y. Okazaki, and K. Machida, "Evaluation of ESD hardness for fingerprint sensor LSIs," in *Proc. EOS/ESD Symp.*, 2004, pp. 75–81.

[14] M.-D. Ker and C.-C. Yen, "Transient-to-digital converter for system-level ESD protection in CMOS integrated circuits," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 3, pp. 620–630, Aug. 2009.

[15] IEC 61000-4-2 Standard, "*EMC – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*," IEC, 2008.