# Overview on the design of low-leakage power-rail ESD clamp circuits in nanoscale CMOS processes

*Invited Paper*

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***Abstract*—The circuit techniques to overcome the gate leakage issue in advanced nanoscale CMOS technologies are presented. These circuit techniques can reduce the total leakage current from the high value of 21$\mu$A in the traditional power-rail ESD clamp circuit down to only 96nA (under 1 Volt operating voltage, at room temperature) while maintaining very high ESD robustness (as high as 8kV HBM and 800V MM) in a 65-nm CMOS technology.**

## I. Introduction

Electrostatic Discharge (ESD) phenomenon is a charge flow that happens when two objects with different potential reach contact. This discharge is the result of the charge balance between the two objects, and usually causes a high energy transfer in a very short period of time. Such an ESD event can damage the components of an Integrated Circuit (IC). Typical ESD failures can be either thermal breakdown in silicon and/or melting metal interconnection due to the high current, or dielectric breakdown in gate oxide due to high voltage overstress [1]. To protect the circuits against ESD, protection structures such as large-sized MOSFET or Silicon Controlled Rectifiers (SCR) are placed around the inputs, outputs, and also between the $V_{DD}$ and ground lines [2]. Fig. 1 shows a typical whole-chip ESD protection scheme, where the power-rail ESD clamp circuit is highlighted. The protection device can be either a large-sized MOSFET ($M_{ESD}$) or an SCR, whereas the latter can offer better protection than the MOSFET, due to the lower holding voltage to sink more current before fail. For example, the power-rail ESD clamp circuit in a 65-nm technology, with a MOSFET clamp in the area of $70\mu m \times 80\mu m$ passes 4kV HBM [3], while using an SCR in the area of $60\mu m \times 8\mu m$ passes 8kV HBM [4]. The SCR has more than 10 times better ESD protection level per unit area. The capacitor used in the RC delay circuit of the power-rail ESD clamp circuit is usually implemented with a MOSFET for the purpose of saving area, because the MOS gate has the highest capacitance per area ratio in standard CMOS processes.

With the advance of the CMOS technology, the transistors have been shrunk in size, and also the operation voltages have become lower. As the transistors become smaller, the gate oxide becomes thinner. The fact that the gate oxide becomes thinner (around 2 nanometers in 65-nm technologies) impacts seriously in the ESD protection circuits. First, the gate oxide breakdown voltage also becomes smaller, so the protection devices need to be triggered at lower voltages, and also the holding voltages need to be lower to effectively protect it. Second, as the gate oxide reaches the nanometer scale, the gate tunneling effect becomes a serious problem [5]–[7] to increment drastically the leakage current of the circuits. When the MOS transistor used as a capacitor and/or the protection MOSFET are large in area, the power-rail ESD clamp circuit could have considerable leakage current due to the gate tunneling issue. A comparison of this issue among different CMOS technologies is shown in Table I. For example, the gate leakage current on an NMOS (PMOS) transistor in the area of $30\mu m \times 25\mu m$ under 1 Volt bias is $55\mu$A ($13\mu$A) in a 65-nm CMOS technology. The big discrepancy between the leakages in the NMOS and PMOS transistors makes the latter to be the better option for implementing the capacitor.

TABLE I: Gate leakage current on MOS capacitors

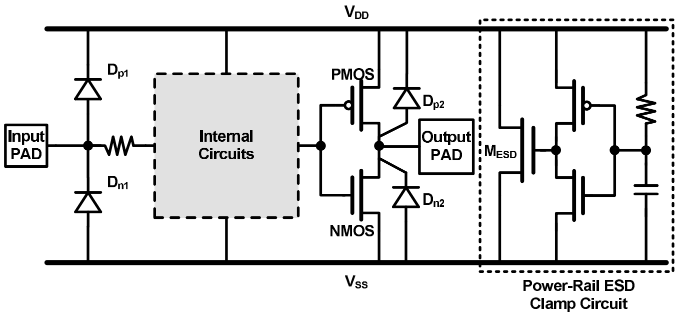
| Generation | MOS Type | $t_{ox}$ | Gate leakage current at 1V (W/L = $1\mu m/1\mu m$) |
|---|---|---|---|
| 90-nm | NMOS | ~2.3nm | ~11nA |
| | PMOS | ~2.5nm | ~3nA |
| 65-nm | NMOS | ~2.0nm | ~140nA |
| | PMOS | ~2.2nm | ~80nA |
| 45-nm | NMOS | ~1.9nm | ~260nA |
| | PMOS | ~2.1nm | ~95nA |

In this work, different circuit techniques are explained and compared with the consideration of leakage current at the operating voltage, ESD protection level, and layout area.

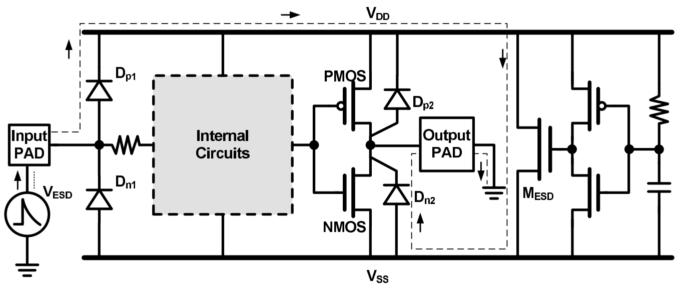
## II. Impact of Gate Current in Power-Rail ESD Clamp Circuits

A diagram of a power-rail ESD clamp circuit is shown in Fig. 2a. The circuit is comprised by an RC delay circuit formed by the resistor $R$ and the PMOS transistor $M_{CAP}$, a trigger circuit formed by the transistors $M_p$ and $M_n$, and an SCR as ESD clamp. The transistor $M_p$ is large-sized to support the SCR trigger current.

When a positive ESD pulse is zapping at the node $V_{DD}$ with $V_{SS}$ grounded, the initial value of $V_{rc}$ is kept at ~0V. Then, the node $V_{rc}$ is charged up through the resistor $R$ with the

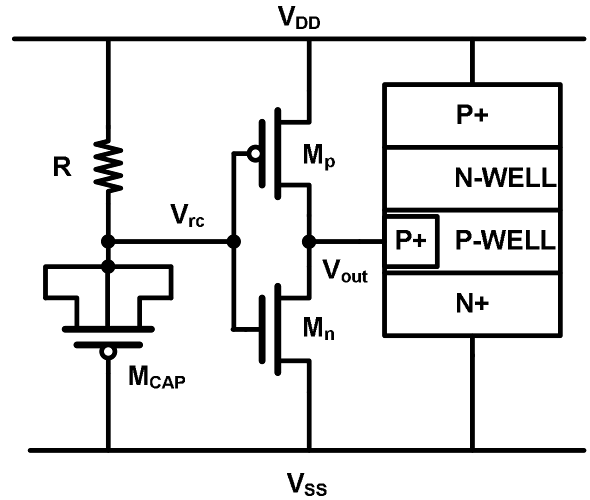



(a)

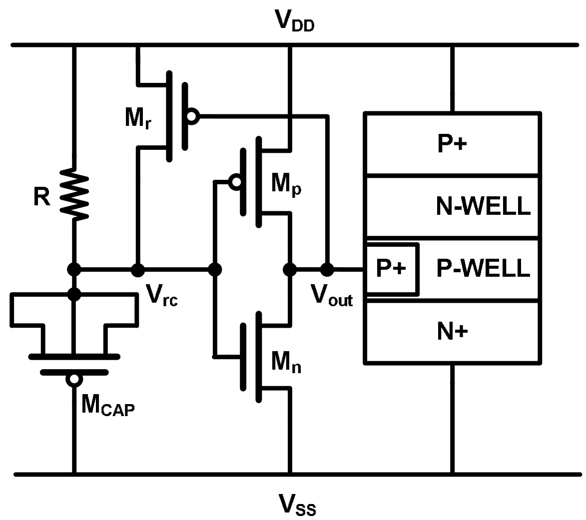



(b)

Fig. 1: (a) Typical whole-chip ESD protection scheme designed with the power-rail ESD clamp circuit, and (b) ESD current path during a typical pin-to-pin ESD event.




(a)




(b)

Fig. 2: (a) Traditional RC-based power-rail ESD clamp circuit, and (b) Modified power-rail ESD clamp circuit with a level restorer.

time constant RC (in the order of microseconds). As the node $V_{rc}$ remains low, the transistor $M_p$ is turned on and drives the triggering current to the SCR, causing the SCR to turn on and therefore to protect the internal circuits.

Under normal circuit operation with $V_{DD}$/$V_{SS}$ power supplies, the capacitor $M_{CAP}$ presents a high impedance, so the voltage at the node $V_{rc}$ is kept at $V_{DD}$. Therefore, the transistor $M_p$ is turned off, and the SCR trigger point is tied to $V_{SS}$, maintaining the SCR in off state. The RC time constant of the capacitor $M_{CAP}$ and resistor $R$ is relatively fast enough (in the order of $\mu$s), so the RC delay stage can follow the $V_{DD}$ voltage transient waveform and there are no misstriggers during the power-on ramp transition with a slow rise time (usually 100$\mu$s to 1ms). However, in advanced CMOS technologies, there is a gate leakage current through the capacitor ($M_{CAP}$), which induces a voltage drop across the resistance $R$. Therefore, the voltage at the node $V_{rc}$ is lower than $V_{DD}$. As the node $V_{rc}$ is connected to the gate of the transistor $M_p$, $M_p$ is not fully turned off. There is another leakage path through the channels of the transistors $M_p$ and $M_n$, which increases the total leakage current in the power-rail ESD clamp circuit. According to SPICE simulation, the leakage current of the traditional power-rail ESD clamp circuit (with $M_{CAP}$ in the area of $20\mu m \times 20\mu m$) under 1 Volt bias is 21.6$\mu$A, using the BSIM4 HSPICE parameters in a 65-nm CMOS process, in which the gate current is considered and modeled [8]. Also, if the protection device used is an NMOS transistor, as the node $V_{out}$ is not fully biased to $V_{SS}$, the transistor would not be fully turned off, and therefore there is another leakage path through the transistor channel.

A modification design of the power-rail ESD clamp circuit, depicted in Fig. 2b, consists of adding a level restorer ($M_r$) in the node $V_{rc}$. This transistor ties the voltage at the node $V_{rc}$ to $V_{DD}$. Therefore, the transistor $M_p$ can be fully turned off and there is no leakage current through $M_p$. The node $V_{out}$ is fully tied to $V_{SS}$, so there is no leakage through the protection device. As the node $V_{rc}$ is kept at $V_{DD}$, the voltage drop across $M_{CAP}$ provokes a current to flow. Therefore, even though the leakage is reduced, the leakage due to the gate tunneling is still high (13$\mu$A in the simulation with $M_{CAP}$ in the area of $20\mu m \times 20\mu m$ in a 65-nm CMOS process).

## III. Power-Rail ESD Clamp Circuits With Consideration of The Gate Current

The gate current can affect the performance of the power-rail ESD clamp circuits drastically, as discussed above. Some recent works have reported the reduction in the gate current by changing the device structure, by using metal instead of silicon for the gate [9], or AlGaN in channel [10], [11], but such process techniques will be used in the 32-nm node and below in IC industry. So the gate current is still an important issue in 90-nm, 65-nm, and 45-nm technologies. To overcome this issue, several circuit techniques have been reported, which are reviewed in the following.

### A. Using MOM Capacitor To Reduce Leakage

As mentioned before, the capacitor used for the RC time delay in the traditional ESD clamp circuit is usually implemented with a MOSFET due to area concern. But, recent work [12] reported that metal-over-metal (MOM) capacitors can be used without significant area overhead.

MOM capacitors have been used in IC design mostly due to their high linearity, quality factor, and small temperature variation [13]. The main issue with MOM capacitor is area overhead. As the oxide thickness between metal layers is larger than that between poly gate and silicon, the capacitance-per-area ratio of MOM capacitor is much lower than that of MOS capacitor. However, as the CMOS technologies keep shrinking, the separation between metal layers decreases, increasing the capacitance density of MOM capacitor. Therefore, this structure can replace the leaky MOS capacitor in the power-rail ESD clamp circuit, because the MOM capacitor does not suffer from gate tunneling current. Fig. 3 shows the power-rail ESD clamp circuit with the MOM capacitor. This circuit is similar to the circuit presented in Fig. 2a, whereas the leaky MOS capacitor has been replaced by the non-leaky MOM capacitor.

This circuit has been fabricated in a 65-nm CMOS technology. The measured leakage current was 358nA under an operating voltage of 1V, and the ESD level is 4kV HBM and 350V MM, with the SCR drawn in a size of $40\mu m \times 7.8\mu m$.

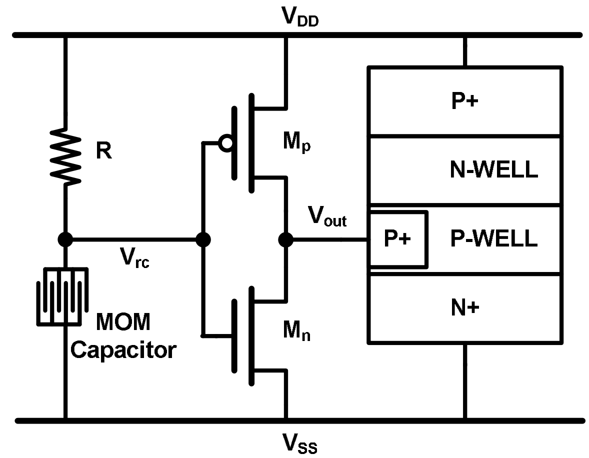



Fig. 3: Schematic diagram of the power-rail ESD clamp circuit reported in [12] with MOM capacitor.

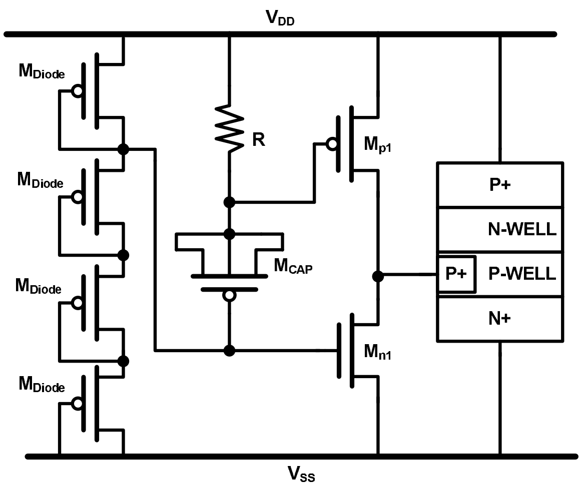



Fig. 4: Schematic diagram of the power-rail ESD clamp circuit reported in [14].

### B. Using Stacked Transistors To Reduce Leakage

A series of stacked diode-connected transistors was used to reduce the voltage across the capacitor under normal circuit operation, therefore reducing the total leakage current [14]. The circuit reported in Fig. 4 consists of a series of stacked diode-connected PMOS transistors, an RC circuit, and the SCR clamp with the driver stage (formed by the transistors $M_{p1}$ and $M_{n1}$). The main difference between the circuits is that the gate plate of the MOS capacitor is not connected to $V_{SS}$ but instead is biased by the diode-connected transistors. The voltage drop across the transistor $M_{CAP}$ under normal circuit operation with $V_{DD}$/$V_{SS}$ power supplies is reduced, and therefore the gate leakage is reduced. The leakage current through the diode-connected transistors is reduced by increasing the number of stacked transistors, and their respective channel length. During ESD stress, due to the RC delay, the transistor $M_{p1}$ gate is initially kept at ~0V, so the transistor is turned on and starts to send the trigger current to the SCR. The RC time constant is designed so that the transistor $M_{p1}$ is turned on during the duration of ESD stress.

This circuit has been fabricated in a 65-nm CMOS technology. The measured leakage current was 228nA under an operating voltage of 1V, and the ESD level is 8kV HBM and 750V MM, with the SCR drawn in a size of $60\mu m \times 7.8\mu m$.

### C. Using Circuit Design To Reduce Leakage

A couple of transistors was used to actively drive the gate node of the MOS capacitor to decrease the voltage drop across the MOS capacitor under normal circuit operation, as shown in Fig. 5 [4]. The reported circuit uses the transistors $M_{p3}$ and $M_{n2}$ to control the voltage at the node $V_B$, allowing it to be tied to either $V_{DD}$ or $V_{SS}$. During normal circuit operation with $V_{DD}$/$V_{SS}$ power supplies, $V_B$ is tied to $V_{DD}$, so there is no voltage drop across the transistor $M_{CAP}$ to eliminate the gate leakage. Under ESD stress, $V_B$ is tied to $V_{SS}$, so the transistors $M_{p1}$ and $M_{p2}$ are turned on to trigger the SCR on.

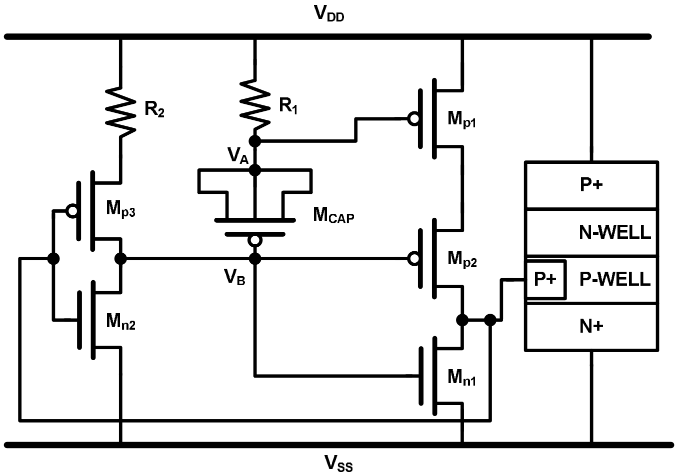



Fig. 5: Schematic diagram of the power-rail ESD clamp circuit reported in [4].

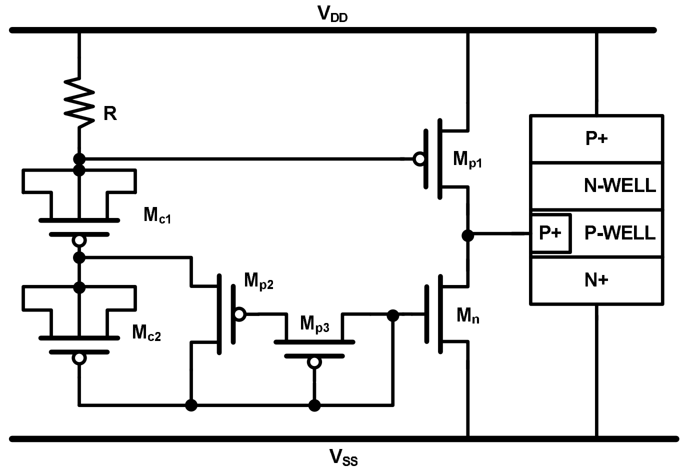



Fig. 6: Schematic diagram of the power-rail ESD clamp circuit reported in [15].

During power-on transition, the node $V_{DD}$ raises to the operating voltage with a slope in the order of milliseconds. The RC time constant is designed in the order of microseconds, so the circuit can never be triggered by a power-on transition. With such a slow rise time, the nodes $V_A$ and $V_B$ follow the $V_{DD}$ voltage in time to keep the transistors $M_{p1}$ and $M_{p2}$ in off state. Through the feedback path, the transistors $M_{p3}$ and $M_{n2}$ are kept on and off, respectively, so the node $V_B$ is tied to $V_{DD}$ by the transistor $M_{p3}$.

When a positive ESD pulse zaps to $V_{DD}$ ($V_{SS}$ grounded) with a fast rise time, the voltages of the nodes $V_A$ and $V_B$ are initially kept at ∼0V. Therefore, the transistors $M_{p1}$ and $M_{p2}$ are initially turned on, so they start to send the trigger current to the SCR. Moreover, the transistor $M_{n2}$ is turned on by the feedback path, tying the node $V_B$ to $V_{SS}$. Therefore, the node $V_A$ starts charging up by the RC time constant. The turned-on SCR provides a low impedance path to safely discharge the ESD current.

This work has been realized in a 65-nm CMOS technology. The measured leakage current was 116nA under an operating voltage of 1V, and the ESD level is 8kV HBM and 800V MM, with the SCR drawn in a size of $60\mu m \times 7.8\mu m$.

### *D. Using Stacked Capacitors To Reduce Leakage*

The work reported in [15] uses stacked capacitors to reduce the total leakage current, as shown in Fig. 6. The transistor $M_{p1}$ is used to generate the SCR trigger current under ESD stress. The transistor $M_n$ is turned on under normal circuit operation to tie the SCR trigger node to $V_{SS}$, therefore guarantying the SCR is kept in off state during normal circuit operation. The RC time constant from $R$, $M_{c1}$, $M_{c2}$, and $M_n$ is designed in the order of microseconds to distinguish ESD events from normal power-on transitions. The transistors $M_{p2}$ and $M_{p3}$ act as start-up circuit to conduct some gate current through the transistor $M_{c1}$ to bias the internal nodes.

Under normal circuit operation with $V_{DD}$/$V_{SS}$ power supplies, the gate voltage of the transistor $M_{p1}$ is biased at $V_{DD}$ through the resistor $R$, so $M_{p1}$ is kept off to avoid possible SCR misstriggers. Moreover, the gate of the transistor $M_n$ is biased at a low voltage (around 0.45V). This voltage is higher than the transistor threshold voltage to assure the transistor $M_{n1}$ is turned on to keep the SCR trigger node at $V_{SS}$.

When a positive ESD zaps at $V_{DD}$ with $V_{SS}$ grounded, the RC delay in the ESD detection circuit keeps the transistor $M_{p1}$ gate at low voltage, thus turning the transistor on and driving the trigger current into the SCR trigger point, so the SCR can be turned on in time to discharge the ESD current safely.

This work has been realized in a 65-nm CMOS technology. It was reported to have a leakage current of 96nA under an operating voltage of 1V, and the ESD level is 7kV HBM and 325V MM, with the SCR drawn in a size of $45\mu m \times 7.8\mu m$.

## IV. Discussion

All these circuit techniques can reduce the leakage current of the power-rail ESD clamp circuits from $21\mu$A to as low as 96nA (under 1V bias), while the ESD robustness is not reduced. A comparison among the performance of the reviewed circuits is shown in Table II.

The different SCR sizes used in the power-rail ESD clamp circuits impact directly on the ESD level. Layout optimization is also important, as a careful layout design will lead to a higher ESD robustness. It can be seen in Table II that the SCR used in the circuits of Fig. 3 and Fig. 6 are similar in size, but their ESD levels are different. The circuits from Fig. 4 and Fig. 5 are examples of careful layout design. Using an SCR of size 50% higher than the other circuits, these power-rail ESD clamp circuits double the ESD levels in both of the HBM and MM ESD tests.

In addition, one new circuit designed without using the capacitor in the ESD detection circuit has been reported recently [16]. Such a new capacitor-less design can also significantly reduce the leakage current in the power-rail ESD clamp circuit.

TABLE II: Comparison among the power-rail ESD clamp circuits

| Circuit | ESD Level | | Leakage Current at $V_{DD} = 1V$ | SCR size | CMOS technology |
|---|---|---|---|---|---|
| | MM | HBM | | | |
| Circuit of Fig. 2a | — | — | 21$\mu$A (sim.) | — | 65-nm |
| Circuit of Fig. 2b | — | — | 12$\mu$A (sim.) | — | 65-nm |
| Circuit of Fig. 3 | 350V | 4kV | 358nA | $40\mu m \times 7.8\mu m$ | 65-nm |
| Circuit of Fig. 4 | 750V | >8kV | 228nA | $60\mu m \times 7.8\mu m$ | 65-nm |
| Circuit of Fig. 5 | >800V | >8kV | 116nA | $60\mu m \times 7.8\mu m$ | 65-nm |
| Circuit of Fig. 6 | 325V | 7kV | 96nA | $45\mu m \times 7.8\mu m$ | 65-nm |

## V. Conclusion

The gate tunneling effect impacts drastically in the leakage current of the traditional power-rail ESD clamp circuit in nanoscale CMOS technologies. The leakage current of the traditional power-rail ESD clamp circuit could scale up to several hundred microamperes in 65-nm CMOS technology. The addition of a level restorer helps to reduce the leakage, but it is still in the microamperes order.

The circuit techniques reviewed in this work can successfully reduce the leakage current of the power-rail ESD clamp circuit to the nanoamperes order, without significant area overhead, and without decreasing the ESD robustness. The first presented circuit uses a MOM capacitor to avoid the gate tunneling current, so the leakage is only caused by the SCR driving transistors. The second circuit uses stacked transistors to reduce the MOS capacitor voltage, so the leakage current through the MOS capacitor, which is highly dependent of the applied voltage, is reduced. The third circuit controls the MOS capacitor gate node to eliminate the voltage drop among the resistor and capacitor, thus eliminating the MOS capacitor leakage current. The fourth circuit uses stacked capacitors to reduce the leakage current.

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