Modified LC-Tank ESD Protection Design for 60-GHz RF Applications

Chun-Yu Lin[1], Li-Wei Chu[1], Shiang-Yu Tsai[1], Ming-Dou Ker[1], Tse-Hua Lu[2], Tsun-Lai Hsu[2], Ping-Fang Hung[2], Ming-Hsiang Song[2], Jen-Chou Tseng[2], Tzu-Heng Chang[2], and Ming-Hsien Tsai[2]

[1] National Chiao-Tung University, Hsinchu, Taiwan
[2] Taiwan Semiconductor Manufacturing Company

***Abstract* — Nanoscale CMOS technologies, which were sensitive to electrostatic discharge (ESD), have been widely used to implement radio-frequency (RF) integrated circuits. Against ESD damages, ESD protection design must be included in RF circuits. A novel modified LC-tank ESD protection design was presented in this work. Such ESD protection circuit had been designed for 60-GHz RF applications and verified in a 65-nm CMOS process. The modified LC-tank can lower the power loss and reduce the layout area under the required human-body-model (HBM) ESD robustness, as compared with the traditional designs. With the better performances, the modified LC-tank ESD protection design was very suitable for RF ESD protection.**

***Index Terms* — Electrostatic discharge (ESD), LC-tank, radio frequency (RF).**

I. Introduction

RF integrated circuits have been widely designed and fabricated in CMOS processes due to the advantages of high integration and low cost for mass production. Electrostatic discharge (ESD) must be taken into consideration during the design phase of all ICs, including the RF circuits. In the RF circuits, the input/output (I/O) pads are usually connected to the gate terminal or silicided drain/source terminal of the metal-oxide-semiconductor field-effect transistor (MOSFET), which leads to a very low ESD robustness if no appropriate ESD protection design is applied. Once the RF front-end circuit is damaged by ESD, it can not be recovered and the RF functionality is lost. Therefore, on-chip ESD protection design must be provided for all I/O pads in RF ICs.

However, ESD protection devices cause RF performance degradation with several undesired effects [1], [2]. Conventional ESD protection devices with large dimensions have the parasitic capacitance which is too large to be tolerated for RF front-end circuits. As shown in Fig. 1, the parasitic capacitances of ESD protection devices cause power loss from the pads to ground. Moreover, the parasitic capacitance also changes the input matching condition. Consequently, RF performance is deteriorated.

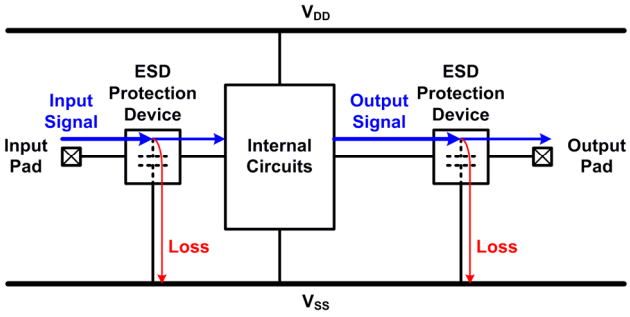

Fig. 1. Power loss at input and output pads of RF ICs with ESD protection devices.

To mitigate the performance degradation caused by ESD protection devices, the LC-tank ESD protection design has been developed to block the parasitic effects of ESD protection devices from the RF circuits [3], [4]. The ESD protection circuit with reduced parasitic effects can be easily combined or co-designed with RF circuits. However, the transient voltage across the traditional LC-tank ESD protection circuit must be reduced to improve ESD robustness of the RF circuits, especially for the circuits realized in nanoscale CMOS technology. Therefore, a new modified LC-Tank ESD protection design is proposed in this paper. Such ESD protection circuit has been designed for 60-GHz RF applications and verified in a 65-nm CMOS process.

II. Design Consideration for ESD Protection

To achieve effective ESD protection, the voltage across the ESD protection device during ESD stress conditions should be carefully designed [5]. Fig. 2 shows the ESD design window of an IC, which is defined by the power-supply voltage (V_{DD}) of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage (V_{BD}) of MOSFET. The turn-on resistance (R_{on}) of ESD protection device should be minimized to reduce the joule heat generated in the ESD protection device and the clamping voltage of the ESD protection device during

ESD stresses. As CMOS technology is continuously scaled down, the power-supply voltage is decreased and the gate oxide becomes thinner, which leads to the reduced gate-oxide breakdown voltage of MOSFET. Typically, the gate-oxide breakdown voltage is decreased to only ~5 V in a 65-nm CMOS process with gate-oxide thickness of ~20 Å [6]. As a result, the ESD design window becomes much narrower in nanoscale CMOS technologies. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharging paths in time.

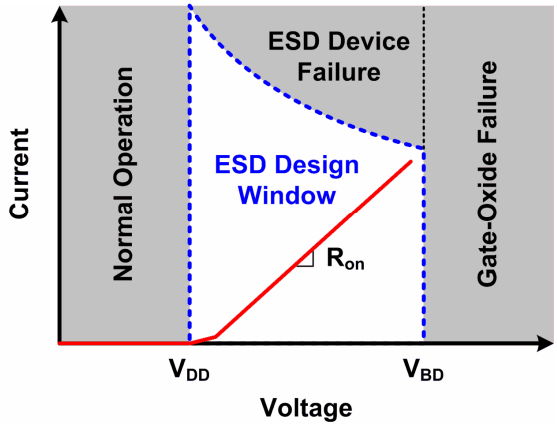

Fig. 2. ESD design window.

III. Traditional LC-Tank ESD Protection Design

LC-tank has been reported for RF ESD protection design, which consists of an inductor, a capacitor, and an ESD diode. As shown in Fig. 3, a pair of the LC-tanks is placed at the I/O pad. One LC-tank consists of the inductor L_P, capacitor C_P, and ESD diode D_P, is placed between the I/O pad and V_{DD}. Another LC-tank consists of the inductor L_N, capacitor C_N, and ESD diode D_N, is placed between the I/O pad and V_{SS}. The LC-tanks are designed to resonate for "open circuit" at the operating frequency of the RF circuit. Thus, the parasitic effects of ESD diodes (D_P and D_N) will be isolated. On the other hand, the ESD diodes (D_P and D_N) can block the steady leakage current path from I/O to V_{DD} or V_{SS} under normal circuit operating conditions. Under ESD stress conditions, the ESD current path of I/O-to-V_{DD} (V_{SS}-to-I/O) consists of L_P and D_P (D_N and L_N).

The simulated S_{11}- and S_{21}-parameters of the traditional LC-tank ESD protection are shown in Fig. 4, where the operating frequency is designed to 60 GHz. At 60 GHz, there is ideally infinite impedance from the signal path to ground. Consequently, the parasitic effects of ESD diodes are isolated, which can mitigate the RF performance degradation caused by the ESD protection devices.

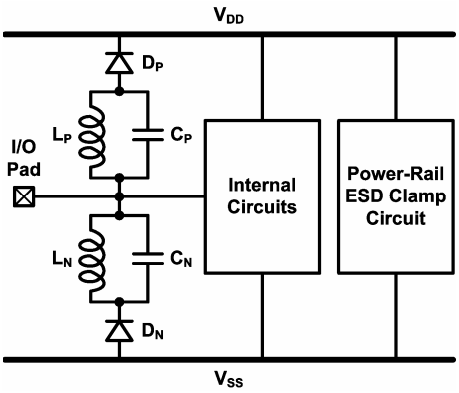

Fig. 3. Traditional LC-tank ESD protection design in RF circuits.

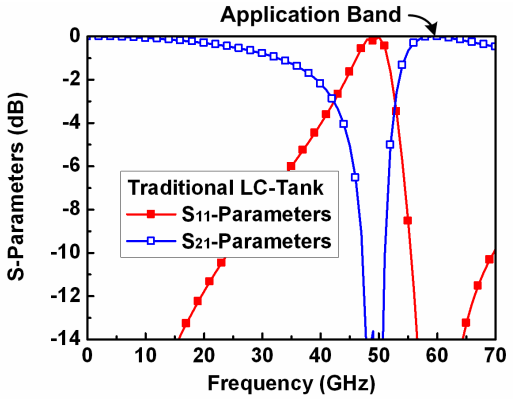

Fig. 4. Simulated S-parameters of traditional LC-tank ESD protection design in Fig. 3.

IV. Modified LC-Tank ESD Protection Design

A. Circuit Design

Fig. 5(a) shows the circuit design of modified LC-tank ESD protection, where a pair of the modified LC-tanks is placed at the I/O pad. The series LC (L_P-C_P and L_N-C_N) are designed to resonate at low frequency. At the frequency above the resonant frequency, the inductances dominate the impedances of the series LC, and then the inductances can eliminate the parasitic capacitances of ESD diodes (D_P and D_N). Besides, the inductors in series with the capacitors can block the leakage path from I/O to V_{DD} or V_{SS} under normal circuit operating conditions. Under ESD stress conditions, the ESD current path of I/O-to-V_{DD} (V_{SS}-to-I/O) consists of only one ESD diode D_P (D_N). Therefore, the turn-on resistance (R_{on}) of the modified LC-tank ESD protection design can be reduced to improve the ESD robustness, as compared with that of the traditional LC-tank ESD protection design.

To reduce the inductor used in the modified LC-tank ESD protection, another design using only one inductor is

shown in Fig. 5(b). The inductor used in Fig. 5(b) is smaller than that used in Fig. 5(a), since the smaller inductance can resonate with the larger parasitic capacitance from two ESD diodes. To further reduce the inductance in modified LC-tank, another capacitor C_C can be added besides the ESD diodes. The simulated S-parameters of the modified LC-tank are shown in Fig. 6.

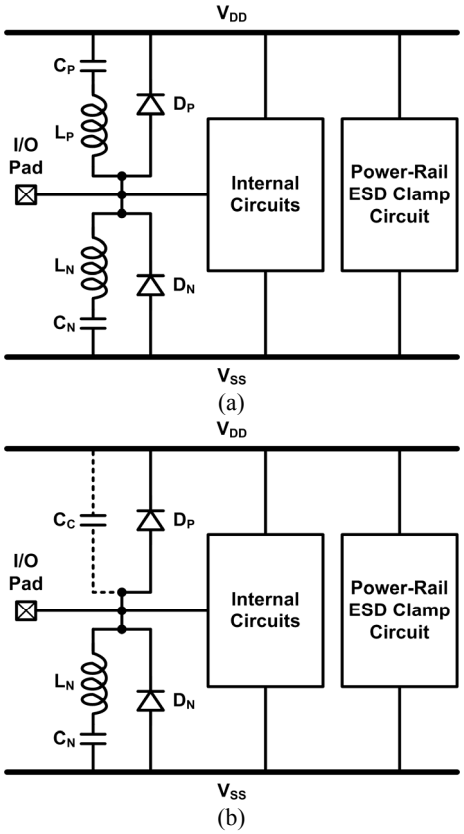

Fig. 5. Modified LC-tank ESD protection design in RF circuits with (a) a pair of inductors and (b) only one inductor.

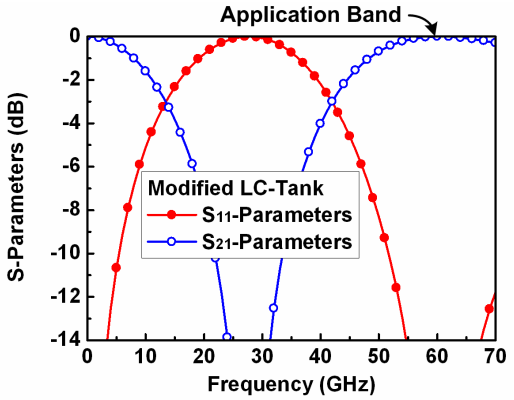

Fig. 6. Simulated S-parameters of modified LC-tank ESD protection design in Fig. 5(b).

B. Measurement Results

The traditional LC-tank and modified LC-tank ESD protection designs have been fabricated in a 65-nm CMOS process. Table I summarizes the device parameters of the test circuits. The ESD robustness of the fabricated ESD test circuits with the RF-NMOS emulators [7] are evaluated by the ESD tester in human-body model (HBM). The positive-to-V_{DD} (PD-mode), positive-to-V_{SS} (PS-mode), negative-to-V_{DD} (ND-mode), and negative-to-V_{SS} (NS-mode) ESD robustness of all ESD test circuits are tested. The measured HBM ESD levels of all ESD test circuits are listed in Table II. Besides, the S-parameters of these ESD test circuits have been measured around 60 GHz. The voltage supply of V_{DD} (V_{SS}) is 1 V (0 V), and the input dc bias is 0.5 V. Fig. 7 shows the measured S_{21}-parameters of modified LC-tank ESD protection design. The measured S-parameters at 60 GHz of all ESD test circuits are also listed in Table II. The traditional LC-tank ESD protection circuit with 1.5-kV HBM ESD robustness exhibits 3.1-dB power loss. The modified LC-tank ESD

TABLE I
DEVICE PARAMETERS OF ESD PROTECTION DESIGNS

	Traditional LC-Tank ESD Protection	Modified LC-Tank ESD Protection			
		M1	M2	M3	M4
L_P	0.08 nH	N/A	N/A	N/A	N/A
C_P	90 fF	N/A	N/A	N/A	N/A
D_P	30 μm (36 fF)	8 μm (9 fF)	15 μm (18 fF)	23 μm (27 fF)	30 μm (36 fF)
L_N	0.08 nH	0.11 nH	0.11 nH	0.11 nH	0.11 nH
C_N	90 fF	300 fF	300 fF	300 fF	300 fF
D_N	30 μm (44 fF)	8 μm (12 fF)	15 μm (22 fF)	23 μm (34 fF)	30 μm (44 fF)
C_C	N/A	60 fF	40 fF	20 fF	N/A

TABLE II
COMPARISON ON EXPERIMENTAL RESULTS AMONG ESD PROTECTION DESIGNS IN SILICON

	Traditional LC-Tank ESD Protection	Modified LC-Tank ESD Protection				Distributed ESD Protection [7]			
		M1	M2	M3	M4	D1	D2	D3	D4
S_{11}-Parameters at 60 GHz	-12 dB	-16 dB	-17 dB	-19 dB	-21 dB	-18 dB	-25 dB	-27 dB	-22 dB
S_{21}-Parameters at 60 GHz	-3.1 dB	-1.3 dB	-1.4 dB	-1.6 dB	-1.8 dB	- 0.9 dB	- 1.1 dB	- 1.9 dB	- 2.1 dB
HBM ESD Robustness*	1.5 kV	0.25 kV	1.25 kV	1.75 kV	2 kV	0.75 kV	1.5 kV	2.25 kV	2.5 kV
Layout Area (Without Pad)	160x100 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	130x150 μm^2	130x150 μm^2	110x220 μm^2	110x220 μm^2

* Obtained from the lowest level of PD-, PS, ND, and NS-mode ESD robustness.

protection circuits with 0.25-, 1.25-, 1.75-, and 2-kV HBM ESD robustness exhibit 1.3-, 1.4-, 1.6-, and 1.8-dB power loss, respectively.

The measured S-parameters, HBM ESD robustness, and the layout area of the traditional LC-tank, modified LC-tank, and distributed ESD protection designs [7] are compared in Table II. Among these ESD protection designs, the modified LC-tank can achieve the required 2-kV HBM ESD robustness with the lower power loss and smaller layout area.

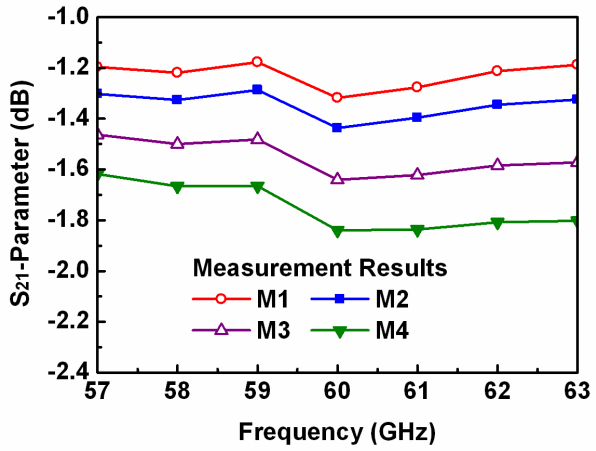

Fig. 7. Measured S_{21}-parameters of modified LC-tank ESD protection design.

V. CONCLUSION

The proposed modified LC-tank ESD protection design for 60-GHz RF applications has been successfully verified in a 65-nm CMOS process. As compared with the traditional designs, the modified LC-tank ESD protection design has been demonstrated to achieve the required 2-kV HBM ESD robustness with the lower power loss and smaller layout area. Thus, the proposed modified LC-tank ESD protection design is very suitable for RF ESD protection.

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