ESD-Aware Circuit Design in CMOS Integrated Circuits to Meet System-Level ESD Specification in Microelectronic Systems

Ming-Dou Ker[1, 2], *Fellow, IEEE*
[1] Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
[2] Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan.

***Abstract* -- Circuit solution for system-level electrostatic discharge (ESD) protection is presented in this invited talk. To prevent the microelectronic system frozen at the malfunction or upset states after system-level ESD test, on-chip ESD-aware circuit in CMOS ICs should be built to rescue itself from the unknown states for returning normal system operation. A novel concept of transient-to-digital converter is innovatively provided to detect the fast electrical transients during the system-level ESD events. The output digital thermometer codes of the transient-to-digital converter can correspond to the different ESD voltages during system-level ESD tests. The proposed solution has been applied in some display panels to automatically recover the system operations after system-level ESD test.**

I. Introduction

The reliability issue of system-level electrostatic discharge (ESD) events has attracted more attentions in the IC Industry. The microelectronic product must sustain the ESD level of ±8kV (±15kV) under contact-discharge (air-discharge) test mode to achieve the specification of "level 4" in the IEC 61000-4-2 test standard [1]. Such ESD-induced transient noises often caused hardware damage and/or malfunction to CMOS ICs inside the microelectronic system under test.

In order to solve such system-level ESD issues, the traditional solution is to add some board-level discrete components or board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transients under system-level ESD tests [2], [3]. By the way, the transient voltage suppressor (TVS) arranged in array style were fabricated by some special processes to efficiently protect the CMOS ICs against system-level ESD test, especially, for the high-speed I/O applications (such as USB 3.0 and HDMI 1.4) [4], [5].

II. ESD-Aware Circuit Design and Applications

A. Transient-to-Digital Converter

The transient-to-digital converter consisted of four transient detection circuits with four different RC filter networks is shown in Fig. 1 [6]. The RC filter network is realized with one decoupling capacitor and two resistors with equal value to provide the noise filter function during system-level ESD stresses. The RC noise filter network can suppress the transient peak voltages on V_{DD} and V_{SS}, which has influence on positive and negative system-level ESD voltages to cause transition at the output (V_{OUT}) node of the on-chip transient detection circuit. As the transient-to-digital converter with different R and C values in the filter networks, different ESD levels on V_{DD} and V_{SS} will reach to each transient detection circuit. During system-level ESD zapping, the four transient detection circuits will have different output voltage responses. Therefore, by combining with different RC noise filter networks, the transient-to-digital converter can be designed to detect different ESD voltage levels and transfer the output voltages into digital thermometer codes during system-level ESD stress.

B. Experimental Verification

The transient-to-digital converter has been designed and fabricated in a 0.18-μm CMOS process with 3.3-V devices. The fabricated chip photo for system-level ESD test is shown in Fig. 2. The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the transient-to-digital converter under system-level ESD test with the ESD zapping voltage of +0.8kV [+3.1kV] are shown in Fig. 3(a) [Fig. 3(b)]. During the high-energy fast transient of ESD stress, the transient detection circuits can detect the occurrence of disturbance on V_{DD}/V_{SS}. After system-level ESD test with the ESD zapping voltage of +0.8kV [+3.1kV], the output nodes can be transferred into a digital thermometer code of "0001" ["1111"].

C. Application in Display Panel

The hardware/firmware co-design with the transient detection circuit can effectively improve the robustness of the microelectronic products against electrical transient disturbance. Under system-level ESD zapping, the measured results on a TFT-LCD display panel without and with hardware/firmware system co-design are shown in Figs. 4(a) and 4(b), respectively. After system-level ESD zapping, the display panel products would be easily locked in some frozen / unknown states and the correct RGB data cannot be displayed continually, as shown in Fig. 4(a). By applying the output codes of the transient-to-digital converter as the firmware index, the display panel can automatically recover all electrical functions to successfully release the frozen states caused by system-level ESD transient disturbance. Therefore, it can display the picture on panel correctly after system-level ESD stress, as that shown in Fig. 4(b).

III. Conclusion

The ESD-aware concept realized with the transient-to-

978-1-4577-1997-4/11/$26.00 ©2011 IEEE

digital converter to automatically recover the normal system operation after system-level ESD test has been successfully verified. The output digital thermometer codes of the transient-to-digital converter can correspond to different ESD voltages under system-level ESD tests. These output digital thermometer codes can be used as the firmware index to execute different system recovery procedures of microelectronic products. The transient-to-digital converter is an effective on-chip circuit solution to solve the system-level ESD reliability issue in microelectronic systems equipped with CMOS ICs.

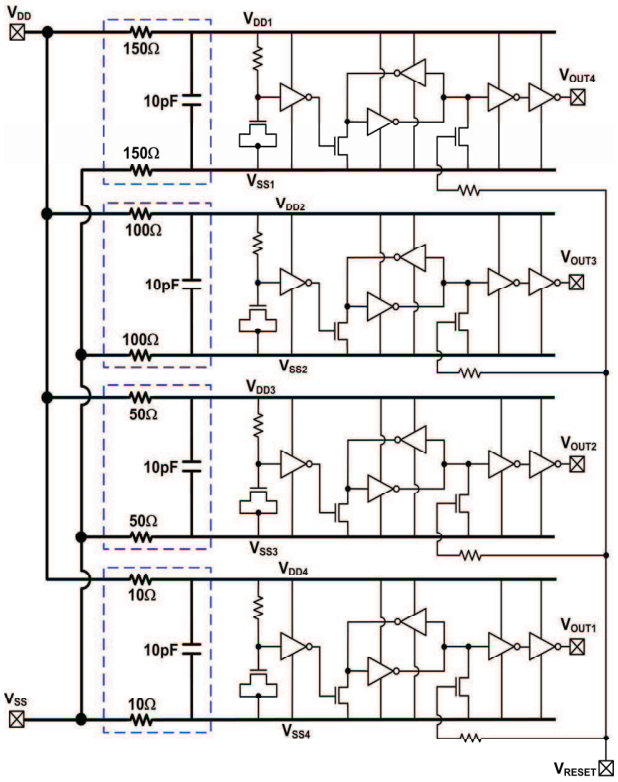

Fig. 1. The 4-bit transient-to-digital converter realized with four transient detection circuits and four RC filter networks.

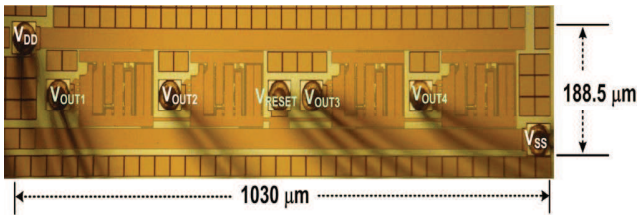

Fig. 2. Die photos of the whole 4-bit transient-to-digital converter realized with four transient detection circuits and RC filter networks, which has been verified in a 0.18-μm CMOS process.

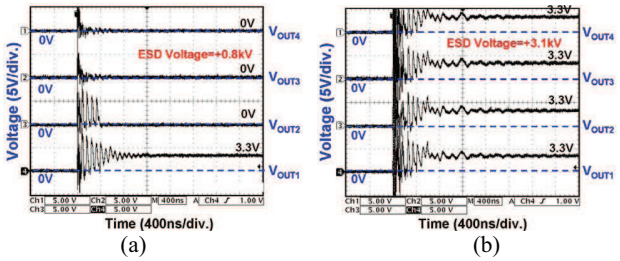

Fig. 3. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms under system-level ESD test with ESD zapping voltage of (a) +0.8kV and (b) +3.1kV.

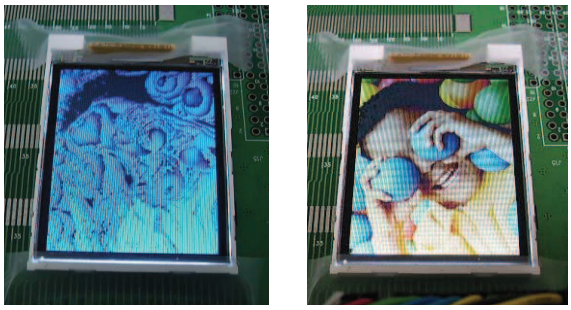

Fig. 4. Measured results on a TFT-LCD display panel (a) without, and (b) with, the transient detection circuit and hardware/firmware system co-design under system-level ESD zapping.

ACKNOWLEDGMENT

This work was partially supported by National Science Council (NSC), Taiwan, under the Contract of NSC 98-2221-E-009-113-MY2; and partially supported by "Aim for Top University Plan" of National Chiao Tung University and Ministry of Education, Taiwan.

REFERENCES

[1] IEC 61000-4-2 Standard, "*EMC – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*," IEC, 2001.

[2] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, Piscataway, NJ: IEEE Press, 2000.

[3] M.-D. Ker and S.-F. Hsu, "Evaulation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. on Electromagnetic Compatibility*, vol. 48, no. 1, pp. 161-171, Feb. 2006.

[4] AZM-LCDL1-10B: 10-line RLC EMI filter with ESD protector in chip scale package, *Datasheet of Amazing Microelectronic Corp.*, Mar. 2010. (online: www.amazingIC.com).

[5] AZ1065-06F: Ultra low capacitance ESD protection array for high speed I/O port, *Datasheet of Amazing Microelectronic Corp.*, Aug. 2010. (online: www.amazingIC.com).

[6] M.-D. Ker and C.-C. Yen, "Transient-to-digital converter for system-level electrostatic discharge protection in CMOS ICs," *IEEE Trans. on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 620-630, Aug. 2009.