

On-chip detection circuit for protection design in display panel against electrical fast transient (EFT) disturbance

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Abstract. A new on-chip detection circuit is proposed for electrical fast transient (EFT) protection design in a display system. For microelectronic products, electrical transient disturbances often cause upset or frozen states under the IEC test standard. The output signal of the proposed detection circuit can be used as a firmware index to execute system automatic recovery operations and to release the EFT-induced locked states in display panels. The circuit function to detect positive or negative electrical transients has been investigated in HSPICE simulation and verified in silicon chip. The experimental results have confirmed successful circuit performance under EFT tests. With hardware/firmware co-design, the immunity of a display system against electrical transient disturbance has been significantly improved.

1. Introduction

Electrical fast transient (EFT) event has become an important reliability issue to display systems equipped with CMOS driver integrated circuits (ICs) [1], [2]. This tendency results from not only the progress of more functions integrated into a single silicon chip but also from the strict requirements of reliability test standards, such as the EFT test. The microelectronic product must sustain the EFT voltage level of ± 2 kV under EFT tests to achieve the immunity requirement of “level 4” in the IEC 61000-4-4 test standard [3]. When some real-world EFT events occurred, the power lines of the CMOS ICs in the microelectronic products no longer maintained normal voltage levels, but an exponential voltage pulse with the amplitude of several tens volts occurred. The waveform of a single EFT pulse has a rise time of about ~ 5 ns and the pulse duration of ~ 50 ns. The CMOS ICs inside the microelectronic products are very susceptible to electrical transient disturbance [4]-[8], even though they have passed the component-level ESD specifications.

In this work, an on-chip detection circuit is designed to detect electrical transient disturbance under EFT tests and verified in a $0.13\text{-}\mu\text{m}$ CMOS process. The proposed circuit can provide a hardware/firmware co-design solution to improve the susceptibility of microelectronic display systems against EFT-induced electrical transient disturbance.

2. On-Chip Detection Circuit

2.1. Circuit Implementation

In this work, an on-chip detection circuit has been proposed, as shown in Fig. 1. The CR-based circuit structure is designed to detect EFT-induced transient disturbance. The NMOS (M_{nr}) is used to set the initial output voltage levels at nodes V_{OUT} and V_A as 1.8 V with the V_{DD} of 1.8 V. During the normal operating condition, the node V_X is biased at 0 V by connecting to the V_{SS} line through a poly resistor. The two-inverter latch is designed to memorize the logic state before and after EFT events. The MOSFET capacitor is a PMOS device and connected between the V_{DD} line and the node V_X to sense transient disturbance coupled to the 1.8-V power line. For the buffer stage, there are three inverters designed in series to drive the 8-pF loading capacitance of the voltage probe at node V_{OUT} . Under the EFT tests with an overshooting transient voltage, the node V_X will be coupled with positive voltage by the MOSFET capacitor coupling. Then, the NMOS device (M_{nt}) will be turned on by the overshooting EFT voltage to pull down the voltage level at the node V_A from 1.8 V to 0 V. Therefore, the logic level stored at the node V_B can be further pulled up from logic “0” to logic “1” to memorize the EFT events. With the buffer inverters, the final output voltage of the proposed detection circuit is changed from logic “1” to logic “0” to detect the occurrence of EFT-induced transient disturbance.

The simulation conditions and measurement setup for the EFT test combined with the attenuation network is shown in Fig. 2. The EFT generator is connected to the V_{DD} line of the device under test (DUT) through -40dB attenuation network. The V_{DD} and V_{OUT} transient responses of the detection circuit are monitored by the digital oscilloscope.

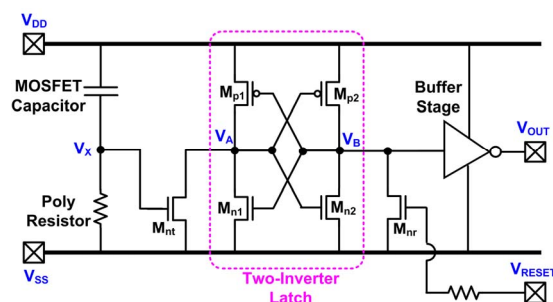


Figure 1. The proposed on-chip detection circuit.

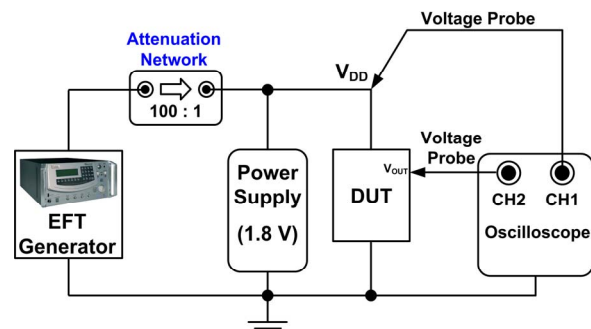


Figure 2. Measurement setup and simulation conditions for EFT test combined with -40dB attenuation network.

2.2. HSPICE Simulation

For HSPICE simulations, with the proper parameters (including the rise time constant τ_1 (=3 ns), fall time constant τ_2 (=25 ns), rise time delay t_{d1} (=200 ns), fall time delay t_{d2} (=210 ns), initial dc voltage value V_1 (=1.8 V), and exponential pulse voltage value V_2), the exponential voltage pulse can be constructed to simulate the EFT-induced disturbance under EFT tests. The rising edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(rise)}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right) \right], \text{ when } t_{d1} \leq t \leq t_{d2}. \quad (1)$$

The falling edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(fall)}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right) \right] + (V_1 - V_2) \times \left[1 - \exp\left(-\frac{t - t_{d2}}{\tau_2}\right) \right], \text{ when } t \geq t_{d2}. \quad (2)$$

The simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip detection circuit with positive and negative exponential pulse transient disturbance on V_{DD} line are shown in Figs. 3(a) and 3(b), respectively. From the simulated waveforms, V_{DD} begins to change rapidly from 1.8 V and acts with positive or negative exponential voltage pulse waveform during the simulated transient disturbance on power line. During EFT zapping conditions, V_{OUT} is disturbed simultaneously during the EFT-induced disturbance in the simulation. After V_{DD} finally returns to its normal voltage level of 1.8 V, V_{OUT} will be changed from 1.8 V to 0 V, as shown in Figs. 3(a) and 3(b). In future works, the variation of transistor parameters should be taken into design considerations.

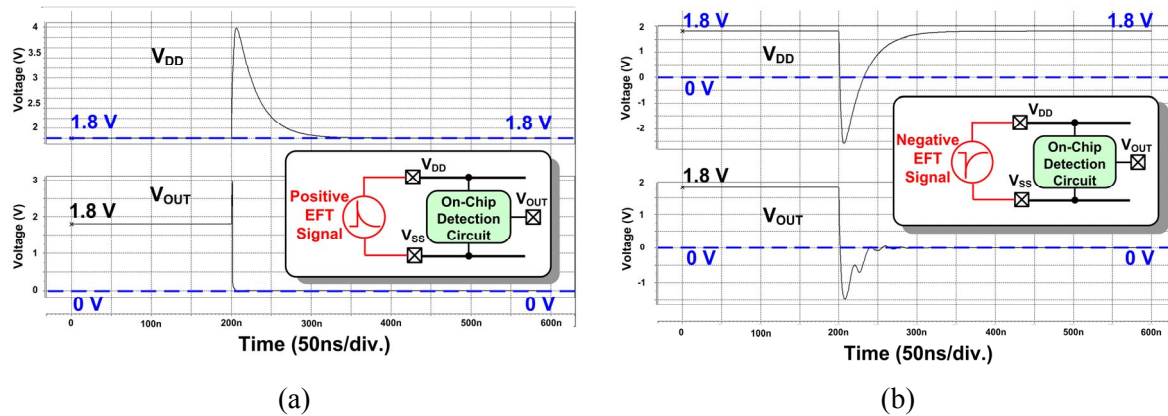


Figure 3. Simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip detection circuit under EFT tests with (a) positive, and (b) negative, exponential voltage pulse waveforms coupled to V_{DD} .

3. Experimental Results

The measured V_{DD} and V_{OUT} waveforms of the on-chip detection circuit under EFT test with EFT voltage of +200 V and -350 V are shown in Fig. 4(a) and 4(b), respectively. As shown in Fig. 4(a) (Fig. 4(b)), under the EFT test with positive (negative) EFT voltage, V_{DD} begins to increase (decrease) rapidly from 1.8 V. Meanwhile, V_{OUT} begins to greatly increase (decrease) with positive (negative) exponential voltage pulse coupled on V_{DD} line. Finally, after the EFT-induced transient disturbance, the final output voltage (V_{OUT}) of the detection circuit is changed the logic “1” to logic “0.”

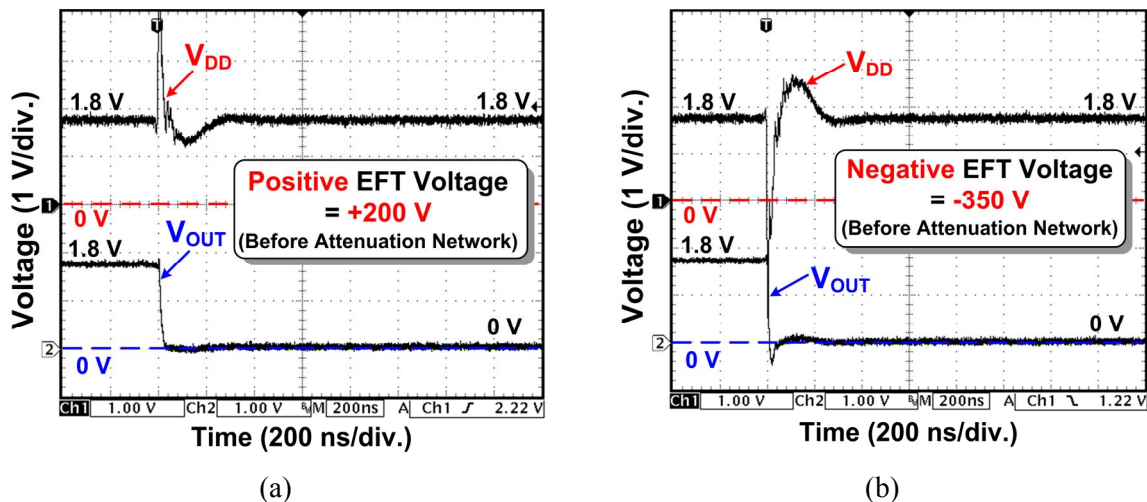


Figure 4. Measured V_{DD} and V_{OUT} waveforms on the proposed on-chip detection circuit under EFT tests with (a) +200-V, and (b) -350-V, EFT voltages combined with attenuation network.

4. Application in Display Systems

The high-voltage electrical fast transients often cause CMOS ICs inside the equipment under test (EUT) to be upset or frozen after the system-level electrical transient disturbance. It has been reported that electrical transient disturbance coupled to power and ground pins of a super twisted nematic (STN) liquid crystal display (LCD) driver circuit can cause abnormal function of the LCD panel. The transient disturbance energy can couple through the indium tin oxide (ITO) film from the LCD panel into the CMOS driver ICs to cause display malfunction.

In this work, the proposed on-chip detection circuit can cooperate with firmware operation to provide hardware/firmware co-design for improving the robustness of the display products against EFT-induced stresses. The detection results can be used as firmware index to execute an automatic recovery procedure when display products are disturbed with EFT events. The detection circuit can connect with the 1.8-V power line to detect and memorize the occurrence of EFT-induced transient disturbances coupled on the digital subsystem of display products. In the beginning, the output (V_{OUT}) state of the detection circuit is set to logic “1” by the power-on procedure. When the electrical transients happen, the output state (V_{OUT}) of the detection circuit will transit from 1.8 V to 0 V. Simultaneously, firmware recovery procedure can be started to restore the display system to a known stable state as soon as possible. After the recovery procedure, the output level of the detection circuit and the firmware index are both re-set to logic “1” again for detecting the next EFT-induced electrical transient disturbance event.

5. Conclusions

An on-chip detection circuit to memorize EFT events has been proposed and successfully verified in a CMOS 0.13- μm process. The circuit performance under different positive and negative EFT-induced transient disturbance has been investigated by HSPICE simulation. The experimental results in silicon chip have confirmed that the proposed detection circuit can successfully detect and memorize the occurrence of fast electrical transients during EFT tests. The proposed detection circuit can be further combined with firmware design to provide an effective solution against the frozen or locked states caused by EFT-induced transient disturbance events in microelectronic display products.

Acknowledgments

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