Design of Low-Leakage Power-Rail ESD Clamp Circuit with MOM Capacitor and STSCR in a 65-nm CMOS Process

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***Abstract* — A power-rail electrostatic discharge (ESD) clamp circuit designed with low-leakage consideration has been proposed and verified in a 65-nm low-voltage CMOS process. By using the metal-oxide-metal (MOM) capacitor in the ESD-detection circuit, the power-rail ESD clamp circuit realized with only thin-oxide (1-V) devices has very low stand-by leakage current, as compared to the traditional design. The experimental results in the silicon chip showed that the stand-by leakage current is only 358 nA at room temperature (25 °C) under the power-supply voltage of 1 V, whereas the traditional design realized with the NMOS capacitor is as high as 828 µA under the same bias condition.**

I. Introduction

In order to protect the internal circuits against electrostatic discharge (ESD) stresses, on-chip ESD protection circuits must be equipped at all I/O and power (V_{DD}/V_{SS}) pads. The typical design of on-chip ESD protection scheme in a CMOS IC is illustrated in Fig. 1. In such ESD protection scheme, the power-rail ESD clamp circuit is very important because it can significantly increase the overall ESD robustness of the IC chips [1]. With the turn-on efficient power-rail ESD clamp circuit between the V_{DD} and V_{SS} power lines, the internal circuits of CMOS ICs can be effectively protected against ESD damages. In the traditional design, the power-rail ESD clamp circuit was often realized with the RC-based ESD-detection circuit and one main ESD clamp device (M_{NESD}), as shown in Fig. 1.

With consideration of area efficiency and fabrication cost, the capacitor (C_1) in the ESD-detection circuit was often realized by the MOS capacitor, because MOS capacitors have the largest capacitance per unit area in the baseline CMOS processes. However, in nanoscale CMOS technology, the gate oxide thickness becomes thinner, which makes the gate-tunneling issue more serious and could not be ignored at all. The gate leakage issue had been studied and the gate-direct-tunneling mechanisms had been modeled for circuit simulation [2], [3]. With the increased gate leakage current in the nanoscale CMOS process, the traditional power-rail ESD clamp circuit with a MOS capacitor in the ESD-detection circuit will cause huge leakage issue in CMOS ICs. Some previous works had addressed this leakage issue with the MOS capacitors in the ESD-detection circuit and provided the modified designs to reduce the overall leakage current [4], [5]. However, the MOS capacitor in ESD-detection circuit always has some leakage current, because there is always a voltage drop across it under the normal circuit operating condition with V_{DD} bias. As the result, additional modified design had been proposed to decrease the leakage current by reducing the voltage drop across the MOS capacitor [6]. But those circuit techniques in the ESD-detection circuit would somehow decrease the trigger ability during the beginning of ESD-stress event. Thus, if the capacitor in the traditional RC-based ESD-detection circuit could be replaced by another capacitor which without the gate leakage issue, the traditional RC-based ESD detection circuit is still the most useful and convenient circuit in the ESD protection design.

In this work, a power-rail ESD clamp circuit with the metal-oxide-metal (MOM) capacitor of ultra low leakage is proposed and verified in a 65-nm CMOS process with the thin-gate oxide devices.

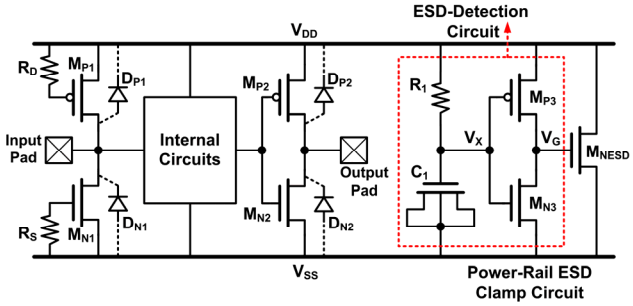

Fig. 1. Typical on-chip ESD protection scheme.

II. Gate-Tunneling Mechanisms and Impacts on Traditional Power-Rail ESD Clamp Circuit with MOS Capacitor

Three kinds of gate-tunneling mechanisms (ECB, EVB, and HVB) were reported to explain the gate leakage in CMOS technology [2], [3], as shown in Fig. 2. The ECB is the electron tunneling from the conduction band across the oxide barrier and it basically needs 3.1eV before the electron has the probability to tunnel across the oxide barrier. The EVB is the electron tunneling from the valence band across the oxide barrier and it basically needs 4.2eV before the electron has the probability to tunnel across the oxide barrier. The HVB is the hole tunneling from the valence band across the oxide barrier and basically needs 4.5eV before the hole has the probability to tunnel across the oxide barrier. When the gate-oxide thickness is scaled down, the tunneling carriers increase with a great proportion to cause the gate leakage current. In the nanoscale CMOS processes, the gate-oxide thickness in MOS devices is only a few nanometers and it has been reported to have large leakage current. Due to the gate leakage of the MOS capacitor (C_1) in the ESD-

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detection circuit, the PMOS (M_{P3}) in the ESD-detection circuit (shown in Fig. 1) cannot be fully turned off, which causes another leakage path through the inverter in the ESD-detection circuit under normal circuit operating conditions. If the ESD clamp device is realized by NMOS (M_{NESD}), the large size ESD clamp NMOS will leak more current because its gate voltage was not fully biased to V_{SS} under normal circuit operating conditions due to the gate leakage on the MOS capacitor (C_1).

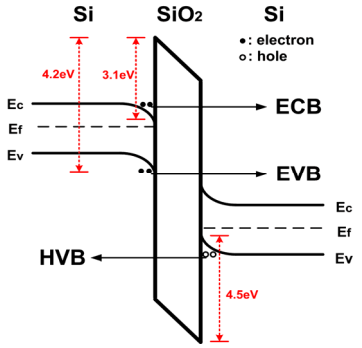


Fig. 2. Gate-tunneling mechanisms in MOS structure.

III. Power-Rail ESD Clamp Circuit with MOM Capacitor

MOM capacitors have been commonly used in IC design, because the MOM capacitor has higher linearity, higher quality factor (Q), small temperature variation, and almost no leakage current [7]. But in the early generation of CMOS processes, the capacitance density of MOM capacitor is very low, because the lateral and vertical intervals between metal layers are not close enough. As the result, the MOM capacitor would consume more chip area than MOS capacitor to achieve the required capacitance. However, when the dimensions keep shrinking in advanced CMOS processes, the capacitance density of MOM is increased significantly. Thus, to realize the ESD-detection circuit with MOM capacitor will not occupy large chip area. Therefore, the MOM capacitor used in the ESD-detection circuit can solve the leakage issue in the traditional design with MOS capacitor. The proposed low-leakage power-rail ESD clamp circuit with MOM capacitor (C_1) is shown in Fig. 3, which consists of the ESD-detection circuit with MOM capacitor and the substrate-triggered silicon-controlled rectifier (STSCR) as the ESD clamp device. Without the thin gate-oxide structure, SCR has very low leakage current under normal circuit operating conditions. Besides, SCR had been proven to have the highest ESD robustness under the smallest device size [8]. Moreover, SCR can be safely used without latchup danger in advanced CMOS technologies with low supply voltage. The power-rail ESD clamp circuit is designed to provide ESD current path between V_{DD} and V_{SS} during ESD stresses, and to be kept off under normal circuit operating conditions. To meet these requirements, the RC time constant in the ESD-detection circuit is designed to be about 0.1–1 μs to achieve the desired operations.

A. Operation Under Normal Circuit Operating Conditions

Under the normal V_{DD} power-on conditions, the V_{DD} power-on voltage waveform has a rise time in the order of millisecond (ms). With a slow rise time of the normal power-on transition, the voltage level at V_x can follow up the V_{DD} voltage waveform in time to keep M_{P1} off. Simultaneously, the M_{N1} is turned on because its gate terminal is connected to V_x. Therefore, no trigger current is injected into STSCR. As the result, STSCR can be kept off under normal circuit operating conditions. Fig. 4 shows the simulated transient waveforms of the ESD-detection circuit with MOM capacitor under normal power-on transition with a rise time of 0.1 ms. With the power-supply voltage of 1 V, the simulated overall leakage current of the power-rail ESD clamp circuit is only about 307 nA at 25 °C.

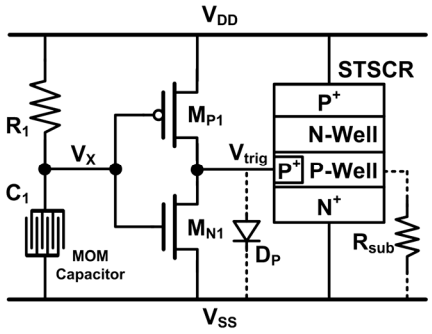


Fig. 3. Low-leakage power-rail ESD clamp circuit with MOM capacitor (C_1).

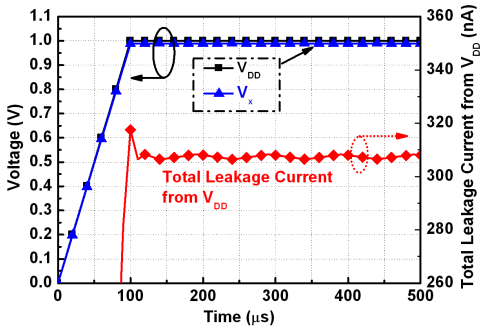


Fig. 4. Simulated transient waveforms of the ESD-detection circuit under normal power-on transition.

B. Operation Under ESD-Stress Conditions

Under the ESD-stress conditions, the ESD voltage has a rise time in the order of nanosecond (ns). The voltage level of V_X in Fig. 3 is increased very slower than the voltage level at V_{DD} power line when the ESD stress is conducted across V_{DD} and V_{SS} power lines. With the relatively lower voltage level kept at V_X due to the RC delay, the PMOS (M_{P1}) in the ESD-detection circuit will be turned on to inject trigger current into the V_{trig} of STSCR. Consequently, the turned-on STSCR provides a low-impedance path to discharge ESD current from V_{DD} to V_{SS}. Although the equivelant circuit model of STSCR device is needed to preciously simulate the quasi-static trigger point and the

clamping voltage during high-current conditions, the P-well/N+ diode (D_P) and P-substrate resistor (R_{sub}) can be used to represent the STSCR device before it turned on. Thus, the trigger ability of ESD-detection circuit with D_P and R_{sub} can be simulated. Fig. 5 shows the simulated voltage waveforms and the trigger current of the ESD-detection circuit with MOM capacitor under ESD-like stress condition. When a 5-V voltage pulse with 10-ns rise time and 100-ns pulse width is applied to V_{DD}, which is used to simulate the rising edge of ESD event before device junction breakdown, the ESD-detection circuit can successfully inject the trigger current of ~40 mA to trigger on the STSCR.

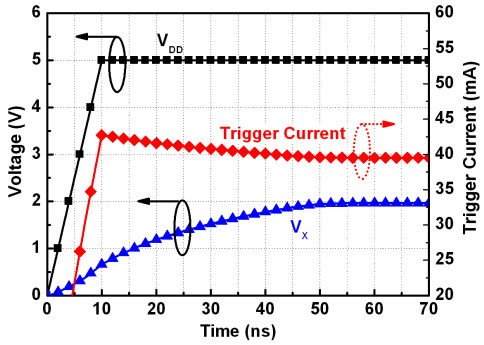


Fig. 5. Simulated transient waveforms of the ESD-detection circuit under ESD-like stress condition.

IV. Experimental Results

The RC-based power-rail ESD clamp circuit with different capacitors have been drawn in the same test chip and fabricated in the same wafer by a 65-nm CMOS process. All devices used in this work are fully-silicided thin-oxide (1-V) devices without using the additional silicide-blocking mask. The device dimensions used in the power-rail ESD clamp circuits are listed in Table I, where these two circuits have the same RC time constant of 200 ns. To achieve 2-pF capacitance, the NMOS capacitor is drawn with 29 μm channel width (W_C) and 28 μm channel length (L_C) to occupy a total layout area of 37 μm x 34 μm. With the same capacitance, the MOM capacitor which realized with 3-layer metals can have similar layout area as compared to that of the MOS capacitor. Thus, each power-rail ESD clamp circuit occupies the same layout area of 45 μm × 75 μm in this work. The chip photograph of the fabricated power-rail ESD clamp circuits and test devices is shown in Fig. 6. Figs. 7(a) and 7(b) show the measured gate leakage currents of the PMOS and NMOS capacitors (W_C = 29 μm and L_C = 28 μm) with gate-oxide thickness of ~20 Å in a 65-nm CMOS low-voltage process, respectively. Under 1-V bias, the gate leakage current of PMOS capacitor (NMOS capacitor) at 25 °C is as high as 21 μA (51 μA). The leakage currents between two power-rail ESD clamp circuits at different temperatures are compared in Fig. 8 with V_{DD} of 1 V. Besides, the leakage currents at 25 °C and 125 °C are also listed in Table II. Comparing with the leakage current of the stand-alone NMOS capacitor, much higher leakage current is observed in the power-rail ESD clamp circuit with NMOS capacitor (828 μA), which indicates that the leaky MOS capacitor actually causes other leakage path in the ESD-detection circuit. However, the leakage current of the low-leakage design with MOM capacitor has the lowest leakage current of only 358 nA. The leakage current of the design with MOM capacitor is three orders smaller than that with NMOS capacitor from low temperature to high temperature.

TABLE I. Device Dimensions in Power-Rail ESD Clamp Circuits

Circuit Type	R1	Cap. Layout Area (W/L)	M_{P1} (W/L)	M_{N1} (W/L)	STSCR (W/L)
With NMOS Capacitor	100 kΩ	37 μm / 34 μm	100 μm / 0.15 μm	20 μm / 0.15 μm	40 μm / 7.8 μm
With MOM Capacitor	100 kΩ	39 μm / 36 μm	100μm / 0.15 μm	20 μm / 0.15 μm	40 μm / 7.8 μm

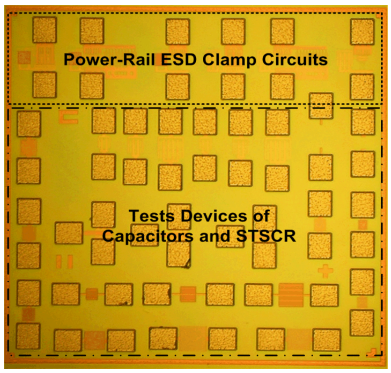
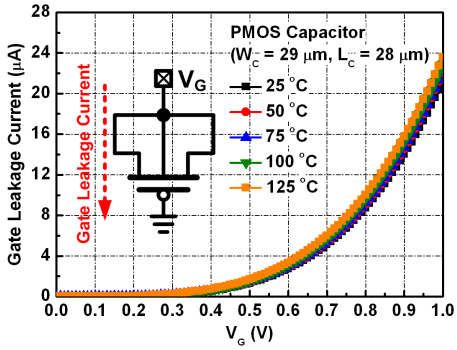
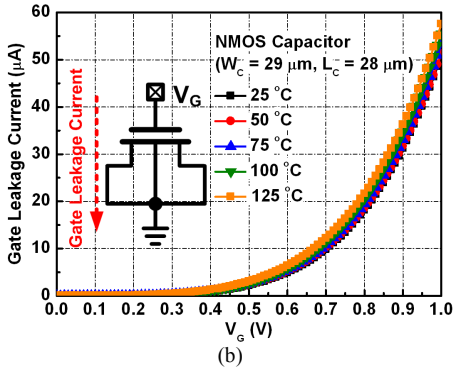


Fig. 6. Chip photograph of the fabricated power-rail ESD clamp circuits and test devices in a 65-nm CMOS process.



(a)



(b)

Fig. 7. Measured gate leakage current of the 65-nm (a) PMOS and (b) NMOS capacitor at different temperatures.

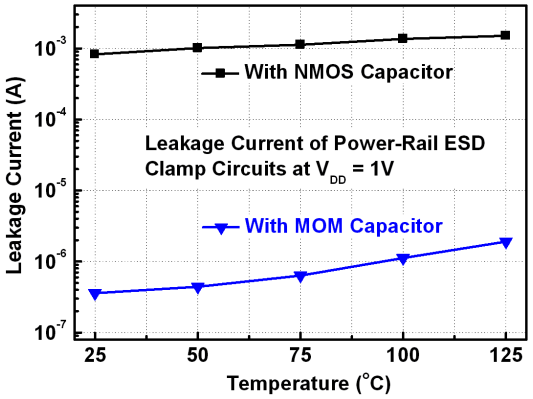


Fig. 8. Measured leakage currents between two fabricated power-rail ESD clamp circuits under different temperatures.

To investigate the turn-on behavior of the ESD clamp device with ESD-detection circuit during ESD stress event, the transmission line pulse (TLP) generator with 100-ns pulse width and 10-ns rise time was used to measure the second breakdown current (I_{t2}) of ESD protection circuits. The TLP-measured I-V characteristics of the STSCR with and without the ESD-detection circuit are shown in Fig. 9. Without any trigger current, the original trigger voltage (V_{t1}) of stand-alone STSCR (width = 40 μm) device is as high as 10.7 V, and the I_{t2} is 2.3 A. However, with the proposed ESD-detection circuit, the V_{t1} of the STSCR device is significantly reduced to 3 V and the I_{t2} is 2.5 A. Therefore, the lower V_{t1} of the power-rail ESD clamp circuit ensures its effective ESD protection capability. In addition, the holding voltage of SCR shown in Fig. 9 is ~2.5 V; therefore this proposed power-rail ESD clamp circuit is free to the latchup issue in the CMOS ICs with V_{DD} of 1V.

The human-body-model (HBM) and machine-model (MM) ESD levels of these two power-rail ESD clamp circuits are evaluated by the ESD simulator (ETS-910). These data are also listed in Table II. The failure criterion is defined as 30 % shift in the leakage current under 1-V V_{DD} bias. The power-rail ESD clamp circuit with SCR width of only 40 μm can achieve ESD robustness of 4 kV in HBM and 350 V in MM, respectively.

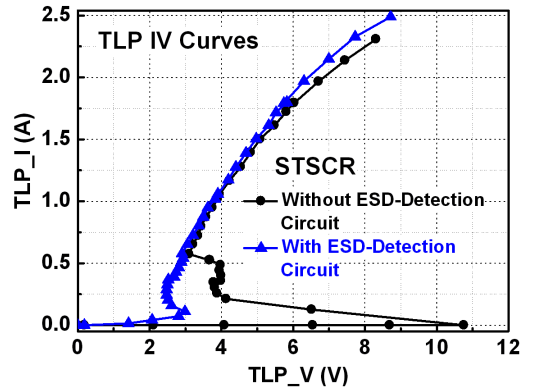


Fig.9. TLP-measured I-V characteristics of the STSCR with and without the proposed ESD-detection circuit.

TABLE II. MEASURED LEAKAGE CURRENTS AND HBM/MM ESD ROBUSTNESS BETWEEN THE FABRICATED POWER-RAIL ESD CLAMP CIRCUITS

Circuit Type	Leakage Current at V_{DD} = 1V		ESD Robustness	
	25 °C	125 °C	HBM	MM
With NMOS Capacitor	828 μA	1.53 mA	4 kV	350 V
With MOM Capacitor	358 nA	1.91 μA	4 kV	350 V

V. CONCLUSION

A power-rail ESD clamp circuit designed with the consideration of gate-leakage issue has been proposed and successfully verified in a 65-nm low-voltage CMOS process. By using the MOM capacitor in the ESD-detection circuit, the power-rail ESD clamp circuit can achieve low leakage current and keep good ESD protection ability. Besides, comparing with the MOS capacitor, the MOM capacitor does not consume more layout area. The power-rail ESD clamp circuit with MOM capacitor is suitable for on-chip ESD protection design in advanced nanoscale CMOS processes.

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