Transient-to-Digital Converter to Detect Electrical Fast Transient (EFT) Disturbance for System Protection Design

Cheng-Cheng Yen, Wan-Yen Lin, Ming-Dou Ker, Ching-Ling Tsai, Shih-Fan Chen, and Tung-Yang Chen

***Abstract*—A new on-chip 4-bit transient-to-digital converter for electrical fast transient (EFT) protection design has been proposed. The converter is designed to detect EFT-induced transient disturbances and transfer different EFT voltages into digital codes under EFT tests. The experimental results in silicon chip have confirmed the successful digital output codes.**

***Index Terms* —electromagnetic compatibility (EMC), electrical fast transient (EFT) test, transient detection circuit, transient-to-digital converter.**

I. Introduction

Recently, the electrical fast transient (EFT) tests have become an important reliability issue in the microelectronic systems equipped with CMOS integrated circuits (ICs) [1]-[5]. It has been investigated that, the EFT-induced electrical transients can cause transient-induced latchup (TLU) failure in inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs. It has been reported that, for a super twisted nematic (STN) liquid crystal display (LCD) driver circuit, the electrical transient disturbance can couple into power and ground pins and cause upset states of panel. Furthermore, during transient disturbance conditions, some of EFT-induced or ESD overshooting/undershooting transients can cause locked states or malfunction on the CMOS ICs inside the microelectronics products [6]-[13].

This reliability issue results not only from the integration of more electrical functions into single chip but also from the strict requirements of reliability test standards, such as the EFT test. Typically, if display panel products are required to achieve the immunity of "level 4" in the IEC 61000-4-4 standard [14], the equipment under test (EUT) should sustain the EFT voltage level of ±2 kV under EFT tests. During EFT tests, the power lines of the CMOS ICs in the microelectronic products no longer maintained normal voltage levels, but an exponential voltage pulse with the amplitude of several tens volts occurred. Such EFT-induced transients are quite large and can randomly couple into power, or signal pins of microelectronic circuits. According to the IEC 61000-4-4 standard, for the simplified circuit diagram of the EFT generator, only the output impedance resistor (50 Ω) and the dc blocking capacitor (10 nF) are fixed. The repetitive EFT test is a test with bursts consisting of a number of fast pulses. With the repetition frequency of 5 kHz and 100 kHz, the burst repeats every 300 ms and the application time is not less than 1 minute. With a 50 Ω as output loading, due to the impedance matching, the measured pulse peak is half of the input EFT pulse voltage. The waveform of a single pulse has a rise time of about ~5ns and the pulse duration of ~50 ns. The EFT levels for testing power supply ports and for testing I/O, data, and control ports of the equipment are listed in Table I.

In order to solve such EFT issues, the traditional solution is to add some board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transients under EFT tests. However, with more functions integrated into a system-on-a-chip (SOC), such additional discrete noise-bypassing components may not be integrated into a single chip due to the limitation of chip area and substantially increase in the fabrication cost of microelectronic products. Therefore, to meet high EFT specifications for microelectronic products, the chip-level solutions without additional discrete components on the printed circuit board (PCB) are highly desired by the IC industry.

In this paper, a new on-chip 4-bit transient-to-digital converter is proposed to detect the fast electrical transients and convert different EFT voltages into digital codes under EFT tests. The test chip fabricated in a 0.13-μm CMOS process has verified the circuit performance and output digital codes.

TABLE I
Voltage Levels and Repetition Rates of EFT Tests

Level	On Power and PE (Protective Earth) Ports		On I/O (Input/Output) Signal, Data, and Control Ports	
	Voltage Peak (kV)	Repetition Rate (kHz)	Voltage Peak (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	Specified by Customer	Specified by Customer	Specified by Customer	Specified by Customer

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II. Transient Detection Circuit

Fig. 1 shows the on-chip CR-based transient detection circuit The CR-based circuit structure is designed to detect EFT-induced transient disturbance. The NMOS (M_{nr}) is used to set the initial output voltage levels at nodes V_{OUT} and V_A as 1.8 V with the V_{DD} of 1.8 V. During the normal operating condition, the node V_G is biased at 0 V by connecting to V_{SS} line through poly resistor. The two-inverter latch is designed to memorize the logic state before and after EFT events. The MOSFET capacitor is designed by PMOS device and connected between V_{DD} line and node V_G to sense transient disturbance coupled on 1.8-V power line. Under the EFT tests with an overshooting transient voltage, the node V_G will be coupled with positive voltage by MOSFET capacitor coupling. Then, the NMOS device (M_{n1}) will be turned on by the overshooting EFT voltage to pull down the voltage level at the node V_A from 1.8 V to 0 V. Therefore, the logic level stored at the node V_B can be further pulled up from logic "0" to logic "1" to memorize the EFT events. With the buffer inverters, the final output voltage of the proposed detection circuit is changed from logic "1" to logic "0" to detect the occurrence of EFT-induced transient disturbance.

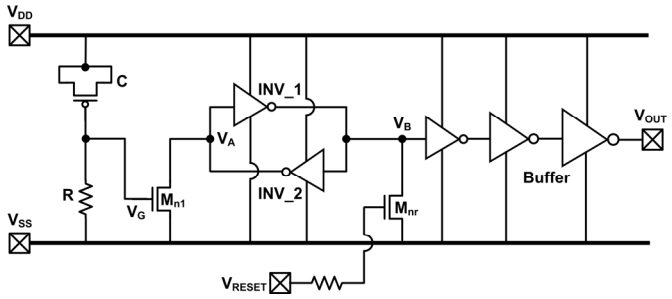

Fig. 1. The on-chip CR-based transient detection circuit.

III. Experimental Results

In order to simulate the EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with -40 dB degradation is used in this work. The amplitude of EFT-induced transients can be adjusted through the attenuation network. The measurement setup for EFT test combined with attenuation network is shown in Fig. 2. EFT generator is connected to the device under test (DUT) through the attenuation network with V_{DD} of 1.8 V.

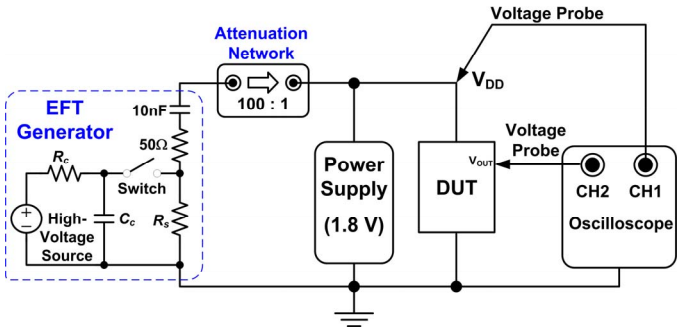

Fig. 2. Measurement setup for EFT test combined with attenuation network.

The V_{DD} and V_{OUT} transient responses of the CR-based transient detection circuit are monitored by the digital oscilloscope. Before each EFT test, the initial output voltage (V_{OUT}) is reset to 1.8 V. After each EFT test, the output voltage (V_{OUT}) level is monitored to check the final voltage level and to verify the detection function.

The measured V_{DD} and V_{OUT} waveforms of the CR-based detection circuit under EFT test with EFT voltage of +200 V (-350 V) are shown in Fig. 3(a) (Fig. 3(b)). As shown in Fig. 3(a) (Fig. 3(b)), under the EFT test with positive (negative) EFT voltage, V_{DD} begins to increase (decrease) rapidly from 1.8 V. Meanwhile, V_{OUT} begins to greatly increase (decrease) with positive (negative) exponential voltage pulse coupled on V_{DD} power line. Finally, after the EFT-induced transient disturbance, the output voltage (V_{OUT}) of the CR-based detection circuit is changed from 1.8 V to 0 V. Therefore, the detection circuit can successfully memorize the occurrence of the EFT event with positive (negative) EFT voltage.

From the EFT test results, the CR-based on-chip transient detection circuit can successfully memorize the occurrence of EFT-induced transient disturbance events.

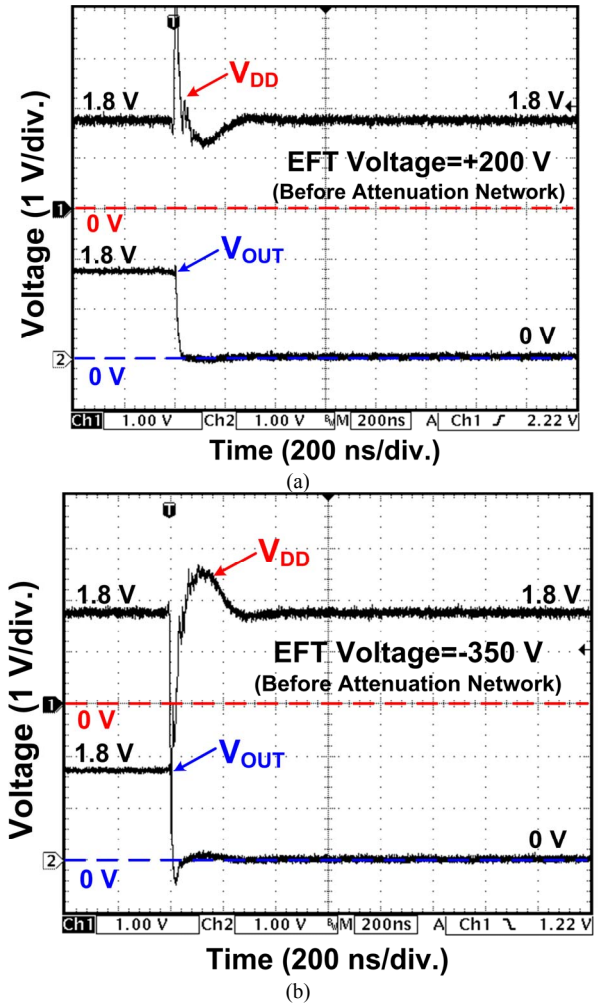

Fig. 3. Measured V_{DD} and V_{OUT} waveforms on the new proposed on-chip transient detection circuit under EFT tests with (a) +200-V, and (b) -350-V, EFT voltages combined with attenuation network.

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IV. Application in Display Panel

A. Circuit Structure

Fig. 4 shows the proposed on-chip transient-to-digital converter. For the CR-based transient detection circuit shown in Fig. 1, the EFT energy coupled to node V_G can be further adjusted by different resistive voltage dividers. Therefore, the minimum EFT voltage to cause transition at the output (V_{OUT}) of the proposed CR-based transient detection circuit can be designed for each stage in the transient-to-digital converter.

It has been also investigated that noise filter networks can reduce the susceptibility of CMOS ICs against transient disturbance by decoupling or bypassing EFT-induced noise energy. The noise filter network can suppress the transient peak voltages on power lines, which has influence on EFT voltages to cause transition at the output (V_{OUT}) of the transient detection circuit. In the previous design, 10-pF on-chip decoupling capacitor is used in noise filter network [10]. In this work, a 3-pF on-chip capacitor with a current mirror is adopted to replace the large 10-pF decoupling capacitor between power lines to avoid the gate leakage issue in nanoscale CMOS processes. With different device ratios in the current mirror, different EFT levels on V_{DD} line will reach to each transient detection circuit. Under the EFT zapping conditions, the four transient detection circuits will have different output voltage responses. Therefore, by combining with different filter networks, the proposed transient-to-digital converter can be designed to detect different EFT voltage levels and transfer output voltages into digital codes under EFT tests.

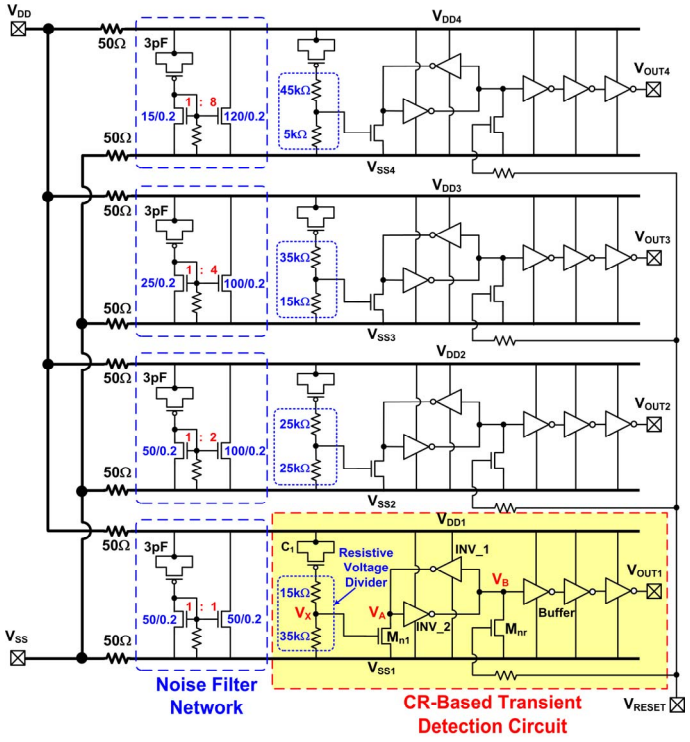

Fig. 4. The proposed 4-bit transient-to-digital converter realized with four CR-based transient detection circuits and four different noise filter networks.

B. Measurement Results

The EFT generator combined with attenuation network shown in Fig. 2 is used to evaluate the digital codes of the proposed on-chip transient-to-digital converter under EFT tests. The V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient responses of the proposed on-chip transient-to-digital converter are monitored by the digital oscilloscope. Before EFT test zapping, the initial output voltages of the proposed on-chip transient-to-digital converter are all reset to 1.8 V. After each EFT zapping, the output voltage levels are measured to check the final voltage levels and to verify the transferred digital codes.

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed transient-to-digital converter under EFT test with EFT voltage of +400 V are shown in Fig. 5. During the EFT-induced disturbance, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously. Finally, V_{OUT1} will be changed from 1.8 V to 0 V, while V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at 1.8 V. Therefore, under EFT test with EFT voltage of +400 V zapping, the detection output voltages can be transferred into a digital code of "1110."

Similarly, under EFT test with EFT voltages of +500 V, +700 V, and +2000 V, the transferred digital codes of proposed converter are "1100," "1000," and "0000," respectively. Therefore, under EFT tests with positive EFT voltages, the proposed on-chip transient-to-digital converter can successfully transfer different EFT voltage levels into digital codes.

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} voltage waveforms of the proposed transient-to-digital converter under EFT test with EFT voltage of -700 V are shown in Fig. 6. During the high-energy fast transient of EFT stress, all transient detection circuits can detect the EFT-induced transient disturbance coupled on V_{DD} line. Finally, when V_{DD} returns into the normal operation voltage level of 1.8V, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} have been pulled down from 1.8 V to 0 V. The four outputs of CR-based transient detection circuit transit from logic "1" to logic "0."

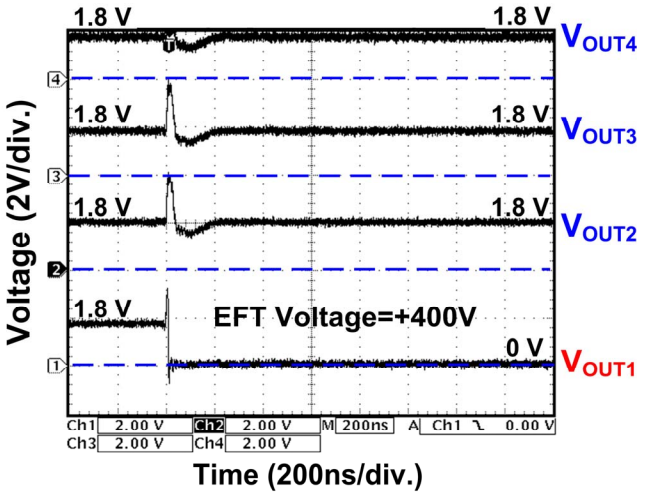

Fig. 5. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms under EFT tests with EFT voltages of +400V.

From the measurement results under EFT test with EFT voltage of -700 V, the output responds of the proposed 4-bit transient-to-digital converter can be transferred into a digital code of "0000."

Similarly, under EFT test with EFT voltages of -410 V, -450 V, and -500 V, the transferred digital codes of proposed converter are "1110," "1100," and "1000," respectively. Therefore, under EFT tests with negative EFT voltages, the proposed on-chip transient-to-digital converter can successfully transfer different EFT voltage levels into digital codes.

Table II depicts the EFT voltage to digital code characteristic of the proposed 4-bit transient-to-digital converter. Under EFT tests, larger EFT voltage levels can response to higher digital codes. The digital code goes from "1110" to "0000" as the magnitude of EFT voltage increases from +0.4 kV to +2.0 kV and from -0.41 kV to -0.7 kV.

The digital codes from transient-to-digital converter can be temporarily stored as system recovery index for different recovery procedure designs. This hardware/firmware co-design can effectively improve the robustness of the microelectronic products against EFT-induced transient disturbance.

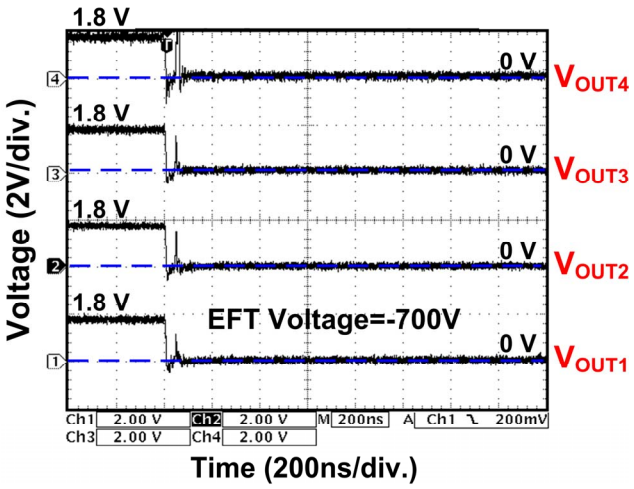

Fig. 6. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms under EFT tests with EFT voltages of -700V.

TABLE II
EFT VOLTAGE TO DIGITAL CODE CHARACTERISTIC

Digital Codes	Positive EFT Voltage (kV)	Negative EFT Voltage (kV)
1111	< +0.4	> -0.41
1110	+0.4 ~ +0.5	-0.41 ~ -0.45
1100	+0.5 ~ +0.7	-0.45 ~ -0.5
1000	+0.7 ~ +2.0	-0.5 ~ -0.7
0000	> +2.0	< -0.7

V. CONCLUSIONS

A novel transient-to-digital converter composed of four CR-based transient detection circuits and four different noise filter networks has been successfully designed and verified in a 0.13-μm CMOS process with 1.8-V devices. In this filter design, the on-chip capacitor with a current mirror can replace the large decoupling capacitor and avoid the gate leakage issue. The output digital codes can correspond to different EFT voltages under EFT tests. These output digital codes can be used as the firmware index for microelectronic products to execute different system recovery procedures and to solve the EFT-induced transient disturbance events in microelectronic systems equipped with CMOS ICs.

ACKNOWLEDGMENT

This work was partially supported by National Science Council, Taiwan, under Contract NSC 99-2811-E-009-051; and by Himax Technologies Inc., Taiwan.

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