Impact of Shielding Line on CDM ESD Robustness of Core Circuits in a 65-nm CMOS Process

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Abstract — **The charged-device-model (CDM) ESD robustness of core circuit with/without the shielding line was studied in a 65-nm CMOS process. Verified in silicon chip, the CDM ESD robustness of core circuit with the shielding line was degraded. The damage mechanism and failure location of the test circuits were investigated in this work.**

Keywords - Charged-device model (CDM), ESD, shielding line.

I. Introduction

Adding the shielding lines near to the signal lines of high-speed circuits is an efficient method to limit the inductive coupling and to reduce the crosstalk noise between signal lines [1], [2]. The signal lines are generally shielded by the shielding lines which are biased at V_{DD} or V_{SS}. However, the coupling effect between the shielding and signal lines during charged-device-model (CDM) ESD event could induce large transient current to damage the core circuits. Among the chip-level ESD test standards (HBM, MM, and CDM), the CDM ESD events play major roles to cause failures in today's manufacturing and packaging environments [3], [4]. Therefore, several ESD protection designs against CDM ESD events have been reported to protect the input/output (I/O) buffers which are directly connected to the external pins [5]. Besides the I/O buffers, the core circuits would also suffer the dangers when the CDM events happened at the I/O buffers. As shown in Fig. 1, the coupling effect between I/O line and core line during CDM ESD event can induce large transient current to damage the core circuit, even if the shielding line is inserted. In this paper, the impact of shielding line on CDM ESD robustness of core circuit is investigated in a 65-nm CMOS process.

II. Test Circuits

One set of test circuits is shown in Fig. 2. The I/O buffer realized with inverter is connected to the I/O pad through the I/O line with ESD clamp at the I/O pad. The ESD clamp is realized with the gate-grounded NMOS (GGNMOS) of 360μm/0.12μm (W/L). The core circuits without (with) inserting the shielding line between I/O line and core circuit 1 (core circuit 2) are arranged in parallel to the I/O buffer. The spacing between I/O line and core line is labeled as S, and the length of each line in layout with metal layer is labeled as L. The spacing between I/O line and the shielding line, the width of shielding metal, and the spacing between the shielding line and the core line are labeled as S1, S2, and S3, respectively. The split conditions of the test circuits with different L, S, S1, S2, and S3 are listed in Table I. The layout top view of one test circuit with 100-μm L and 0.78-μm S is shown in Fig. 3. All these circuits have been fabricated in a 65-nm CMOS process with the thin-gate oxide of ~20 Å.

III. Measurements Results and Failure Analysis

The test circuits with a die size of ~2x1.5 mm^2 have been assembled in DIP-40-pin packages. The CDM ESD stresses are applied by the field-induced CDM tester. The failure criterion is 30% shift of the leakage current under 1-V V_{DD} bias from its original level. CDM ESD robustness among these test circuits are listed in Table I. The negative CDM ESD robustness of all core circuits exceeded -600 V. The positive CDM ESD robustness of some core circuits without inserting the shielding line exceeded 600 V. Even if the metal length (L) of core circuits without inserting shielding is reduced, which leads to the lower impedance and higher overshoot voltage, the positive CDM ESD robustness can still achieve 400 V. However, the positive CDM ESD robustness of core circuits with inserting the shielding line are seriously degraded to only 100 V.

As shown in Fig. 4, there are two discharging paths (path1 and path2) from the core circuits to the grounded I/O pad during the CDM ESD stress. The CDM charges located around the p-substrate of core circuits can be conducted through the P+ pickup of core circuits into the V_{SS} line, and then discharged through the ESD clamp device at the I/O pad to external ground, as the dashed line of path1 shown in Fig. 4. The CDM ESD event typically has a fast rise time of only ~0.2 ns. Such very fast transient ESD pulse will be inherently conducted by the displacement current of capacitor, $i = C \times (dv/dt)$, to the external ground through the path with capacitive structures. When the parasitic capacitance becomes larger due to inserting the shielding line between I/O line and core line in chip layout, some of CDM charges will be discharged by the displacement current, as the dashed line of path2 shown in Fig. 4. Since the positive charges located around the PMOS of core circuit can not be efficiently discharged through the P+ pickup and ESD clamp, the positive charges located around the PMOS can only be discharged through the gate oxide of PMOS (path2), which is a capacitive path with low impedance under fast transient. The ESD current discharged through the thin gate oxide of PMOS in the core circuit will cause damage on it.

The scanning-electron-microscope (SEM) photograph of the test circuit with 100-μm L and 0.78-μm S after 200-V CDM ESD test is shown in Fig. 5. The failure point is located only at the poly gate of PMOS transistor in core circuit 2, which fully agrees with aforementioned explanation in Fig. 4.

When the CDM charges stored in the P-substrate is negative, the high reverse breakdown voltage of the parasitic P-substrate/N-well diode will limit the CDM current being discharged through the path2 to external ground. Therefore, the negative CDM ESD robustness was not degraded by inserting the shielding line in chip layout, as compared in Table I.

IV. Conclusion

After inserting the shielding line between I/O line and core signal line, the coupling effect during CDM ESD event has been found to induce large transient current to damage the core circuits. This mechanism has been practically verified in silicon chip. The experimental results of this work can help foundries or IC design houses to optimize their layouts for better CDM ESD protection.

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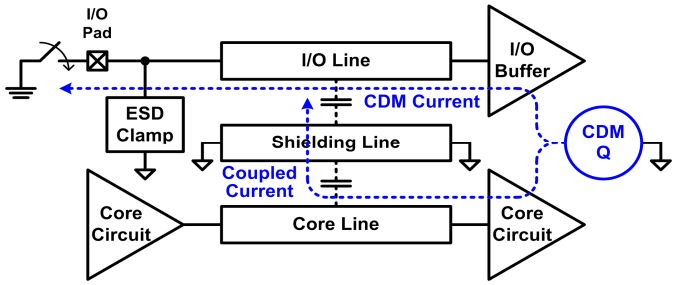

Figure 1. CDM ESD issues at I/O buffer and core circuit.

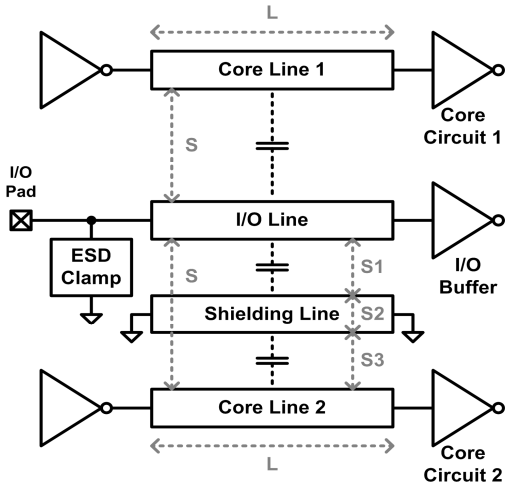

Figure 2. Test circuit without (with) inserting shielding between I/O line and core circuit 1 (core circuit 2).

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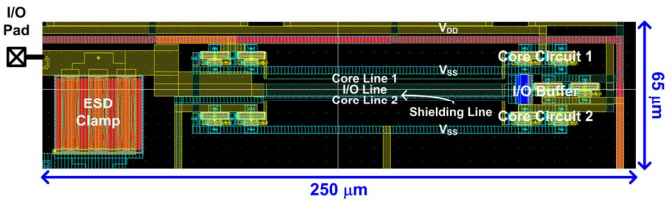

Figure 3. Layout top view of one test circuit for fabrication in a 65-nm CMOS process with 1-V devices.

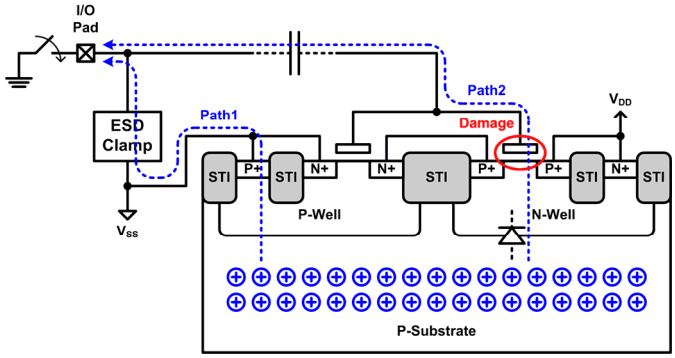

Figure 4. PMOS of core circuit suffers serious CDM damage during CDM ESD event with positive charges.

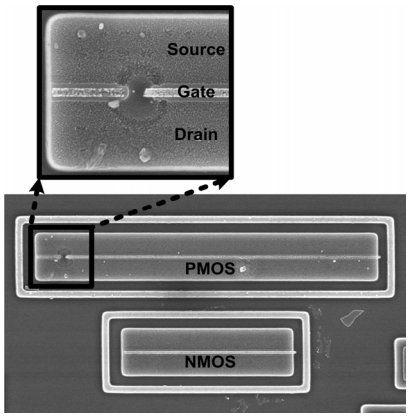

Figure 5. SEM photo of failure point in core circuit 2 after 200-V CDM test.

Table I. CDM ESD robustness of test circuits with/without inserting the shielding line between I/O line and core line.

Core Circuit 1 (Without Shielding)							Core Circuit 2 (With Shielding)						
L (μm)	*S (μm)*	*S1 (μm)*	*S2 (μm)*	*S3 (μm)*	*Positive CDM ESD Robustness (V)*	*Negative CDM ESD Robustness (V)*	*L (μm)*	*S (μm)*	*S1 (μm)*	*S2 (μm)*	*S3 (μm)*	*Positive CDM ESD Robustness (V)*	*Negative CDM ESD Robustness (V)*
20	0.78	N/A	N/A	N/A	400	< -600	20	0.78	0.3	0.18	0.3	**100**	< -600
20	1.98	N/A	N/A	N/A	> 600	< -600	20	1.98	0.3	0.18	1.5	**100**	< -600
50	0.78	N/A	N/A	N/A	400	< -600	50	0.78	0.3	0.18	0.3	**100**	< -600
50	1.98	N/A	N/A	N/A	> 600	< -600	50	1.98	0.3	0.18	1.5	**100**	< -600
100	0.78	N/A	N/A	N/A	> 600	< -600	100	0.78	0.3	0.18	0.3	**100**	< -600
100	1.98	N/A	N/A	N/A	> 600	< -600	100	1.98	0.3	0.18	1.5	**100**	< -600

* The CDM test voltage was increased in 100-V step.