Design of Power-Rail ESD Clamp Circuit with Adjustable Holding Voltage against Mis-trigger or Transient-Induced Latch-On Events

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***Abstract* -- In this work, a new design of the ESD-transient detection circuit with the n-channel metal-oxide-semiconductor (nMOS) transistor drawn in the layout style of big field-effect transistor (BigFET) has been proposed and verified in a 65nm 1.2V CMOS process. As compared to the traditional *RC*-based ESD-transient detection circuit, the layout area of the new ESD-transient detection circuit can be greatly reduced by more than 54%. From the experimental results, the new proposed ESD-transient detection circuit with adjustable holding voltage can achieve long turn-on duration under the ESD stress condition, as well as better immunity against mis-trigger or transient-induced latch-on event under the fast power-on and transient noise conditions.**

I. INTRODUCTION

With the continuously scaled-down CMOS technology, electrostatic discharge (ESD) protection has become the major concern of reliability for integrated circuits (ICs) in nanoscale CMOS technology. The nanoscale device with thinner gate oxide and shallower diffusion junction depth seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [1]. For the power-rail ESD clamp circuit, it is an important element to achieve whole-chip ESD protection under V_{DD}-to-V_{SS} (or V_{SS}-to-V_{DD}) ESD stress, as well as different ESD stress conditions from the input/output to V_{DD}/V_{SS}, including positive-to-V_{SS} (PS) mode, negative-to-V_{SS} (NS) mode, positive-to-V_{DD} (PD) mode, and negative-to-V_{DD} (ND) mode, which are illustrated in Fig. 1 [2]. Therefore, the power-rail ESD clamp circuit can provide efficient protection to the internal circuits of IC products.

The ESD clamp device drawn in the layout style of big field-effect transistor (BigFET) had revealed excellent ESD protection performance in advanced nanoscale CMOS ICs [3]-[6]. Practically, there are two different circuit skills, the *RC*-delay technique [3]-[4] and the capacitance-coupling design [5]-[6], to realize the ESD-transient detection circuit in the power-rail ESD clamp circuit. The traditional *RC*-based power-rail ESD clamp circuit was shown in Fig. 2. The turn-on duration of the ESD clamp device is mainly controlled by the *RC* time constant of the ESD-transient detection circuit. Consequently, the *RC* time constant would be designed large enough about several hundreds nanosecond to keep the ESD clamp device at "ON" state under the ESD stress condition. However, the extended *RC* time constant of the ESD-transient detection circuit suffers not only the larger layout area from the resistance and capacitance but also the mis-trigger of the ESD clamp circuit under fast-power-on application [6].

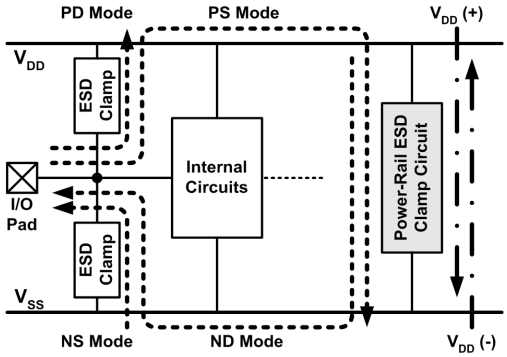


Fig. 1. Typical on-chip ESD protection design with active power-rail ESD clamp circuit under different ESD stress conditions.

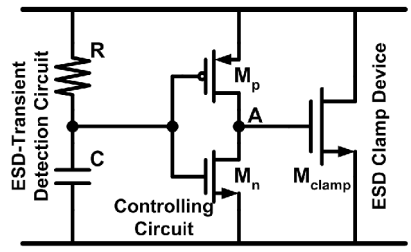


Fig. 2. Typical *RC*-based power-rail ESD clamp circuit with ESD-transient detection circuit, controlling circuit, and ESD clamp device.

In previous studies [3]-[6], they demonstrated the power-rail ESD clamp circuits with feedback circuit methods to extend the turn-on duration. However, the feedback circuit designs would suffer the latch-on issue under the fast power-on or the electrical fast transient (EFT) conditions [7]. Moreover, on-time control circuits [3] had also been used to extend the turn-on duration without the latch-on issue. However, this previous circuit is more complicated with large silicon layout area including the requested resistances and capacitances in the ESD-transient detection circuit.

In this work, a new ESD-transient detection circuit, which is combined with the parasitic capacitance of the ESD clamp nMOS transistor drawn in BigFET layout style, has been proposed and verified in 65nm 1.2V CMOS technology [8]. According to the experimental measured results, the power-rail ESD clamp circuit with the new proposed ESD-transient

detection circuit has revealed a much better performance than that in the traditional *RC*-based power-rail ESD clamp circuit.

II. New Power-Rail ESD Clamp Circuit

A. New Proposed ESD-Transient Detection Circuit

The new ESD-transient detection circuit with different number of diodes in series is illustrated in Fig. 3. The proposed power-rail ESD clamp circuit consists of the ESD-transient detection circuit with feedback technique, which is realized by two transistors (M_n and M_p) and two resistances (R_n and R_p), and the ESD clamp nMOS transistor (M_{clamp}) drawn in BigFET layout style. The gate terminal of M_{clamp} is linked to the output of the ESD-transient detection circuit. The ESD-transient detection circuit with positive-feedback mechanism is constructed by a cascode structure (R_n with M_n, and M_p with R_p), which can command M_{clamp} at "ON" or "OFF" state.

To overcome the transient-induced latch-on issue, the ESD-transient detection circuit is added with one or two diodes to adjust its holding voltage, as shown in Fig. 3. With such a modification, the holding voltage of the power-rail ESD clamp circuit can be adjusted by adding the diodes.

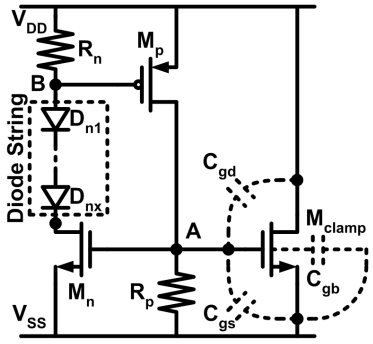


Fig. 3. New proposed power-rail ESD clamp circuit. There are zero, one, and two diodes used in the ESD-transient detection circuit in this work.

B. Operation Principles under ESD Stress

Because the ESD clamp nMOS transistor is drawn in BigFET layout style without silicide blocking, large C_{gd}, C_{gs}, and C_{gb} parasitic capacitances essentially exist in the ESD clamp nMOS transistor. Sufficiently utilizing these parasitic capacitances with the resistance R_p to realize capacitance-coupling mechanism, no additional capacitor is needed in this design. In Fig. 3, the gain (G) of the coupling effect composed of C_{gd}, C_{gs}, C_{gb}, and R_p during the positive V_{DD}-to-V_{SS} ESD stress condition can be expressed as

$$G = \frac{V_A}{V_{DD}} = \left| \frac{\left(\frac{1}{R_p} + j\omega\left(C_{gs} + C_{gb}\right)\right)^{-1}}{\frac{1}{j\omega C_{gd}} + \left(\frac{1}{R_p} + j\omega\left(C_{gs} + C_{gb}\right)\right)^{-1}} \right| \quad (1)$$

According to the design parameters of the proposed power-rail ESD clamp circuit, the gain would be 0.34 with $C_{gd} \fallingdotseq C_{gs}$=0.43pF, C_{gb}=0.39pF, R_p=20kΩ, and signal frequency of 50MHz derived from 5ns fast-rising edge of the voltage pulse.

A 3V voltage pulse with a rise time of 5ns was applied to the V_{DD} node while the V_{SS} node was grounded to simulate the fast-rising edge of the HBM ESD event, as illustrated in Fig. 4. As shown in Fig. 4(a), the coupling voltage at node A is exactly equal to 0.34V_{DD} before the ESD-transient detection circuit is turned on. The M_n is designed to immediately start the ESD-transient detection circuit with positive feedback mechanism when the voltage of node A is elevated. When the sub-threshold current of the M_n can produce enough voltage drop on R_n to further turn on the M_p, the voltage at node A would be elevated quickly to the voltage level at V_{DD} because the ESD-transient detection circuit is turned on. Consequently, the ESD clamp nMOS transistor is turned on by the ESD-transient detection circuit with positive feedback mechanism. In Fig. 4(b), the voltage at node A of the new proposed power-rail ESD clamp circuit can be obviously elevated to the voltage level at V_{DD}. However, the voltage at node A in the *RC*-based power-rail ESD clamp circuit is elevated to the voltage level higher than the threshold voltage of ~0.58V for only the first period of ~300ns. The design parameters, including the device sizes of each transistor and resistor, are listed in Table I. On the other hand, the parasitic drain-substrate diode in the ESD clamp nMOS transistor can provide a low impedance path under the negative V_{DD}-to-V_{SS} ESD stress.

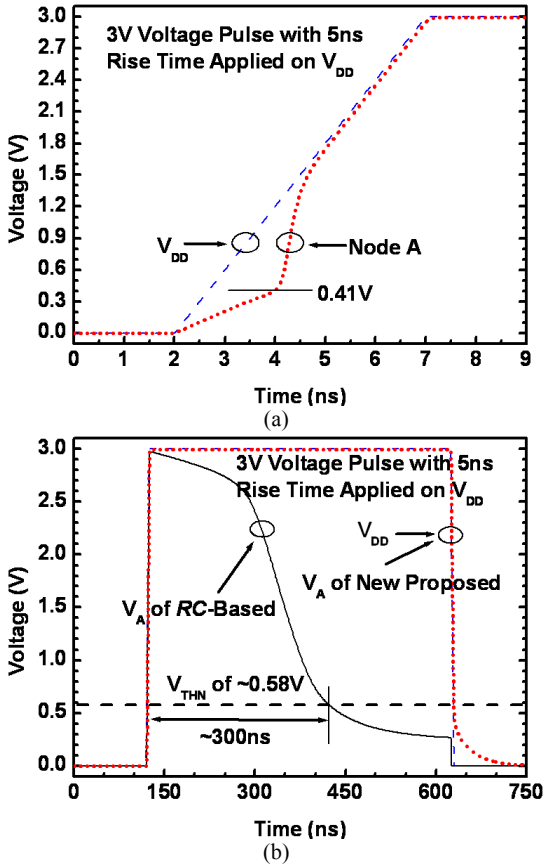


Fig. 4. The simulation results of the voltage transient on V_{DD} and node A for (a) node coupling of new proposed power-rail ESD clamp circuit and for (b) turn-on duration of the power-rail ESD clamp circuits. The 3V ESD-like voltage pulse with 5ns rise time is applied on V_{DD}.

TABLE I
DESIGN PARAMETERS OF THE POWER-RAIL ESD CLAMP CIRCUITS

Design Parameters	*RC*-Based ESD Clamp Circuit	New Proposed ESD Clamp Circuit
Capacitor	64 μm / 2 μm (W/L)	none
Resistor (Ω)	R = 113k	R_n = 40k ; R_p = 20k
PMOS Transistor (M_p)	184 μm / 60 nm	24 μm / 60 nm
NMOS Transistor (M_n)	36 μm / 60 nm	12 μm / 60 nm
ESD Clamp NMOS Transistor (M_{clamp})	2000 μm / 100 nm	2000 μm / 100 nm
Diode (D_n)	none	0.057 μm²

For avoiding the latch-on issue, the holding voltage (V_h) of the ESD protection circuit should be designed to exceed the normal circuit operation voltage V_{DD}. The holding voltage of the proposed power-rail ESD clamp circuit can be indicated as

$$\begin{aligned} V_h &= V_{ds(M_n)} + nV_{ON(Diode)} + V_{gs(M_p)} \\ &= V_{ds(M_n)}\Big|_{I_{ds}=V_{THP}/R_n} + nV_{ON(Diode)} + V_{THP} \\ &\approx nV_{ON(Diode)} + V_{THP} \end{aligned} \quad (2)$$

where n and V_{ON} are the number and the turn-on voltage of the diode, respectively. Based on the device sizes and simulation results, the V_{ds} of M_n transistor is only a few milli-volt and the V_{ON} of diode is about 0.67V. Therefore, the V_h can be represented as the bottom line in the expression (2) due to minor V_{ds} compared to V_{ON} (0.67V) and V_{THP} (0.58V).

III. EXPERIMENTAL RESULTS

The test-chips of power-rail ESD clamp circuits with the traditional *RC*-based and the new proposed ESD-transient detection circuits have been fabricated in a 65nm 1.2V CMOS process. Compared with the traditional *RC*-based ESD-transient detection circuit, the layout area of the new proposed ESD-transient detection circuit is much smaller by 54.5%. Besides, the cell height of the whole power-rail ESD clamp circuit is reduced by 30%, as illustrated in Fig. 5(a) and (b).

A. TLP Measurement

In order to investigate the circuit behavior during high ESD current stress, transmission line pulsing (TLP) generator with a pulse width of 100ns and a rise time of ~2ns is used to measure the power-rail ESD clamp circuits [9]. The ESD clamp circuit is defined to be failed when the leakage current is over 1μA at 1.2V operation voltage. As shown in Fig. 6(a), there are no obvious differences among the curves higher than 4V because the M_{clamp} in all power-rail ESD clamp circuits is drawn with the same device dimension and layout style. The second breakdown currents (It_2) of these four power-rail ESD clamp circuits are all around 5.44A.

The holding voltage of the new proposed ESD-transient detection circuits with zero, one, and two diodes are 0.51V, 1.22V, and 1.95V, respectively, as shown in Fig. 6(b). These measured holding voltages are very close to the theoretical ones of 0.58V, 1.25V, and 1.92V calculated in expression (2). By modifying the number of diodes in the ESD-transient detection circuit, the adjustable holding voltage has been successfully verified by the TLP I-V measurement. The new proposed power-rail ESD clamp circuit with adjustable holding voltage, therefore, can be safely applied to protect any internal circuits from the transient-induced latch-on event.

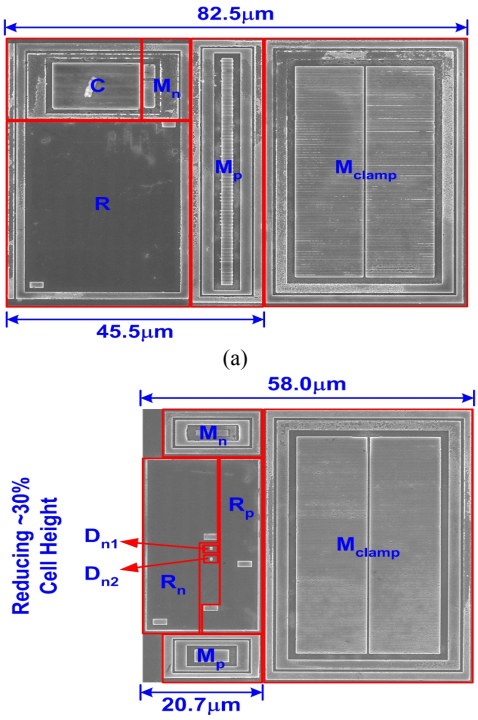


Fig. 5. Chip microphotographs of the power-rail ESD clamp circuit realized with (a) the traditional *RC*-based ESD-transient detection circuit and (b) the proposed ESD-transient detection circuit with two diodes.

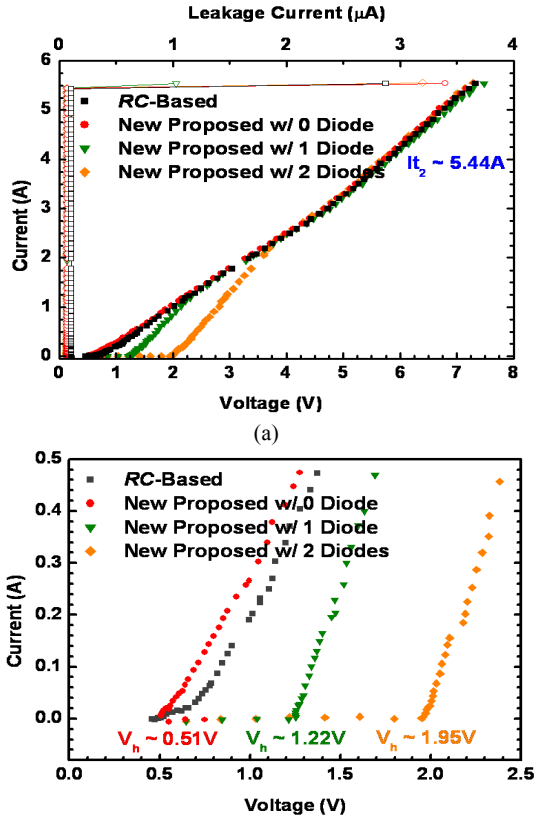
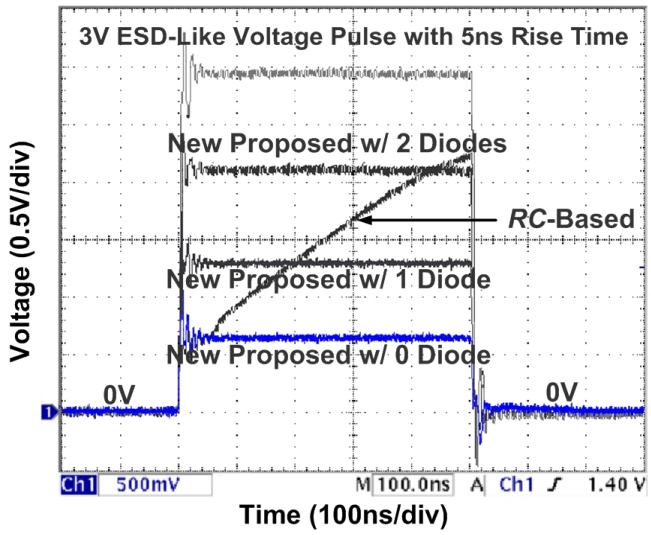


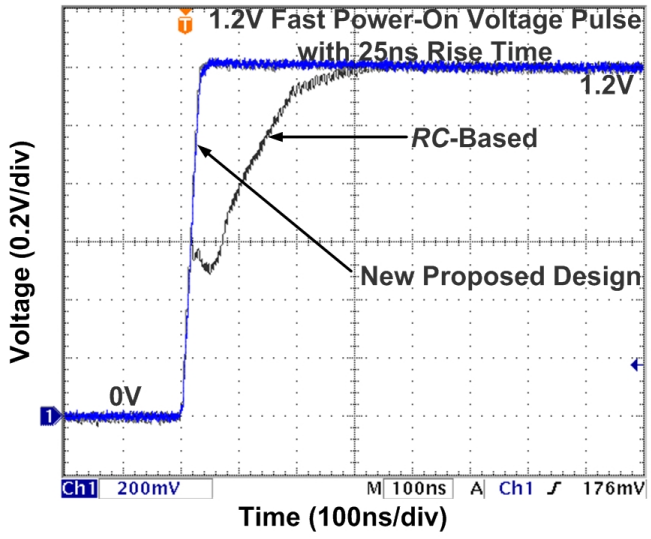
Fig. 6. TLP measured I-V curves of (a) the power-rail ESD clamp circuits with the *RC*-based, the new proposed ESD-transient detection circuit, and (b) the zoom-in illustration for the holding voltages (V_h).

B. Turn-On Verification

In order to observe the turn-on efficiency of the power-rail ESD clamp circuits, a 3V pulse with 5ns rise time to simulate the fast-rising edge of the HBM ESD event is applied to the V_{DD} power line with the grounded V_{SS}. In Fig. 7(a), the voltage waveform of the *RC*-based design rises as the time is increased. On the contrary, the voltage waveforms of the new proposed designs can be clamped to a specific voltage level and the turn-on duration of the M_{clamp} can be efficiently extended during the whole pulse width due to the positive feedback mechanism of the ESD-transient detection circuit.



(a)



(b)

Fig. 7. The voltage waveforms under (a) ESD-transient-like condition with 3V voltage pulse and 5ns rise time, (b) fast-power-on condition with 1.2V voltage pulse and 25ns rise time.

For power-on condition, the voltage usually has a rise time in the order of milliseconds. According to this feature, the coupling voltage at node A is not enough to start up the ESD-transient detection circuit, and the M_{clamp} will be kept at "OFF" state. However, some previous studies [3]-[4] have demonstrated that the power-rail ESD clamp circuits with *RC*-based ESD-transient detection circuits and feedback mechanism were easily mis-triggered and into the latch-on state, respectively, under the fast power-on condition. The new proposed power-rail ESD clamp circuits have been applied with 1.2V voltage pulse with 25ns rise time to investigate their immunity against mis-trigger, as shown in Fig. 7(b). The voltage waveforms of the new proposed power-rail ESD clamp circuits are not degraded under the fast power-on condition. Even though the rise time of fast power-on voltage is shorter than 25ns, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can still perform high immunity against mis-trigger. On the contrary, the *RC*-based power-rail ESD clamp circuit dramatically suffered the mis-trigger under the fast power-on condition, and it spends about 300ns to return back the normal operation voltage level.

IV. Conclusion

The new power-rail ESD clamp circuits with adjustable holding voltage designs have been proposed and successfully verified in a 65nm 1.2V CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance-coupling mechanism to command the ESD clamp nMOS transistor. According to the measured results, the new proposed power-rail ESD clamp circuits demonstrate excellent immunity against mis-trigger under the fast power-on condition, and also perform no latch-on issue under power noise measurement. Moreover, the new proposed ESD-transient detection circuits are also area-efficient, which save layout area by more than 54% compared with the traditional *RC*-based ESD-transient detection circuit.

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