2011 11th IEEE International Conference on Nanotechnology
Portland Marriott
August 15-18, 2011, Portland, Oregon, USA

ESD Protection Consideration in Nanoscale CMOS Technology

Ming-Dou Ker and Chun-Yu Lin

Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
Email: mdker@ieee.org

***Abstract* — The thinner gate oxide in nanoscale CMOS technologies seriously degraded the electrostatic discharge (ESD) robustness of IC products. As the feature sizes in nanoscale CMOS technologies are further scaling down, the on-chip ESD protection designs are more challenging. The ESD protection considerations, including ESD design window, area efficiency, leakage current, and high-voltage tolerance, were presented in this abstract. Some possible solutions against these issues in nanoscale CMOS technologies were also included in this paper.**

Index Terms* – *CMOS, electrostatic discharge (ESD), on-chip ESD protection.

I. Introduction

Nanoscale CMOS technologies have been used to implement integrated circuits with the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of IC products. The minimum requirement for a sub-50nm IC product is to pass 500-V human-body-model (HBM) ESD test [1]. Therefore, ESD protection designs must be added in IC chips. The typical on-chip ESD protection design is shown in Fig. 1 [2], which consists of the ESD protection devices between input/output (I/O) pad and V_{DD}/V_{SS}, and the power-rail ESD clamp circuit between V_{DD} and V_{SS}. However, there are some issues in the scaling-down CMOS technologies. The ESD protection considerations in nanoscale CMOS technologies and some possible solutions against these issues will be introduced in this paper.

II. ESD Protection Considerations in Nanoscale CMOS Technologies

A. ESD Design Window

Fig. 2 shows the ESD design window of an IC [1], which is defined by the power-supply voltage (V_{DD}) of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage (V_{BD}) of MOSFET. First, the trigger voltage (V_{t1}) and holding voltage (V_h) of ESD protection device must be lower than the gate-oxide breakdown voltage of MOSFET to prevent the internal circuits from damage before the ESD protection device is turned on during ESD stresses. Second, the trigger voltage

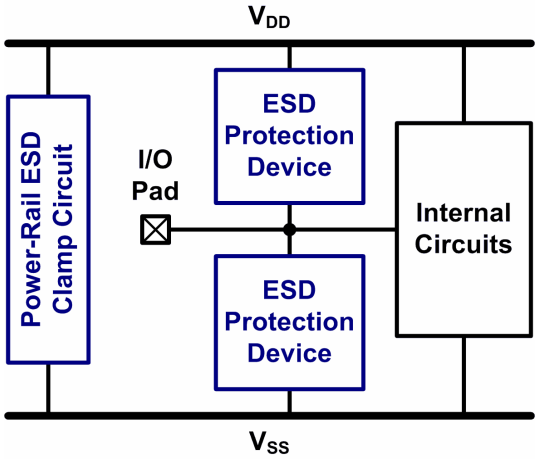

Fig. 1 Whole-chip ESD protection against ESD damages.

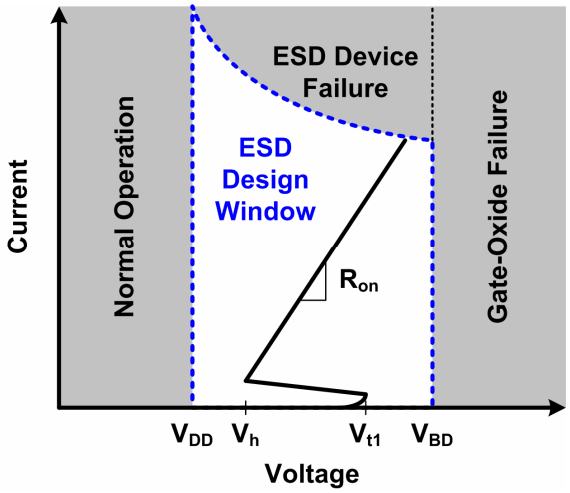

Fig. 2 ESD design window defined by the power-supply voltage (V_{DD}) of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage (V_{BD}) of the MOSFET.

and holding voltage of the ESD protection device must be higher than the power-supply voltage of the IC to prevent the ESD protection devices from being mis-triggered under normal circuit operating conditions. Moreover, the turn-on resistance (R_{on}) of ESD protection device should be minimized to reduce the joule heat generated in the ESD protection device and the clamping voltage of the ESD protection device during ESD stresses. As CMOS technology is continuously scaling down, the gate oxide becomes thinner, which leads to the reduced gate-oxide breakdown voltage of MOSFET. Typically, the gate-oxide

breakdown voltage is decreased to only ~5 V in a 65-nm CMOS process with gate-oxide thickness of ~20 Å. As a result, the ESD design window becomes much narrower in nanoscale CMOS technologies. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharging paths in time.

B. *Area Efficiency*

The scaling-down feature sizes in nanoscale CMOS technologies are expected to improve the area efficiency. However, ESD robustness of IC product needs to be maintained, so the device dimensions of ESD protection devices can not be shrunk. Therefore, the ESD protection devices with higher ESD robustness and smaller layout area are needed in nanoscale CMOS technologies. Besides the MOSFET, more ESD protection devices, such as the silicon-controlled rectifier (SCR) [3], may be more useful in nanoscale CMOS technologies.

The device structure of the SCR is illustrated in Fig. 3. The V_{DD} pad is connected to the first P+ and the pickup N+, which is formed in the N-well. The V_{SS} pad is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The trigger port is connected to the third P+, which is formed in the same P-well. The SCR path between V_{DD} and V_{SS} consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between V_{SS} and V_{DD} consists of P-well and N-well. The equivalent circuit of the SCR consists of a PNP BJT (Q_{PNP}) and a NPN BJT (Q_{NPN}), as shown in Fig. 3. The Q_{PNP} is formed by the P+, N-well, and P-well, and the Q_{NPN} is formed by the N-well, P-well, and N+. As ESD zapping from V_{DD} to V_{SS}, the positive-feedback regenerative mechanism of Q_{PNP} and Q_{NPN} results in the SCR device highly conductive to make SCR very robust against ESD stresses. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of SCR device, the trigger signal can be sent into the base terminal of Q_{NPN} to enhance the turn-on speed. The voltage level of trigger port is in reverse proportion to the trigger voltage of SCR device.

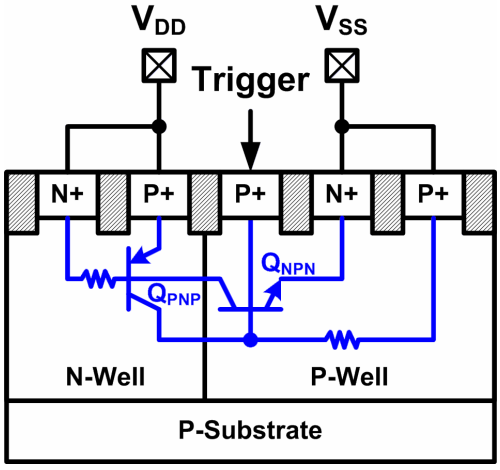

Fig. 3 Device cross-sectional view and equivalent circuit of SCR device.

C. *Leakage Current*

The gate leakage issues exist in the nanoscale technologies which are currently used in production without metal gate structure. The power-rail ESD clamp circuit to effectively protect the internal circuits is traditionally implemented by RC-inverter-triggered NMOS, as shown in Fig. 4 [2]. However, the gate leakage current caused from the large-sized MOS capacitor in the traditional power-rail ESD clamp circuit becomes serious in nanoscale CMOS processes. For example, the gate leakage current flowing through a MOS capacitor with 10 pF under 1-V bias is ~0.2 mA in a 65-nm CMOS process. With such a leakage current in the MOS capacitor, the ESD clamp device (NMOS) with 2000-μm channel width cannot be completely turned off under normal circuit operating conditions, which induces extra large leakage current. The total leakage current of the power-rail ESD clamp circuit is as large as ~0.6 mA in a 65-nm CMOS process. The more serious leakage issue may be found in a sub-50nm CMOS process. Such a leaky power-rail ESD clamp circuit is barely tolerable in IC products with low power requirements.

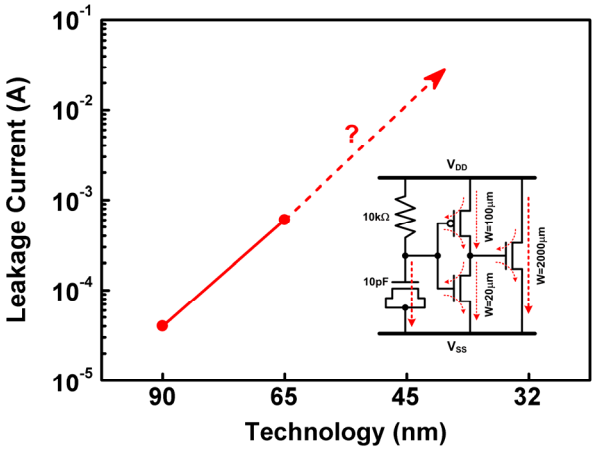

Fig. 4 Estimated leakage current of power-rail ESD clamp circuit in different technology nodes.

To solve the problem of leakage current, some new low-leakage power-rail ESD clamp circuits are proposed, as shown in Figs. 5(a) [4], 5(b) [5], and 5(c), [6]. These SCR-based designs can sustain high ESD level within small silicon area. These designs have been verified in 65-nm CMOS technologies.

In the design of Fig. 5(a), the diode-connected PMOS transistors are used to reduce the voltage across the MOS capacitor. The static current through diode-connected PMOS transistors can be reduced by increasing their channel lengths and number of the stacked PMOS transistors. With enough diode-connected PMOS transistors stacked between V_{DD} and V_{SS}, the voltage across the MOS capacitor can be decreased to reduce the leakage current. As a result, the leakage current of the ESD detection circuit is effectively reduced. The SCR is used instead of the large-sized NMOS as the ESD clamp device. During ESD stresses, due to its

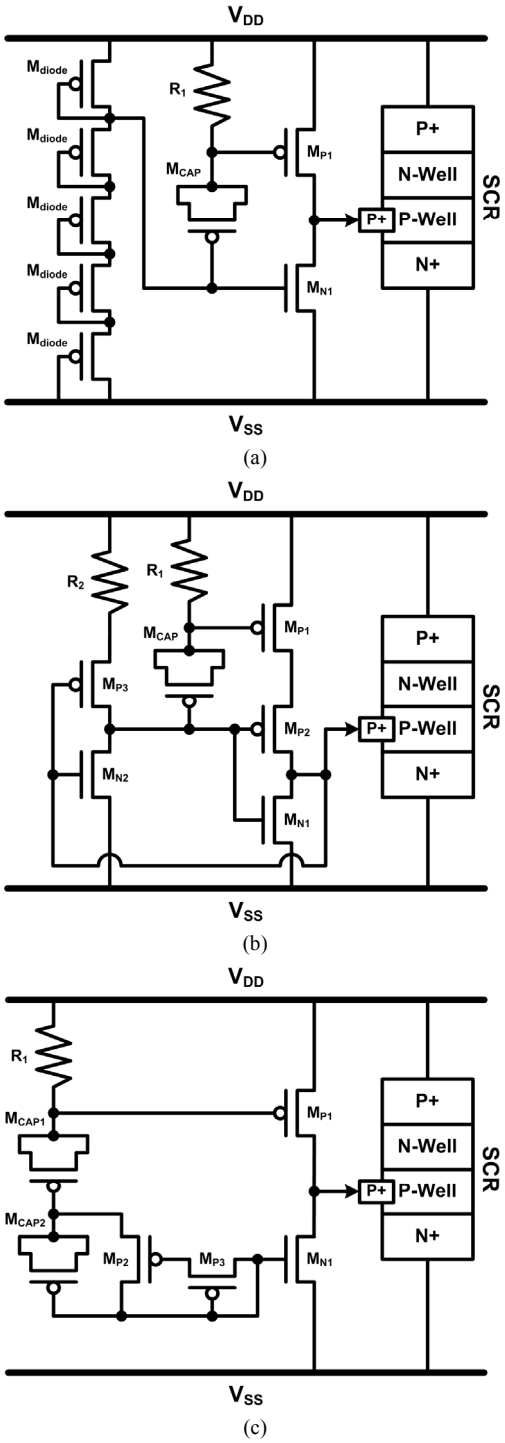

Fig. 5 Power-rail ESD clamp circuits with low-leakage designs.

fast rise time (in the order of nanosecond), the trigger current is injected to turn on the SCR device. This design has 228-nA leakage current at 25 °C in the silicon chip, and it can sustain over 8-kV HBM ESD tests.

In the design of Fig. 5(b), the RC-based ESD detection circuit and the feedback control inverter are combined. Because the MOS capacitor is not directly connected to V_{SS}, no direct leakage path is formed through the large-sized MOS capacitor to ground under normal circuit operating conditions. Besides, there is no voltage drop across MOS capacitor. Without voltage drop across the MOS capacitor under normal circuit operating conditions, the leakage current can be reduced. The measured leakage current of this power-rail ESD clamp circuit is 116 nA at 25 °C. When ESD is zapping to V_{DD} with V_{SS} grounded, the trigger current is injected to turn on the SCR device. This power-rail ESD clamp circuit can achieve the ESD robustness of over 8 kV in HBM.

In the design of Fig. 5(c), the circuit design technique was used to reduce the voltage drop across the MOS capacitors and to minimize the gate leakage current through the MOS capacitors. Under normal circuit operating conditions, the trigger node kept grounded. Without using a feedback network to reduce the device dimension of MOS capacitor, the low-leakage power-rail ESD clamp circuit has only 96-nA leakage current at 25 °C in the silicon chip. When a positive fast-transient ESD voltage is applied to V_{DD} with V_{SS} grounded, the SCR device can be quickly turned on. Verified in the silicon chip, this design can achieve 7-kV HBM ESD robustness.

D. High-Voltage Tolerance

To communicate with other ICs in the microelectronic systems or subsystem, the I/O buffers with low-voltage (1-V) devices will drive or receive high-voltage (1.8-V/2.5-V/3.3-V) signals. Therefore, the I/O buffers must be designed with the consideration of high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of the devices in I/O buffers. To avoid this gate-oxide reliability issue without using additional thick gate-oxide devices, the stacked NMOS configuration has been widely used in the mixed-voltage I/O buffers. With the low-leakage consideration in nanoscale CMOS processes, the new high-voltage-tolerant ESD clamp circuits by using only low-voltage devices have been presented, as shown in Figs. 6(a) [7] and 6(b) [8].

In the design of Fig. 6(a), the $2\times V_{DD}$-tolerant low-leakage ESD clamp circuit is composed of ESD detection circuit and the SCR device as ESD clamp device. The SCR device without poly gate structure has good immunity against the gate leakage problem. The ESD detection circuit with only $1\times V_{DD}$ thin gate-oxide devices was designed with consideration of the gate current and gate-oxide reliability. By utilizing the gate current to bias the ESD detection circuit and optimizing the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor during the normal circuit operating condition can be reduced. The total leakage current, which is resulted from the MOS capacitor, in the ESD detection circuit can be minimized. Therefore, the leakage currents through the ESD clamp device (SCR) and the ESD detection circuit can be well controlled and minimized by this design. This circuit has successfully been verified in a 1-V 65-nm CMOS process, which can achieve 6.5-kV HBM ESD levels under ESD stresses, but only consumes a standby leakage current of 150-nA at 25 °C under normal circuit operating conditions with 1.8-V bias.

In the design of Fig. 6(b), the main ESD current discharging path consists of the SCR with a diode in series. The SCR with diode has high enough holding voltage to prevent from latchup issue [9]. Besides, the SCR device and the forward-biased diode can sustain high ESD level within a small silicon area in CMOS process. With 2-V $2\times V_{DD}$ and grounded V_{SS}, all low voltage transistors sustain only 1 V. Therefore, all low voltage transistors prevent from gate-oxide overstress issue. The total leakage current is only 170-nA at 25 °C. The HBM ESD robustness of this fabricated ESD clamp circuit was 4.8-kV in HBM.

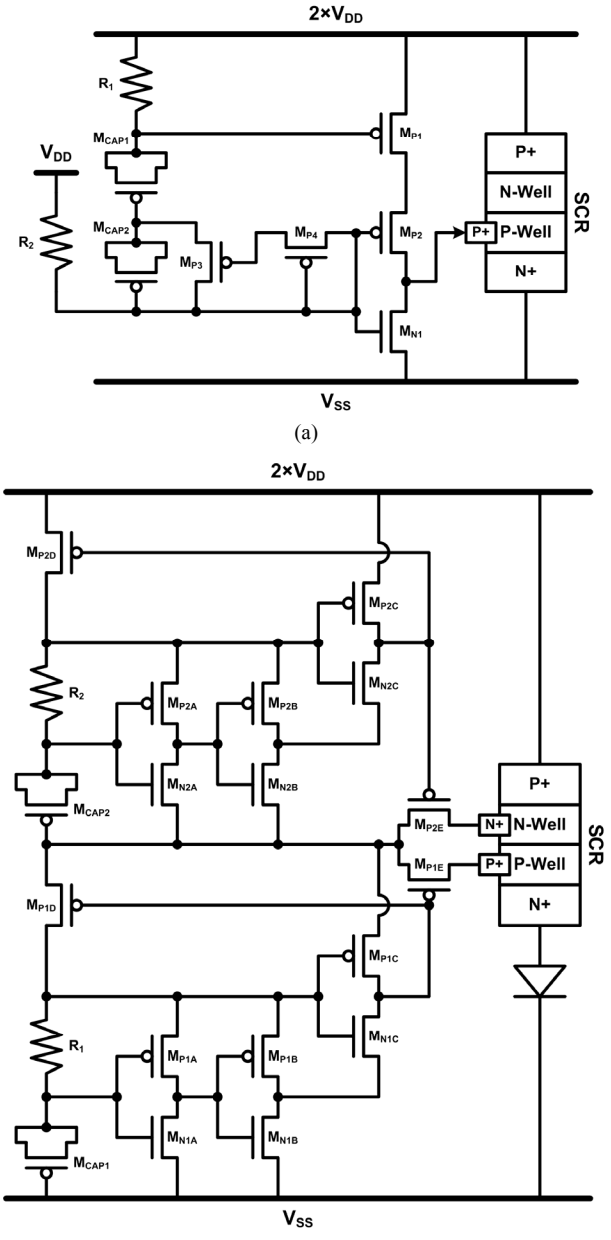

Fig. 6 High-voltage-tolerant power-rail ESD clamp circuits with low-leakage designs.

III. Conclusion

The ESD protection considerations in nanoscale CMOS technologies, including ESD design window, area efficiency, leakage current, and high-voltage tolerance, are presented in this paper. Some solutions against these issues with low-leakage designs in nanoscale CMOS technologies are also presented. The circuit techniques reviewed in this work can successfully reduce the leakage current of the power-rail ESD clamp circuit without significant area overhead, and without decreasing the ESD robustness. As CMOS technologies continuously scaled down, the on-chip ESD protection designs will still be an important design task.

Acknowledgements

This work was partially supported by National Science Council (NSC), Taiwan, under Contract of NSC 99-2220-E-009-021 and Contract of NSC 98-2221-E-009-113-MY2; by Ministry of Economic Affairs, Taiwan, under Grant 99-EC-17-A-01-S1-104; and by the "Aim for the Top University Plan" of National Chiao-Tung University and Ministry of Education, Taiwan.

References

[1] C. Duvvury, "ESD qualification changes for 45nm and beyond," in *IEEE Int. Electron Devices Meeting Dig. Tech. Papers*, 2008, pp. 337-340.

[2] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173-183, Jan. 1999.

[3] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device and Materials Reliability*, vol. 5, no. 2, pp. 235-249, Jun. 2005.

[4] M.-D. Ker, P.-Y. Chiu, F.-Y. Tsai, and Y.-J. Chang, "On the design of power-rail ESD clamp circuit with consideration of gate leakage current in 65-nm low-voltage CMOS process," in *Proc. IEEE Int. Circuits and Systems Symp.*, 2009, pp. 2281-2284.

[5] P.-Y. Chiu, M.-D. Ker, F.-Y. Tsai, and Y.-J. Chang, "Ultra-low-leakage power-rail ESD clamp circuit in nanoscale low-voltage CMOS process," in *Proc. IEEE Int. Reliability Physics Symp.*, 2009, pp. 750-753.

[6] C.-T. Wang and M.-D. Ker, "Design of power-rail ESD clamp circuit with ultra-low standby leakage current in nanoscale CMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 956-964, Mar. 2009.

[7] C.-T. Wang and M.-D. Ker, "Design of 2×VDD-tolerant power-rail ESD clamp circuit with consideration of gate leakage current in 65-nm CMOS technology," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1460-1465, Jun. 2010.

[8] M.-D. Ker and C.-Y. Lin, "High-voltage-tolerant ESD clamp circuit with low standby leakage in nanoscale CMOS process," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1636-1641, Jul. 2010.

[9] M.-D. Ker and W.-Y. Lo, "Design on the low-leakage diode string for using in the power-rail ESD clamp circuits in a 0.35-μm silicide CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 601-611, Apr. 2000.