P-49: Design of Digital Time-Modulation Pixel Memory Circuit on Glass Substrate for Low Power Application

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Abstract

A digital time-modulation pixel memory circuit on glass substrate has been designed and verified in a 3-μm low temperature poly-silicon (LTPS) technology. The proposed circuit can generate 4-bit digital codes and the corresponding inversion data by time-modulation technique to refresh the static image without activating the data driver circuit. Therefore, the data driver of liquid crystal display (LCD) panel is not required to provide the image data of the frame by the proposed circuit while the LCD panel operates in the still mode. The power consumption from data driver can be further reduced in the LCD panel.

1. Introduction

The market for mobile system-on-panel (SOP) LCDs has been rapidly expanding due to the features of high resolution, small size, low power, and high reliability in LTPS technology [1], [2]. Some practical implementation of SOP LCDs had been developed for the mobile phone display with 2.2- to 2.4-inch QVGA resolution [3], [4]. The power consumption of SOP driver circuit tends to be higher than that of silicon ICs because poly-Si TFTs are fabricated with larger design rules, higher threshold voltages, and lower mobility. Therefore, power reduction in SOP LCD circuit is one of the major challenges to expand the mobile SOP-LCD market further.

Recently, memory-in-pixel (MIP) circuit has attracted lots of interests for low-power application. By MIP circuit, polarity inversion can be easily produced even though the data is no longer provided. The prior MIP designs are based on digital memory circuits, which take digital data to display the gray levels on the pixel with SRAM, DRAM, or capacitors [5]. Although these digital memory circuits can produce the normal frame data and reach the polarity inversion easily, the resolution and image quality of display are limited by the number of bits in the digital memory circuit. On the contrary, there is analog memory using storage capacitors and driving transistors to operate the normal and inversion voltages for panel applications [6].

In this work, a 4-bit digital time-modulation pixel memory realized with the TFTs on glass substrate has been proposed and successfully verified in a 3-μm LTPS process. The proposed pixel memory is composed of one DRAM, one latch, and two control switches accompanied with the time-modulation digital data to display different gray levels on panel.

2. Traditional Pixel Memory

The LCD frame displays can be separated into the normal mode and the still mode. The normal mode shows the continuous frame of LCD, and the still mode shows the static frame on the LCD. Fig. 1 shows the block of LCD panel which contains the display panel, data driver, scanning driver, and the embedded pixel memory circuit. The embedded pixel memory is utilized to drive LCD by only the pixel itself when displaying a still image, which means that no additional charging current of the data driver is required in the still mode [7]. In [8], the power consumption of the LTPS TFT LCDs for portable electronic equipments was reduced through lowering the operating frequency of LCD panel for low power consumption in the still mode. The embedded memory circuits with LTPS TFTs in the pixel can display the still image without driving the data line from the data driver.

There are two types of memory to memorize the data for displaying the still image in the pixel. One is the dynamic memory, and the other is the static memory, as shown in Fig. 2 [7]. In Fig. 2(a), since the digital memory stores digital data (high or low voltage levels), the pixel can display only black or white to show 1-bit RGB image in the still mode. Fig. 2(b) shows the timing chart of such a pixel with 1-bit digital memory from normal mode to still mode. At the normal mode, SPOLA and SPOLB are low and this pixel is driven as the conventional pixel. In the pre-still mode, digital memory becomes active to read and memorize the data. Then, data driver and gate driver are turned off, and pixel is driven by the data stored in the digital memory in the still mode. When the memory circuit provides the normal frame data, SPOLA is high, SPOLB is low, and counter electrode is at low voltage level. When the memory circuit provides the corresponding inversion frame data, SPOLA is low, SPOLB is high, and counter electrode is at high voltage level. Therefore, data driver of LCD panel is not required to operate in the still mode, and only little power is consumed to drive the control signals (SPOLA and SPOLB).

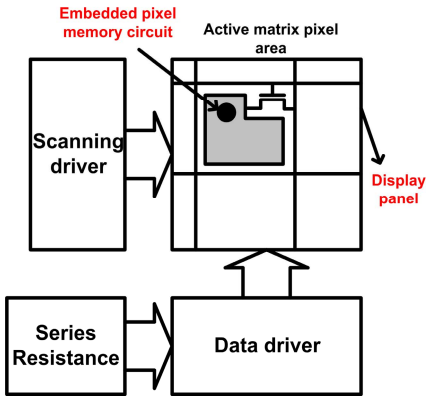


Figure 1. Block of LCD panel on glass substrate with embedded pixel memory circuit.

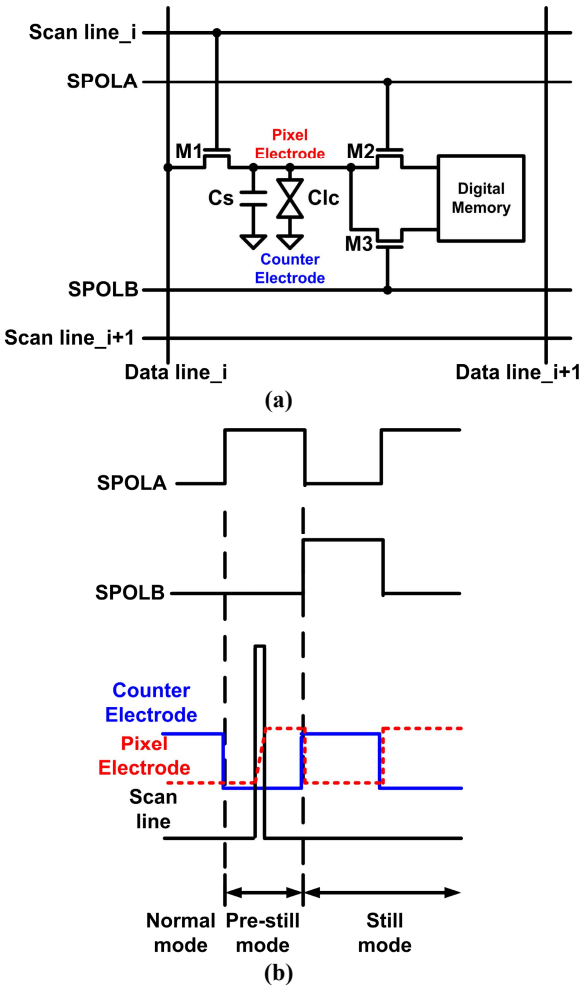


Figure 2. (a) Schematic diagram of static memory in pixel and (b) the timing chart of operations from normal mode to still mode [7].

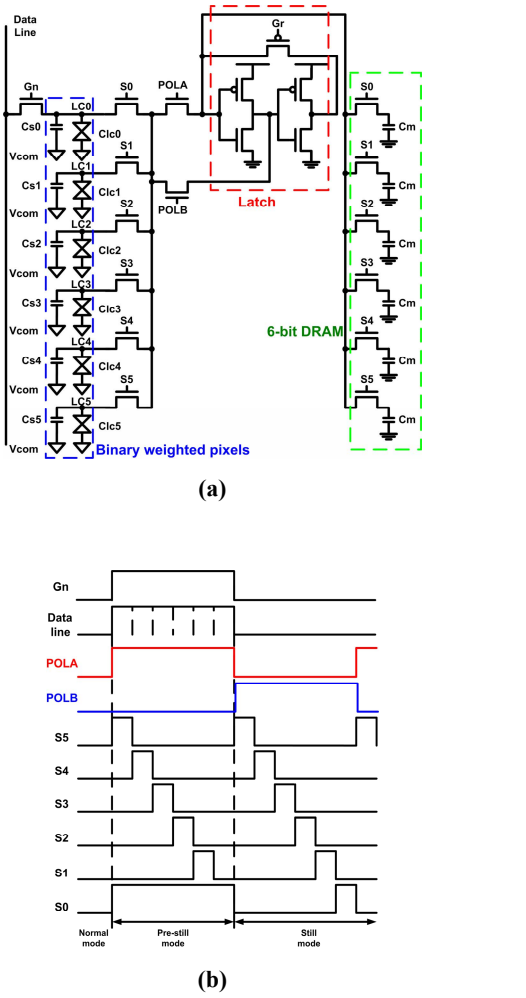


Figure 3. (a) Schematic diagram of area-modulation pixel memory and (b) the corresponding time diagram of control signals [8].

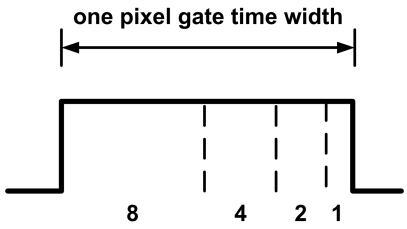
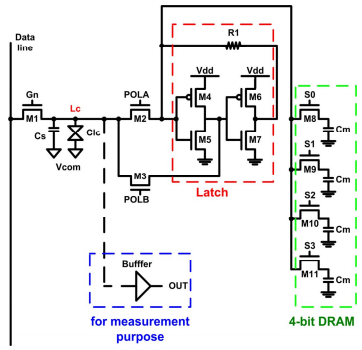


Figure 4. Time width dividing for time-modulation technique.

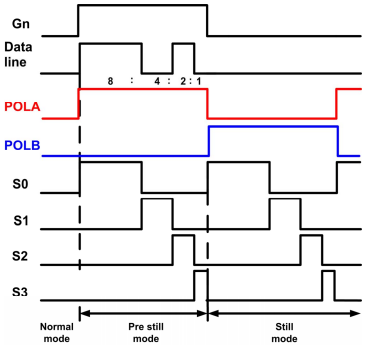
On the contrary, Fig. 3(a) shows the schematic diagram of a 6-bit area coverage modulation pixel memory, which contains one latch, a 6-bit DRAM, and binary weighted pixels. Fig. 3(b) shows the time diagram of the corresponding control signals. In Fig. 3(a), the pixel is divided into six parts, Clc0~Clc5, in a binary weighted way. So, the total area of original pixel is divided into Clc0~Clc5 with the ratio of 32:16:8:4:2:1. At the normal mode, POLA and POLB are low and this pixel is driven as conventional pixel. In the pre-still mode, the 6-bit DRAM is programmed to memorize data from data line. S0~S5 turns on in turns to store the corresponding digital data into the 6-bit DRAM. Then, in the still mode, data driver and gate driver are turned off, and pixel is driven by the digital data stored in the 6-bit DRAM. When the 6-bit DRAM provides the normal frame data, POLA is high, and POLB is low. Furthermore, when the 6-bit DRAM provides the corresponding inversion frame data, SPOLA is low, and SPOLB is high. S0~S5, POLA, and POLB are alternated to reverse the voltage polarity applied at the pixel electrodes (LC0~LC5) in every frame time. By this area coverage modulation, the LCD panel consumes a little power in still mode because data diver circuit does not require to send the same data to the pixel.

3. Proposed Digital Time-Modulation Pixel Memory Circuit

There are two methods for digital pixel memory to mix different gray levels. One is the aforementioned area coverage modulation, which shows gray levels by displaying white and black on different area coverage of pixel. The other method is with time-modulation technique. In a fixed time period, the desired gray levels can be displayed by applying high or low logical voltage on the pixel in different time widths [9]. Fig. 4 illustrates the dividing time width for time-modulation technique. For a 4-bit



(a)



(b)

Figure 5. (a) Schematic diagram of time-modulation digital pixel memory and (b) the corresponding time diagram of the control signals.

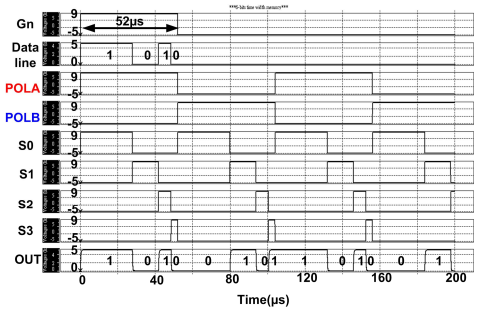


Figure 6. The simulated result of the digital time-modulation pixel memory circuit.

time-modulation, a fixed time period, which is the one pixel gate time width, is divided into the binary weighted ratio of 8:4:2:1. By deciding the pixel white or black for each binary weighted time width to provide high or low voltage level in these time periods, the pixel can mix different time widths to display the desired gray levels.

Fig. 5(a) shows the schematic diagram of the proposed 4-bit digital time-modulation pixel memory which contains a latch (M4, M5, M6, M7, and R1), a 4-bit DRAM (M8, M9, M10, M11, and Cm), and two controlling switches (M2, M3) to decide whether to select inversion data or not. Compared to the area coverage modulation, the proposed circuit does not have to divide the pixel into several parts, so the aperture for the LCD panel can be increased. Fig. 5(b) shows the control signal for this time-modulation design. In the normal mode, M2 and M3 are off so that the LCD panel works as the original pixel circuit. In the pre-still mode, the corresponding digital value for each time interval are stored into 4-bit DRAM with M2 on, M3 off, and S0~S3 goes high in turns. In the still mode, M1 is off and the pixel memory circuit can produce the time-modulation digital signal at the LC node without data providing from driver circuit. When the normal frame data is applied, M2 will turn on and M3 will turn off. When the corresponding inversion data is needed, M3 will turn on and M2 will turn off, the corresponding digital value will produce an inverting value at the node LC through one inverter (M4, M5). By turning M2 and M3 on in turns, the pixel memory circuit can do inversion without reading the data from driver circuit.

Considering the parasitic capacitor in the experimental measurement, a buffer is added to LC node. Such a buffer is especially drawn in the test panel to verify the function of the proposed time-modulation design. In real panel application, the pixel does not need this buffer. A test pattern and its simulation timing chart are shown in Fig. 6. The controlling signal of Gn, POLA, POLB, and S0~S3 are set as -5V to 9V to make sure all TFT switches fully turn on and off. The test pattern is given as "1010" with binary weighted ratio of 8:4:2:1 for 4-bit time-modulation on data line and its voltage range is from 0V to 5V. Since one frame time for 2.8 inch QVGA is 16.7ms, the time width of Gn is 16.7ms/320=52µs, and the duty cycle of S0:S1:S2:S3 is 8:4:2:1 with Vdd of 5V, Vss of 0V, Clc + Cs of 300fF, and Cm of 600fF. In Fig. 6, Gn is high, so the data "1010" from data line is directly delivered to the OUT node in the pre-still mode. Besides, the corresponding digital value for each time interval are stored into 4-bit DRAM as M2 is on and S0~S3 goes high in turns. When Gn is low, the pixel memory is operated in the still mode. "0101" is shown in OUT node when M3 is on, which means the inversion data has been produced by the proposed circuit successfully. Through such a simulation, the operation of the proposed time-modulation circuit can be verified.

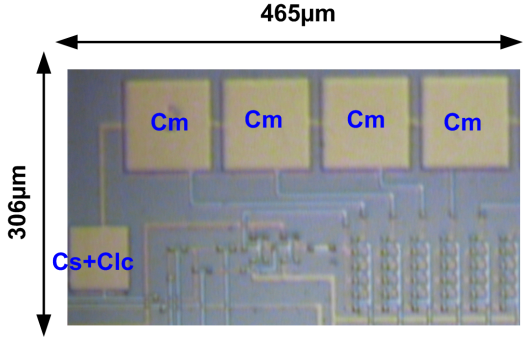


Figure 7. Photo of the fabricated 4-bit time-modulation digital pixel memory in a 3-µm LTPS technology.

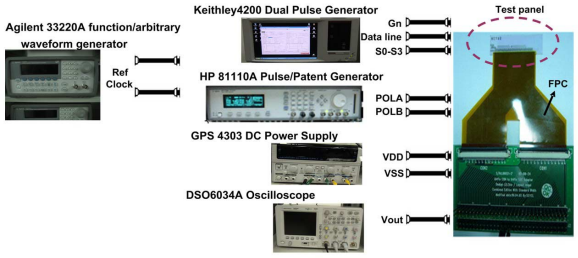


Figure 8. The measurement setup to verify the fabricated pixel memory.

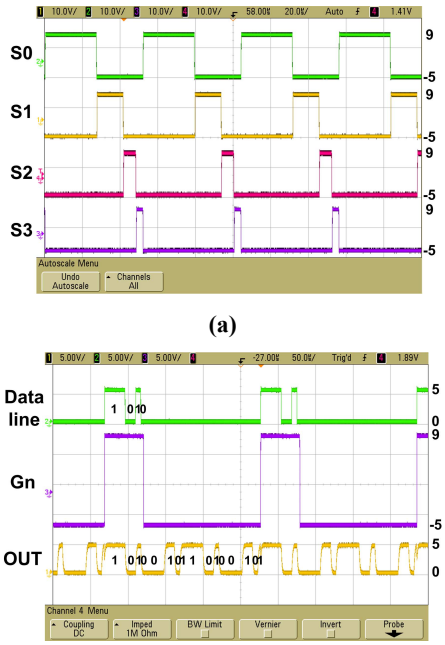


Figure 9. Measured voltage waveforms of the 4-bit time-modulation digital pixel memory with the signal operations at (a) S0, S1, S2, and S3, and (b) data line, Gn, and OUT. The operating data code demonstrated in this measurement is '1010'.

4. Experimental Results

The proposed 4-bit time-modulation digital pixel memory circuit has been fabricated on glass substrate in a 3-μm LTPS technology. The photo of the fabricated pixel memory circuit is shown in Fig. 7 with the size of 306μm×465μm in a test panel. The capacitors, Clc, Cs, and Cm, utilized in the proposed circuit are implemented by the metal-insulator-metal between M1 and M2. The equivalent capacitance of Clc and Cs is 0.3pF, as well as the capacitance of Cm is 0.6pF. To observe the operations of the proposed time-modulation pixel memory circuit with the parasitic loading capacitance (about 10pF), a buffer is added to the LC node for measurement purpose.

The measurement setup is shown in Fig. 8. Keithley4200 Dual Pulse Generator is used to produce Gn, data signal, and S0-S3, which are set 9V to -5V. A pulse/pattern generator (Agilent 81110A) provides a pair of non-overlapping clock signals, POLA and POLB. To synchronize 81110A and Keithley4200, a reference clock generated by another function/arbitrary waveform generator (Agilent 33220A 20MHz) is utilized. Digital oscilloscope DSO6034A is utilized to observe the output waveforms.

The measurement result of 4-bit digital time-modulation pixel memory is shown in Fig. 9. Fig. 9 (a) shows the operating voltage waveforms on the signals of S0, S1, S2, and S3. In order to follow the concept of time modulation, the duty cycle of S0:S1:S2:S3 is 8:4:2:1. When Gn is on, data line produces the test pattern "1010" in Fig. 9 (b). Fig. 9 (b) shows the measured voltage waveforms of the proposed circuit for Gn, data line, and OUT. The pixel memory circuit can provide the data and corresponding inversion data on LC node by itself. Since data line produces "1010" as Gn is on, OUT shows "0101" and "1010" alternatively as Gn is off.

5. Conclusion

A 4-bit digital time-modulation digital pixel memory on glass substrate for panel integration has been successfully designed and fabricated in a 3-μm LTPS technology. A time-modulation digital pixel memory is formed with a 4-bit DRAM, latch, and control switches to produce time-modulation data and its corresponding inversion data. This pixel memory circuit can provide frame data and its corresponding inversion data to refresh the static image without operating data driver circuit, which enables the feature of LCD panel to lower power consumption in the still mode.

6. Acknowledgment

The authors would like to thank the support of test circuit fabrication on on-glass substrate from AU Optronics Corporation, Hsinchu, Taiwan, partially supported by "Aim for the Top University Plan" of the National Chiao-Tung University and Ministry of Education Taiwan, R.O.C., and partially supported by National Science Council (NSC), Taiwan, under contract of NSC 98-2221-E-009-113-MY2.

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