Layout Styles to Improve CDM ESD Robustness of Integrated Circuits in 65-nm CMOS Process

Ming-Dou Ker[1,2], Chun-Yu Lin[1], and Tang-Long Chang[1]

[1] Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
[2] Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan.

Abstract – Due to the thinner gate oxide in the nanoscale CMOS technology and the larger chip size in the system-on-chip (SoC) IC products, the charged-device-model (CDM) electrostatic discharge (ESD) has become the major ESD events to cause failures during IC manufacturing procedures. The effective ESD protection design against CDM ESD stresses should be implemented into the chip with layout optimization to improve its ESD robustness. In this work, the impacts of different layout styles of MOS devices on CDM ESD robustness were investigated in a 65-nm CMOS process. The experimental results can provide useful information to optimize the layout of integrated circuits against CDM ESD events.

I. Introduction

In order to be safely used and to provide moderate life time, all microelectronic products must meet the reliability specifications during mass production and applications. Electrostatic discharge (ESD), which was one of the most important reliability issues to the integrated circuit (IC) products, must be taken into consideration during the design phase of all IC products [1]-[3]. All pads which connect the circuits in the chip to the external nodes, including the input/output (I/O) pads, V_{DD} pads, and V_{SS} pads, must be equipped with ESD devices to provide effective ESD protection for the IC.

Among the three chip-level ESD test standards, which are human-body model (HBM), machine model (MM), and charged-device model (CDM), the CDM ESD events play major roles to cause failures in today's manufacturing and packaging environments [4], [5]. The CDM ESD event happens when a certain pin of the IC is suddenly grounded, and the electrostatic charges originally stored in the chip will be discharged through the grounded pin. The CDM ESD events become more and more critical because of the thinner gate oxide in nanoscale CMOS transistors and the larger die size for the applications of system on chip (SoC). The thinner gate oxide causes a lower gate-oxide breakdown voltage, and an IC for SoC application with larger die size often has a larger volume in substrate to store more static charges. The CDM ESD failure was normally located across the gate oxide of MOS devices, as shown in Fig. 1. Although the circuit is equipped with ESD clamp devices at its corresponding I/O pad, it still suffers CDM ESD issues on the gate oxides [6], [7]. Since the CDM ESD event typically has a fast rise time of only ~0.2 ns, the ESD clamp devices may not be efficiently turned on to protect the gate oxide of the internal circuits during CDM ESD events. Additional ESD protection design against CDM ESD stress should be added into the chip which will be fabricated in nanoscale CMOS technology. It has been reported that the layout style has some impact on the CDM robustness [8], [9].

In this work, the impacts of (1) the deep N-well (DNW) layer and (2) the pick-up layout in MOS devices on CDM robustness are investigated through the silicon chip fabricated in a 65-nm CMOS process.

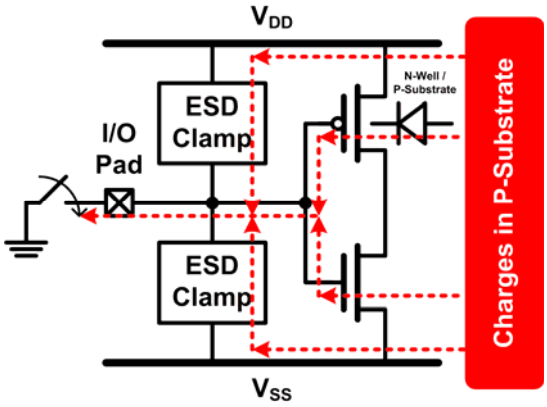


Fig. 1. CDM ESD events occurred at the I/O pad. The CDM charges were initially stored in the substrate of IC chip.

II. Layout of MOS Devices

By adding the DNW layer in ESD clamp or protected devices, the CDM ESD robustness of the input buffer are investigated in this work. One set of N-type test circuits consisting of the gate-grounded NMOS (GGNMOS), the protected NMOS, and the input series resistance (R_{CDM}), are shown in Fig. 2. All GGNMOS drawn with W/L of 180μm/0.09μm are used as the ESD clamp devices. The silicided block technique is used on the drain side of GGNMOS. The protected NMOS with W/L of 20μm/0.09μm is used to simulate the victims under CDM ESD stresses. The DNW are added to GGNMOS of Fig. 2(b) and the protected NMOS of Fig. 2(c). The gate terminal of each protected NMOS is connected to its I/O pad through the R_{CDM}. The test circuits with different R_{CDM} (0.1-, 1-, and 10-kΩ) are implemented to evaluate the CDM ESD robustness. The layout cross-sectional views of the corresponding test circuits in Fig. 2 are shown in Fig. 3. It can be found that the DNW with the assistance of N-well can separate the P-well from the common P-substrate. Under CDM ESD stresses, the charges stored in the stand-along P-well have a much lower amount than those stored in the common P-substrate.

The other set of P-type test circuits consisting of the gate-V_{DD} PMOS (GDPMOS), the protected PMOS, and the R_{CDM}, are shown in Fig. 4. All GDPMOS with W/L of 180μm/0.09μm are used as the ESD clamp devices. The silicided block technique is also used on the drain side of GDPMOS. The protected PMOS with W/L of 20μm/0.09μm is used to simulate the victims under CDM ESD stresses. The DNW are added to GDPMOS of Fig. 4(b) and the protected PMOS of Fig. 4(c). The gate terminal of each protected PMOS is connected to its I/O pad through the R_{CDM}. The test circuits with different R_{CDM} (0.1-, 1-, and 10-kΩ) are implemented to evaluate the CDM ESD robustness. The layout cross-sectional views of the corresponding test circuits in Fig. 4 are shown in Fig. 5.

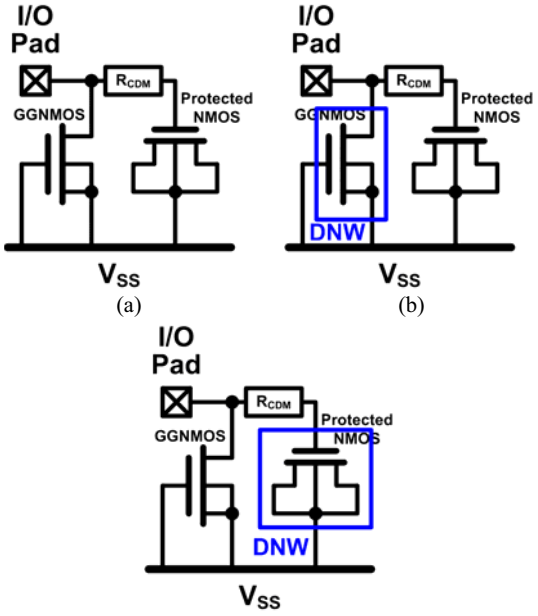


Fig. 2. N-type test circuits (a) without DNW, (b) with DNW in GGNMOS, and (c) with DNW in the protected NMOS.

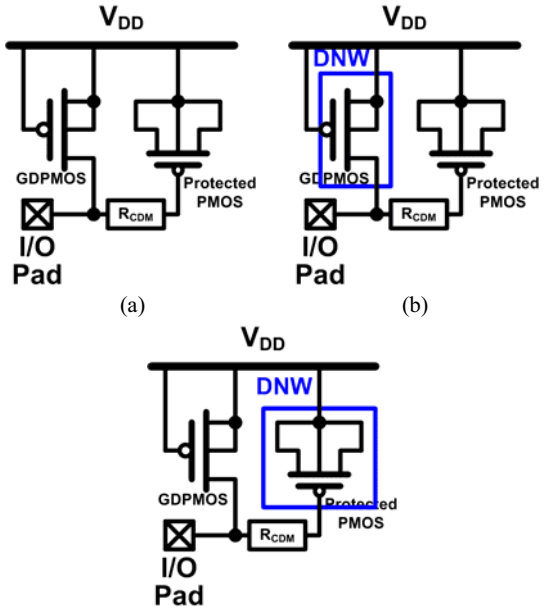


Fig. 4. P-type test circuits (a) without DNW, (b) with DNW in GDPMOS, and (c) with DNW in the protected PMOS.

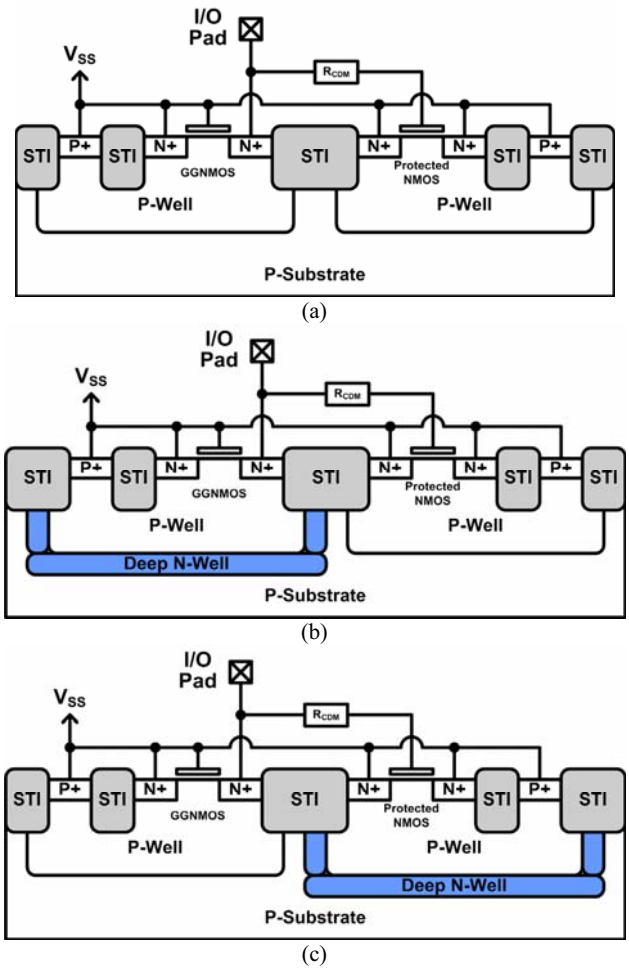


Fig. 3. Cross-sectional view of N-type test circuits (a) without DNW, (b) with DNW in GGNMOS, and (c) with DNW in protected NMOS.

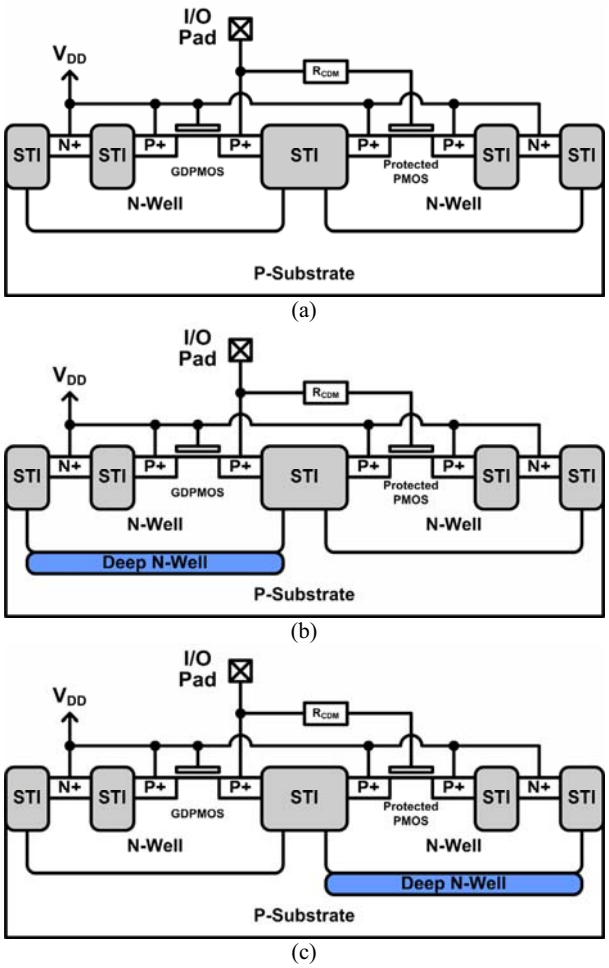
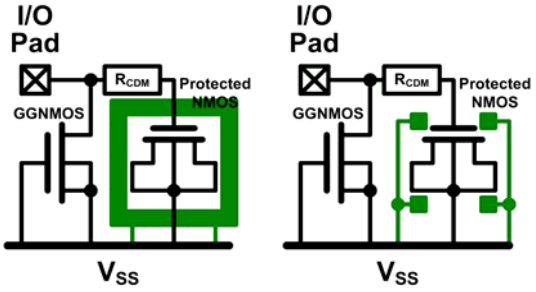
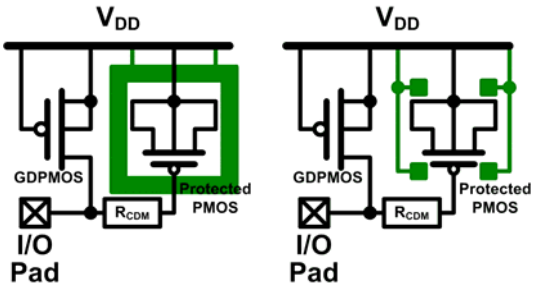


Fig. 5. Cross-sectional view of P-type test circuits (a) without DNW, (b) with DNW in GDPMOS, and (c) with DNW in protected PMOS.



(a) (b)

Fig. 6. N-type test circuits with (a) one P+ guard-ring, and (b) four P+ pick-up, at the protected NMOS.



(a) (b)

Fig. 7. P-type test circuits with (a) one N+ guard-ring, and (b) four N+ pick-up, at the protected PMOS.

The layout styles of body terminals in the protected NMOS and PMOS are also investigated in this work. Figs. 6(a) and 6(b) show the P+ guard-ring surrounded the protected NMOS and four P+ pick-up diffusions at corners of protected NMOS, respectively. Similarly, Figs. 7(a) and 7(b) show the N+ guard-ring surrounded the protected PMOS and four N+ pick-up at corners of protected PMOS, respectively. Besides, the P+ and N+ guard rings are also used to surround the GGNMOS and GDPMOS, respectively, in the layout.

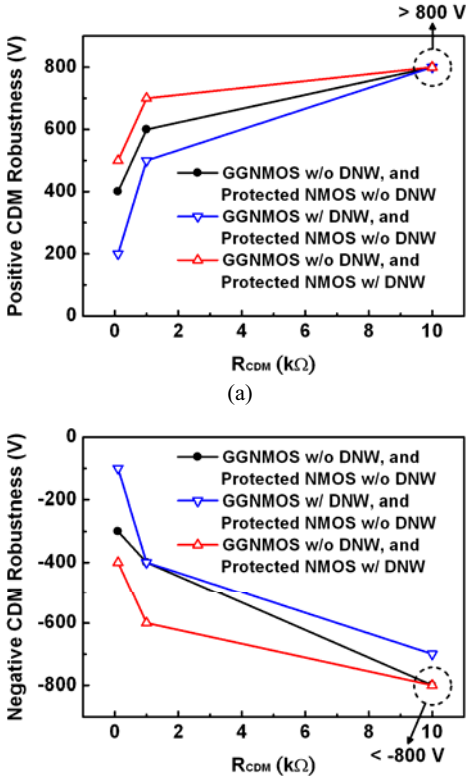
All aforementioned test circuits have been fabricated in a 65-nm CMOS process with the thin-gate oxide of ~20 Å in the core devices.

III. Experimental Results

The test circuits have been assembled in DIP-48-pin package. The CDM ESD stresses are applied by the field-induced CDM tester. The failure criterion is 30% shift of the leakage current under 1-V V_{DD} bias from its original level. The voltage step of CDM ESD stresses to the test circuits is 100 V. The CDM ESD robustness among these test circuits are compared in Figs. 8~11.

As shown in Fig. 8, the protected NMOS surrounded with DNW but the GGNMOS without DNW has the better CDM ESD robustness. The DNW can prevent the protected NMOS from CDM ESD stress because the CDM charges are initially stored in the P-substrate. However, the GGNMOS surrounded with DNW (but the protected NMOS without DNW) will degrade its CDM ESD robustness, because the DNW will limit the charges in P-substrate to directly flow into the P-well of GGNMOS.

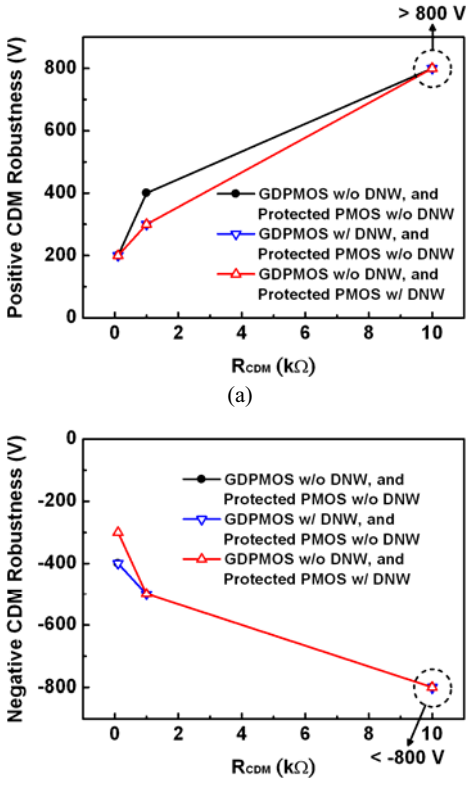
The test circuits of GDPMOS and the protected PMOS with and without the DNW have almost the same CDM ESD robustness, since the DNW in P-type test circuits can not separate the body terminal of PMOS (N-well) from the P-substrate. The DNW under the N-well will increase the amount of charges in the body terminal of PMOS, so the CDM ESD robustness of some P-type test circuits with DNW are little worse than those without DNW.



(a)

(b)

Fig. 8. (a) Positive, and (b) negative, CDM ESD robustness of N-type test circuits with and without DNW.



(a)

(b)

Fig. 9. (a) Positive, and (b) negative, CDM ESD robustness of P-type test circuits with and without DNW.

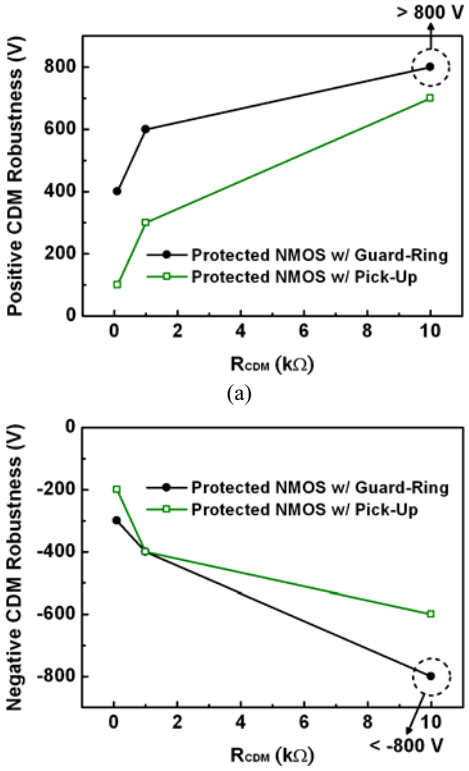


Fig. 10. (a) Positive and (b) negative CDM ESD robustness of N-type test circuits with guard-ring and pick-up.

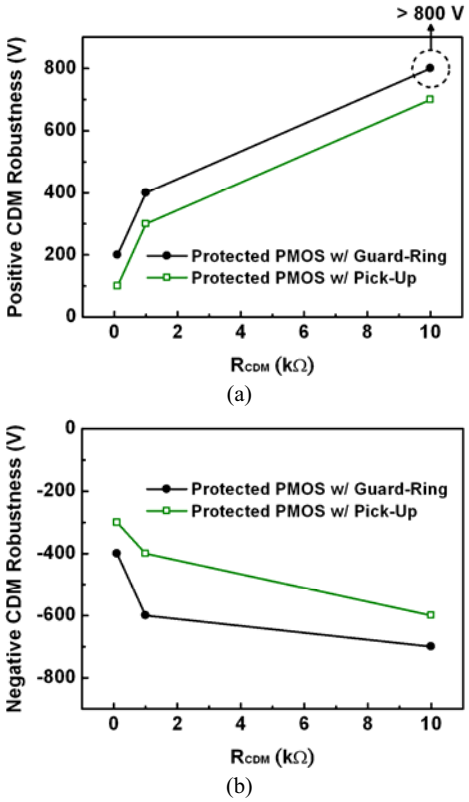


Fig. 11. (a) Positive and (b) negative CDM ESD robustness of P-type test circuits with guard-ring and pick-up.

Figs. 10 and 11 compared the CDM ESD robustness of N-type and P-type test circuits with guard-ring style or pick-up style at their body terminals. From the measured results, the layout with four pick-up diffusions at body terminal on the protected MOS has a lower CDM ESD robustness, because the charges in the P-well (N-well) of the protected NMOS (PMOS) can not be efficiently discharged through the P+ (N+) pick-up to the GGNMOS (GDPMOS) and then to the external ground. The layout style with guard ring on the protected MOS results in a higher CDM ESD robustness. By the way, the CDM ESD robustness can be also increased, when the resistance of R_{CDM} is increased.

IV. Conclusion

The impacts of different layout styles of MOS devices on CDM ESD robustness have been investigated through silicon chip fabricated in a 65-nm CMOS process. Form the experimental results, CDM ESD robustness of NMOS in the input buffer can be improved by realizing the protected NMOS with the DNW. Besides, the CDM ESD robustness of the protected MOS devices with guard-ring layout style can be better than those with only pick-up style. The studied results of this work can help the foundries and/or IC design houses to develop useful ESD design rules for optimizing IC layout against CDM ESD events.

Acknowledgement

This work was partially supported by National Science Council, Taiwan, under Contract NSC 98-2221-E-009-113-MY2, by Ministry of Economic Affairs, Taiwan, under Grant 99-EC-17-A-01-S1-104, and by the "Aim for the Top University Plan" of National Chiao-Tung University and Ministry of Education, Taiwan. The authors would also like to thank TSMC University Shuttle Program for providing chip fabrication.

References

[1] S. Voldman, *ESD: Circuits and Devices*. New York: Wiley, 2006.

[2] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. John Wiley & Sons, 2002.

[3] S.-H. Chen and M.-D. Ker, "Design of on-chip power-rail ESD clamp circuit with ultra-small capacitance to detect ESD transition," in *Proc. International VLSI Design, Automation and Test Symp.*, 2009, pp. 327-330.

[4] A. Righter *et. al.*, "CDM ESD current characterization - package variability effects and comparison to die-level CDM," in *Proc. EOS/ESD Symp.*, 2009, pp. 173-182.

[5] N. Wakai and Y. Kobira, "Consideration for CDM breakdown and reliability designing in the latest semiconductor technology," in *Proc. IEEE Reliability and Maintainability Symp.*, 2009, pp. 509-514.

[6] S.-H. Chen and M.-D. Ker, "Active ESD protection circuit design against charged-device-model ESD event in CMOS integrated circuits," *Microelectronics Reliability*, vol. 47, no. 9-11, pp. 1502-1505, Sep. 2007.

[7] Y. Zhou and J. Hajjar, "CDM ESD failure modes and VFTLP testing for protection evaluation," in *Proc. IEEE International Solid-State and Integrated-Circuit Technology Conf.*, 2008, pp. 333-336.

[8] J. Lee *et. al.*, "The study of sensitive circuit and layout for CDM improvement," in *Proc. IEEE International Physical and Failure Analysis of Integrated Circuits Symp.*, 2009, pp. 228-232.

[9] C.-Y. Lin and M.-D. Ker, "CDM ESD protection design with initial-on concept in nanoscale CMOS process," in *Proc. IEEE International Physical and Failure Analysis of Integrated Circuits Symp.*, 2010, pp. 193-196.