Design of ESD Protection for RF CMOS Power Amplifier with Inductor in Matching Network

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***Abstract*—Due to the potential for mass production, CMOS technologies have been widely used to implement radio-frequency integrated circuits (RF ICs). Electrostatic discharge (ESD), which is one of the most important reliability issues in CMOS technologies, must be considered in RF ICs. In this work, an on-chip ESD protection design for RF power amplifier (PA) was presented. The ESD protection design consisted of an inductor in the matching network of PA. The PA with this ESD protection had been designed and fabricated in a 65-nm CMOS process. The ESD-protected PA can sustain over 4-kV human-body-mode (HBM) ESD stress, while the unprotected PA was degraded after 1-kV HBM ESD stress.**

I. INTRODUCTION

In recent decades, the development of wireless technologies is explosive and rapid. The requirements of wireless products such as smart phones are overwhelming. For the consideration of low cost and high integration, the whole radio-frequency integrated circuits (RF ICs) have been widely fabricated in CMOS processes [1]. Implementing power amplifier (PA) circuits, which play important roles in RF transmitters, in CMOS processes is also an important target. The reliability issues due to the thin gate oxide of the CMOS transistor consequently puzzle RF PA designers. The major reliability issue of CMOS ICs is electrostatic discharge (ESD). As CMOS technology continuously scales down, ESD issues become more serious. Therefore, on-chip ESD protection design must be carefully considered in IC products.

Fig. 1 shows a typical on-chip ESD protection design used in RF ICs [2]. The ESD protection design consists of a power-rail ESD clamp circuit and ESD protection devices. Such ESD protection design has suitable ESD-discharge paths under ESD events and can provide well ESD robustness. Unfortunately, the parasitic effects which ESD protection devices introduce in would cause RF performances degradation. The ESD protection devices are usually designed to have large dimensions in order to sustain large ESD current, but the following are large parasitic capacitances. The parasitic capacitances of ESD protection devices cause power loss and degrade the power gain. Furthermore, the matching conditions of RF ICs are also changed by these parasitic capacitances. The noise coupled through the ESD protection devices undoubtedly degrades the noise figure.

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Improving the RF performance degradation caused by ESD protection devices is an important design consideration, and many methods have been proposed. There are some methods to decrease the parasitic capacitances of ESD protection devices. Connecting diodes in series can efficiently achieve the target [3]. Besides, silicon-controlled rectifier (SCR), which has high ESD level with low parasitic capacitance, is often used [4]. By changing the layout structure of the SCR into another type, such as waffle structure, the parasitic capacitances can be further diminished [4]. Other methods are to use inductors and capacitors to tune out the parasitic capacitances of ESD protection devices. An LC-tank can be used for this purpose [5].

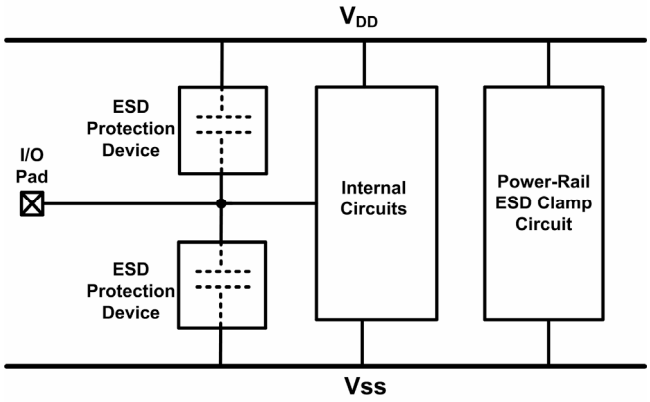

Figure 1. Typical ESD protection design in RF ICs.

However, there are still some challenges while implementing these methods. The most evident problem is that all ESD protection devices are fundamentally "extra" devices to RF ICs. To entirely decrease the parasitic capacitances of ESD protection devices or to entirely tune out the parasitic capacitances are difficult. That is, to entirely eliminate the RF performance degradation caused by ESD protection devices is also difficult. Compared with those methods, merging ESD protection devices into core RF ICs is a proper idea. One method is to combine the ESD protection devices with the matching networks of RF circuits [6].

This paper presents an ESD protection strategy which combines ESD protection circuits with the matching network of a PA. The PA circuits with and without the ESD protection design have been fabricated and verified in a 65-nm CMOS process.

II. Proposed ESD Protection Strategy

To avoid any extra ESD protection devices, the proposed ESD protection strategy utilizes the origin device used in PA. The RF choke inductor between the drain of the output transistor of PA and V_{DD} can be utilized. The architecture of this ESD protection strategy is shown in Fig. 2. Fig. 2 shows a simple structure of a PA with an on-chip RF choke inductor and a power-rail ESD clamp circuit between V_{DD} and V_{SS}. The M_{output} represents the transistor of the output stage of the PA. L_{ESD} is an RF choke inductor used to feed DC power to the PA circuit, which exhibits very low impedance at low frequency, and therefore can also be treated as a low-impedance path for ESD current under ESD events. Since PA is used to deliver large power, the RF choke inductor at the output stage needs to be designed with large metal width so as to sustain large current density. This characteristic is also beneficial to treating the RF choke inductor as an ESD discharge path. In addition, a power-rail ESD clamp circuit is inserted between V_{DD} and V_{SS} to provide ESD paths between the power rails.

The proposed ESD protection strategy can provide ESD discharge paths under every ESD events, including positive-to-V_{SS} (PS) mode, positive-to-V_{DD} (PD) mode, negative-to-V_{SS} (NS) mode, negative-to-V_{DD} (ND) mode, V_{DD}-to-V_{SS} mode, and V_{SS}-to-V_{DD} mode.

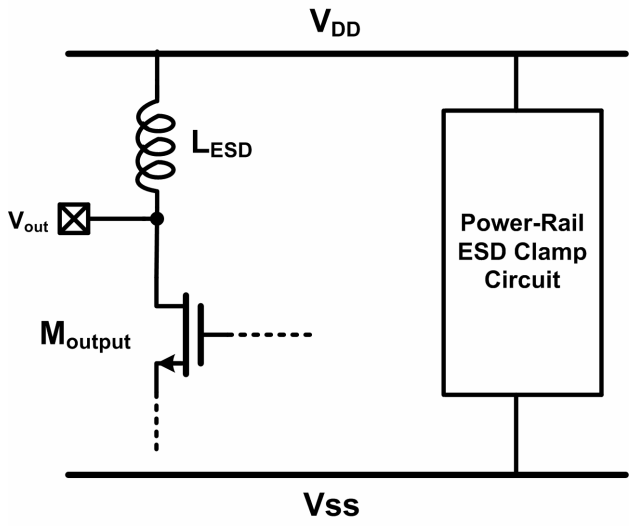

Figure 2. Proposed ESD protection strategy for PA with the inductor L_{ESD} and the power-rail ESD clamp circuit.

III. Implementation of ESD Protection Design

To investigate and verify the ESD protection strategy, the test circuits have been designed and fabricated in a 65-nm CMOS process. The PA is a two-stage class-AB PA with self-biased cascode structure [7]. Fig. 3 shows the schematic circuit of the PA. The metal width of L_{ESD} should be large enough for sustaining high current density under normal operation conditions and discharging ESD current under ESD events.

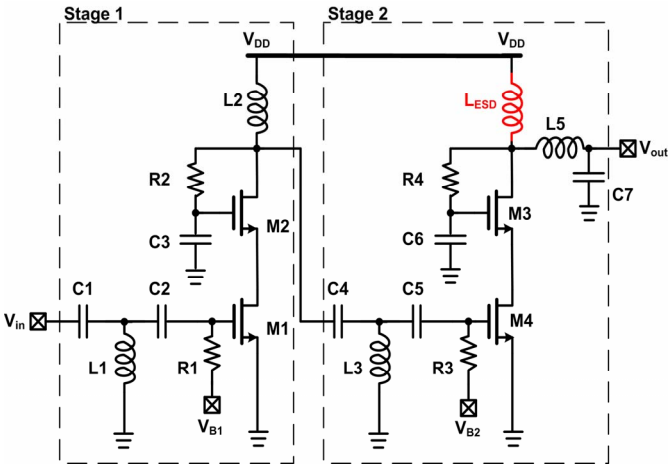

Figure 3. Schematic circuit of class-AB PA.

The power-rail ESD clamp circuit is placed between V_{DD} and V_{SS}, which clamps the V_{DD}-to-V_{SS} overstress and provides ESD discharge paths between V_{DD} and V_{SS} under ESD stress conditions. Fig. 4 shows the used power-rail ESD clamp circuit. The power-rail ESD clamp circuit consists of an ESD detection circuit and a main clamp device. An RC-inverter is utilized to be an ESD detection circuits, and an NMOS (M_{ESD}) with large size is utilized as the main clamp device. The RC-inverter designed with RC time constant on the order of microsecond can distinguish ESD events from normal power-on conditions, and the M_{ESD} should be triggered on in time to provide an ESD discharge path when ESD stress drops across V_{DD} and V_{SS}. Right after ESD events occur, the ESD detection circuit detects ESD events and sends a trigger signal to trigger the main clamp device. The main clamp device is therefore turned on to provide a low-impedance path to discharge ESD current. Besides, the ESD detection circuit has to recognize the normal power-on conditions in order not to mistrigger the main clamp device.

The realization of this ESD protection strategy for PA is shown in Fig. 5. L_{ESD} represents the RF choke inductor at the output stage of the PA circuit with off-chip output matching network. The power-rail ESD clamp circuit consists of the RC-inverter-triggered NMOS. The current discharge paths of PS-mode and NS-mode are shown in Fig. 5(a). For PS-mode, the ESD current first goes through L_{ESD} and then be discharged through the power-rail ESD clamp circuit. For NS-mode, the ESD current is discharged through the power-rail ESD clamp circuit and then goes through L_{ESD}. The current discharge paths of PD-mode and ND-mode are shown in Fig. 5(b). For PD-mode, the ESD current is discharged from the out pad to V_{DD} through L_{ESD}. For ND-mode, the discharge path is in an opposite direction. Fig. 5(c) shows the discharge

paths of V_{DD}-to-V_{SS} mode and V_{SS}-to-V_{DD} mode. For V_{DD}-to-V_{SS} mode, the main clamp device, M_{ESD}, is turned on by the RC-inverter and provide a low-impedance ESD discharge path. For V_{SS}-to-V_{DD} mode, ESD current is discharged through the forward parasitic diode of M_{ESD}.

The ESD protection design merely consists of an on-chip RF choke inductor at the output stage of a PA and a power-rail ESD clamp circuit, and contributes no parasitic capacitances to the RF output. Without extra ESD protection devices at RF output, the design complexity of RF circuit is greatly reduced.

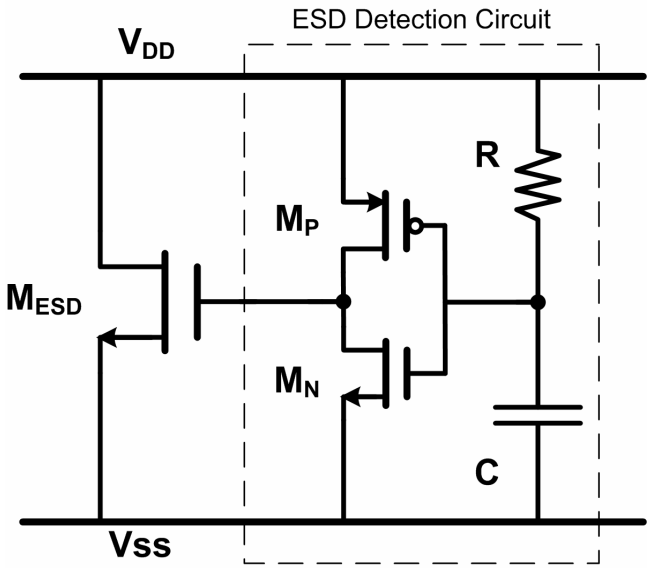

Figure 4. Power-rail ESD clamp circuit.

IV. Measurement Results

PA circuits with and without the on-chip ESD protection inductor, L_{ESD}, have been fabricated in a 65-nm CMOS process. Fig. 6 shows the die photo of the ESD-protected PA. Parts of the output matching network, L5 and C7, are removed from the test chip. Since the MOS transistors in the stage 2 of PA would directly suffer ESD zapping under ESD stress conditions when the inductor L5 was not on-chip, the ESD level of the worst case can be verified. Both kinds of PA chips were zapped by an ESD tester in human-body-mode (HBM). The PS-mode, PD-mode, NS-mode, and ND-mode ESD stresses were applied to the PA output pad. To investigate the ESD robustness, the S-parameters of PAs before and after ESD zapping were compared.

The measured results of RF performance of the unprotected PA are shown in Fig. 7. The S_{21}-parameters of the unprotected PA after 1-kV HBM ESD zapping of the six modes mentioned in Fig. 5 was apparently degraded. This result is far away from the required 2-kV HBM ESD robustness. In contrast, the S_{21}-parameters of the ESD-protected PA after 4-kV HBM ESD zapping of the six modes mentioned above still maintain well, as shown in Fig. 8.

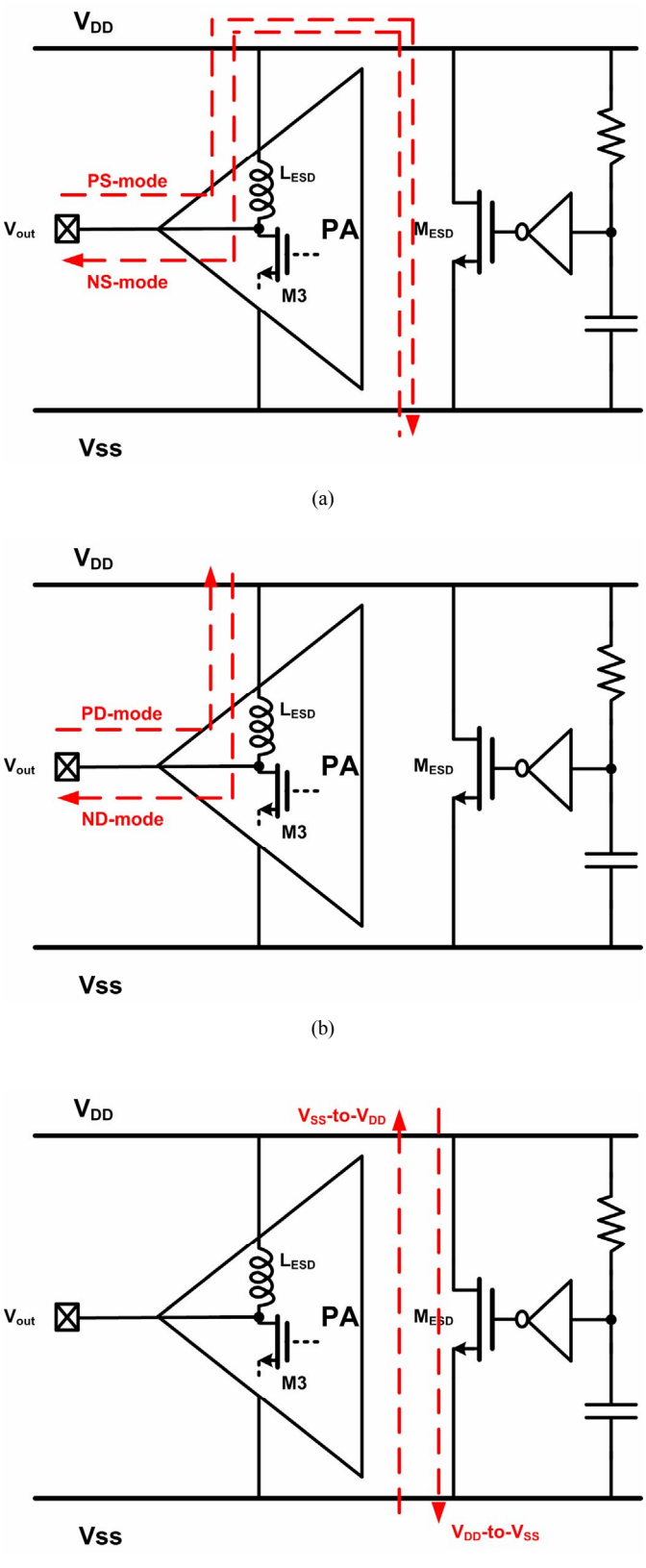

Figure 5. ESD-discharge paths under (a) PS-mode and NS-mode, (b) PD-mode and ND-mode, and (c) V_{DD}-to-V_{SS} mode and V_{SS}-to V_{DD} mode.

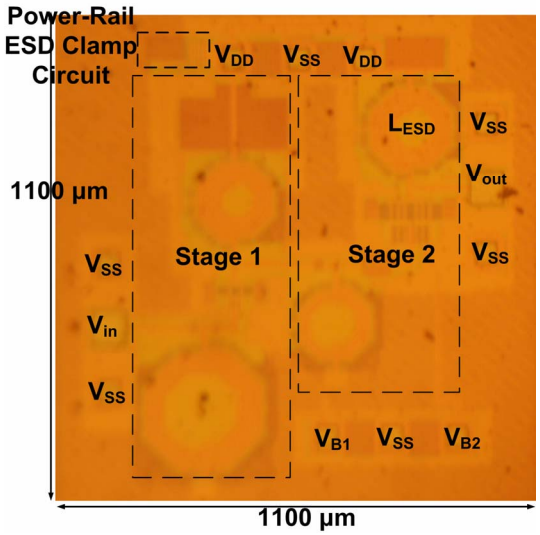

Figure 6. Die photo of ESD-protected PA fabricated in a 65-nm CMOS process.

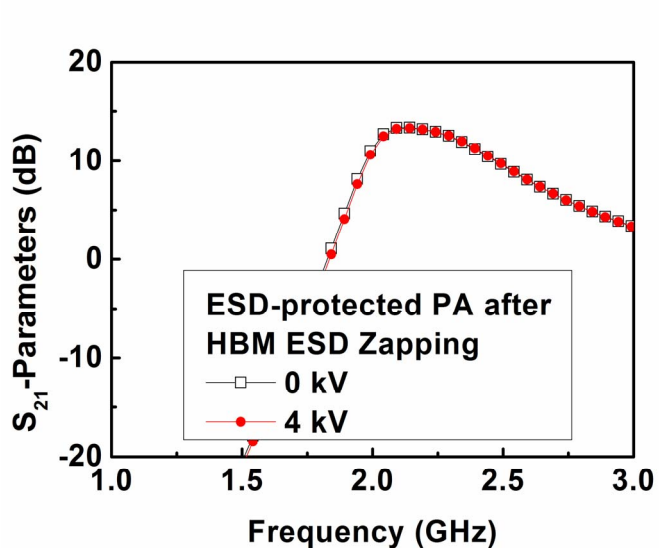

Figure 8. Measured S_{21}-parameters of ESD-protected PA before and after HBM ESD stress of 4 kV.

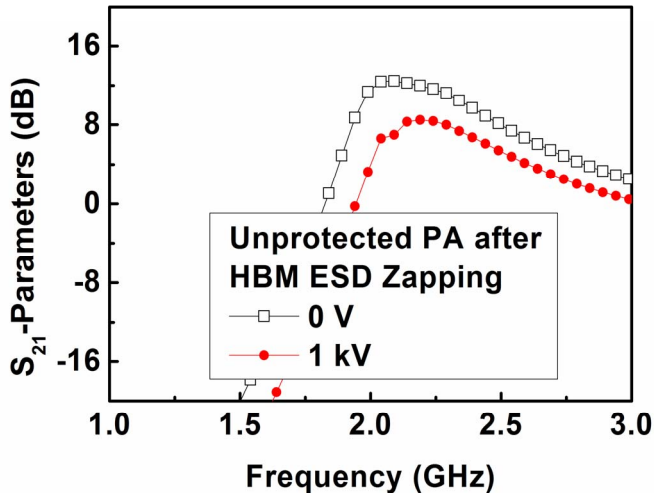

Figure 7. Measured S_{21}-parameters of unprotected PA before and after HBM ESD stress of 1 kV.

V. Conclusion

The proposed ESD protection strategy has been successfully verified in a 65-nm CMOS process. According to the measurement results, the RF performances of the unprotected PA degrade after 1-kV HBM ESD zapping, while those of the ESD-protected PA after 4-kV HBM ESD zapping still maintain the same. The proposed ESD protection strategy merely utilizes an RF inductor of the PA circuits and a power-rail ESD clamp circuit, but can provide at least 4-kV HBM ESD robustness and decrease the complexity of RF circuits design.

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