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A 56–67 GHz Low-Noise Amplifier with 5.1-dB NF and 2.5-kV HBM ESD Protection in 65-nm CMOS

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***Abstract*- This paper presents a V-band low-noise amplifier with high RF performance and ESD robustness. An inductor-triggered silicon-controlled rectifier (SCR) assisted with both a PMOS and an inductor is proposed to enhance the ESD robustness and minimize the impact of the ESD protection block on the millimeter-wave LNA. The initial-on PMOS improves the turn-on speed and the inductor resonates with the parasitic capacitance, respectively. Also, a 3-stage wideband V-band LNA is designed by using the gate inductor in the common-gate stage of the cascode topology as gain peaking to compensate the roll-off at high frequencies for bandwidth extension. The measured results demonstrate a 2.5-kV HBM ESD protection level with a minimum noise figure (NF) of 5.1 dB and a peak gain of 22 dB , also a 3-dB bandwidth of 56–67 GHz can be achieved under a power consumption of only 23 mW.**

***Index Terms* —CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), and millimeter wave (mm-Wave).**

I. INTRODUCTION

The millimeter-wave wireless communication at around 60 GHz has attracted tremendous interests in both academia and industries. Owing to the rapid progress in technology, CMOS shows the capability of high f_T and f_{MAX} under low power operation, and becomes the most suitable candidate for realizing a fully-integrated 60 GHz transceiver [1]-[4]. However, the reduced gate oxide thickness and hence lowered gate oxide breakdown voltage make the device more vulnerable to electrostatic discharge (ESD) [5]. The ESD protection level is in general proportional to the capacitive parasitics if using the conventional ESD devices such as diodes and silicon-controlled rectifier (SCR) [6]-[7]. These pose a significant challenge of designing robust on-chip ESD protection for a 60 GHz transceiver in advance CMOS technology.

In this paper, an inductor-triggered SCR (LTSCR) with the trigger circuit consists of inductor, PMOS, and RC-based ESD detection circuit, is proposed to reduce the trigger voltage and improve the turn-on efficiency of LTSCR. The series inductor can not only provide a detection path between the RC-based detection circuit and the initial-on PMOS, but also serve as a component to resonate the parasitic capacitance introduced by the SCR device. As a result, the signal loss can be reduced in a wide bandwidth. By co-optimization of ESD protection and RF characteristics, the proposed ESD-protected LNA demonstrates an HBM ESD level of 2.5 kV, a minimum NF of 5.1 dB, a peak power gain of 22 dB, and a 3-dB bandwidth of 56–67 GHz, under a power consumption of only 23 mW in 65-nm CMOS technology.

II. CIRCUIT DESIGN

A. Design of Inductor-Triggered SCR ESD Protection

The inductor-triggered SCR ESD protection circuit is shown in Fig. 1, which consists of an SCR device, an inductor (L_{ESD}), a PMOS transistor (M_T), and a RC-based ESD detection circuit embedded in the power-rail ESD clamp. The inductor-triggered SCR ESD protection circuit is employed in conjunction with the ESD clamp and the diode D_N to form a complete ESD network for the four different ESD testing modes, i.e. positive-to-V_{DD} (PD), positive-to-V_{SS} (PS), negative-to-V_{DD} (ND), and negative-to-V_{SS} (NS). The inductor provides a signal path between the RF_{IN} pad and the trigger terminal (node T as shown in Fig. 1) of the SCR device under ESD stress. The PMOS transistor at the trigger path, which is controlled by the ESD detection circuit, is also turned on when ESD zapping occurs. When the trigger signal passes from the RF_{IN} pad to the trigger terminal of the SCR device, the SCR device can be quickly turned on to discharge the ESD current. The RC-based ESD detection circuit is used to distinguish the ESD-stress conditions from the normal RF operation. Therefore, under power-on condition, the PMOS transistor is turned off to block the steady leakage current path from the RF_{IN} pad to the trigger port of the SCR device. Under normal RF operation, the inductor in series with the PMOS is used to compensate the parasitic capacitance of the SCR device (C_{ESD}).

The power-rail ESD clamp circuit consisting of the RC-inverter-triggered NMOS is used to provide ESD current paths between V_{DD} and V_{SS}. The R (~10 kΩ) and C (~10 pF) with the time constant of 0.1 μs ~ 1 μs can prevent the false triggering of the ESD block during normal RF operation. In normal RF operation, the node between R_C and M_C (MOS capacitor) is charged to the high potential (V_{DD}). During ESD stress zapping, the ESD voltage at V_{DD} has the fast rise time in the order of ~10 ns. With the RC delay, the power-rail ESD clamp circuit is turned on to provide an ESD current path from V_{DD} to V_{SS}. The power-rail ESD clamp circuit is placed

between V_{DD} and V_{SS}, and the parasitic induced by the power-rail ESD clamp is not that critical (both nodes connected to the AC ground). Note that the RC-based detection circuit can be embedded in the power-rail ESD clamp circuit to control the PMOS in the inductor-triggered SCR simultaneously, which is also helpful for reducing the chip size.

In the design of inductor-triggered SCR, the optimization of the inductor (L_{ESD}), PMOS transistor (M_T), SCR device, and diode (D_N) are mainly determined by the consideration of its impact on RF performance. Since the sizes of SCR and D_N depend on the required ESD robustness, a considerable amount of parasitic capacitance (C_{ESD}) cannot be avoided, which could seriously degrade the LNA performance. An inductor (L_{eq}) is introduced in parallel with the C_{ESD} to minimize the effect of the parasitic capacitance at the frequency of interest. The resonate frequency can be expressed as

$$\omega_o = \frac{1}{\sqrt{L_{eq} C_{ESD}}} \tag{1}$$

where L_{eq} consists of the equivalent inductances of the series L_{ESD} and M_T,

$$L_{eq} = L_{ESD} - \frac{1}{\omega_o^2 C_{MT}} \tag{2}$$

and C_{MT} can be expressed as

$$C_{MT} \approx C_{gs} + C_{gb} + C_{db}\,. \tag{3}$$

where C_{gs}, C_{gb}, and C_{db} are the gate-to-source capacitance, gate-to-body capacitance, and the drain-to-body capacitance of the PMOS transistor (M_T), respectively. Once the sizes of SCR and D_N have been chosen, the sizes of L_{ESD} and M_T can be designed to optimize the cell area and RF performances.

Fig. 1. Circuit schematic of the proposed ESD network including inductor-triggered SCR with the power-rail ESD clamp.

B. LNA with Common-Gate Inductive Feedback

Fig. 2 illustrates the schematic of the proposed transmission-line-based (TL-based) low noise amplifier. To achieve high-gain performance, a 3-stage cascade and common-gate inductive feedback topology is employed, in which the gate inductors are realized in short circuit stubs. Instead of increasing the dc current to boost the transconductance of the MOSFETs, using common-gate inductive feedback can effectively boost the gain and reduce the thermal noise. As a result, the circuit noise performance is improved with reduced dc power. In this design, for wideband operation, the shunt and series transmission lines formed by micro-strip lines (MSLs) are properly designed in all matching networks.

Fig. 2. Circuit schematic of the proposed LNA with gate inductor peaking.

III. Experimental Results and Discussion

A. RF Measurements

The proposed V-band ESD-protected low-noise amplifier is with a chip area of 1.52×1.28 mm^2 including the all testing pads, fabricated in 65-nm CMOS process. The RF characteristics of circuits were measured on-wafer. The LNAs operate from a 1.0 V supply and draw a current of 23 mA with an associate power consumption of 23 mW. Fig. 3 shows the measured S_{21} of the LNAs with a peak power gain of 22 dB at 64 GHz and a 3-dB bandwidth of 56–67 GHz, indicating successful gate inductor peaking for bandwidth extension. Fig. 3 also shows the measured input and output return losses (S_{11} and S_{22}) of the LNAs. The maximum input and output return losses are 16.8 and 11.6 dB, respectively, in the frequency range of 56–67 GHz. The minimum measured NF is 5.1 dB at 61.5 GHz. In addition, the linearity of the LNA was characterized by the two-tone inter-modulation distortion test. The measured P_{1dB} for the proposed ESD-protected LNA is –20 dBm.

Fig. 3. Measured S_{11}, S_{21}, S_{22} and NF of the proposed ESD-protected LNA.

B. ESD Testing Results

The *transmission line pulse* (TLP) measurement technique is widely used to provide precise, high-voltage and high-current waveforms for ESD characterization. The ESD test was performed on-wafer by dc probes using a Barth 4002 TLP test system. The pulse of a 10-ns rise time with a 100-ns pulse width was used to simulate the HBM ESD condition. The relation between the TLP second breakdown current (It_2) and the HBM ESD level (V_{HBM}) can be approximated as V_{HBM} (V) ~ It_2 (A) · R_{HBM} (Ω), where R_{HBM} (= 1.5 kΩ) is the equivalent resistance of human body resistance. The dc leakage current measurement was performed after each pulse to monitor if the device is damaged. The ESD failure level of the circuit was determined by sudden dc leakage current increase. Fig. 4 shows the test results of different ESD testing combinations (PD, PS, ND, and NS) for the proposed ESD-protected LNA. In the PD mode, the ESD bypass current enters from the RF input pad, flows through diode path of SCR to $V_{DD.}$ A sudden increase of the leakage current suggests that a second breakdown current It_2 is up to 1.9 A, corresponding to a 2.8-kV HBM ESD level. In the PS mode, the ESD current path also enters from the RF input pad, flows through SCR path to V_{SS}. A second breakdown current It_2 of 1.75 A can be achieved, corresponding to a 2.6-kV HBM ESD level. In the NS mode, the ESD current goes through D_N diode, exhibiting a second breakdown current It_2 up to 1.7 A, corresponding to a 2.5-kV HBM ESD level. In the ND mode, the TLP curve shows an It_2 of 1.7 A, corresponding to a 2.5-kV HBM ESD level, and an additional offset voltage and slightly higher on-resistance compared with the NS mode due to the power clamp. Table I compares this work with other previously published RF LNAs with/without ESD protection in the similar frequency range. Compared with the prior arts, this work demonstrates a V-band LNA showing a lowest NF of 5.1 dB, a highest power gain of 22 dB, a large 3-dB bandwidth of 11 GHz, and with a 2.5-kV HBM ESD protection in 65 nm CMOS under the low power consumption of 23 mW.

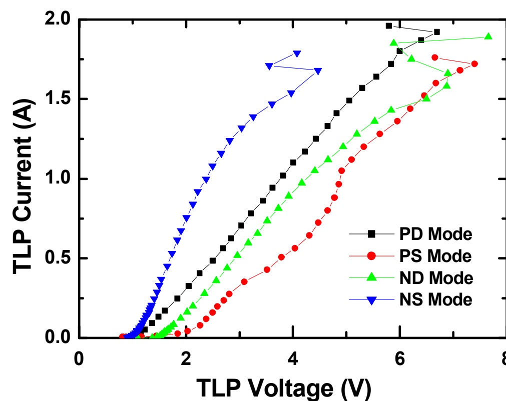

Fig. 4. Measured TLP *I-V* curves of the proposed ESD-protected LNA.

TABLE I
PERFORMANCE COMPARISON OF THE LNAS WITH PRIOR ARTS

Reference	This Work	[2]	[3]	[4]	[8]
Tech. (nm)	65	130	130	65	65
Freq. (GHz)	60	60	60	60	58
Power (mW)	23	65	54	35	18
Min. NF (dB)	5.1	8.6	8.8	6.1	5.3
S_{21} (dB)	22	20.4	12	19.3	17.5
S_{11} (dB)	– 16.8	– 15	< –15	< –15	–15
3-dB BW	56–67	55–62	51–65	55.8–63.5	54–61.5
HBM (kV)	> 2.5	1.5	--	--	> 8
P_{1dB} (dBm)	– 20	– 20	– 10	–16.6	--

IV. CONCLUSION

In this paper, we demonstrated a high performance ESD-protected V-band LNA fabricated in 65-nm CMOS technology. With the inductor-triggered SCR ESD technique, the series inductor can not only provide a detection path between the RC-based detection circuit and the initial-on PMOS, but also resonate with the parasitic capacitance introduced by the SCR device to minimize the impact of ESD block on the LNA core circuit. The proposed LNA demonstrated a 2.5 kV HBM ESD level, a minimum NF of 5.1 dB, a peak power gain of 22 dB, a 3-dB bandwidth of 56–67 GHz, under a power consumption of only 23 mW.

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