# Design of Negative High Voltage Generator for Biphasic Stimulator with SoC Integration Consideration

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***Abstract*—For electronic prosthetic system-on-chip (SoC) in the commercial bulk CMOS processes, a negative high voltage generator used in a biphasic stimulator was proposed. Realized in a 0.18-µm low-voltage CMOS process, the negative high voltage generator can deliver -8 V with a 1.8-V supply.**

## I. Introduction

Biphasic stimulators are generally used for cochlear, retinal, neural, and other electrical stimulations [1]-[3]. It is required that the anodic and cathodic stimulus currents matched for safe consideration. Since the stimulus voltage derived from the product of electrode/tissue impedance and stimulus current was usually as high as ~10 V, the high voltage generator is needed to pump $V_{DD}$ to such high voltage ($V_{CC}$). Besides the positive high voltage generator, another negative high voltage generator is also needed, as shown in Fig. 1. With the potential for mass production, CMOS technologies are more attractive to realize the system on a chip (SoC). Therefore, the positive and negative high voltage generators should be feasible in the commercial low-voltage CMOS processes.

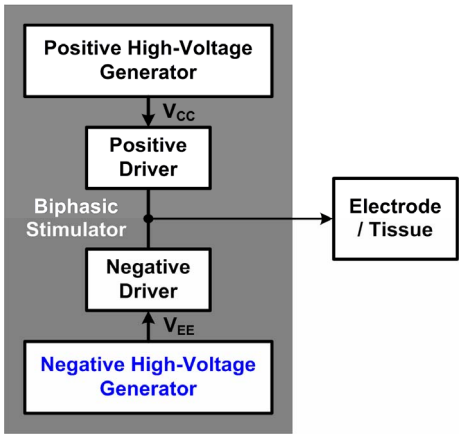


Fig. 1. Biphasic stimulator for electrical stimulation.

To realize the negative high voltage generator, Fig. 2 shows a conventional design which uses all PMOS switches with four-phase negative charge pump in a 0.6-µm high-voltage CMOS process [4]. However, the high-voltage CMOS processes are commonly not used for SoC integration. Besides, if the negative high voltage generator is realized by using PMOS switches in a P-substrate, the body terminals of the PMOS switches must connect to ground to prevent from the substrate leakage issue, which leads to the body effect [5].

The challenges for designing the negative high voltage generator are: (1) substrate leakage issue: if the N-well of PMOS switches is biased to the negative voltage, the leakage occurs through the P-substrate/N-well junction; (2) reliability issue: if the low-voltage transistors operate at high voltage, the gate-oxide breakdown, hot carrier, and other reliability issues would happen; and (3) breakdown voltage limitation: the output voltage must be regulated at the level below the lateral pn-junction breakdown voltage [6].

In this work, a negative high voltage generator has been designed, fabricated, and characterized in a 0.18-µm 1.8-V/3.3-V CMOS process. The detailed design procedures and the measurement results in silicon chip will be presented in following sections.

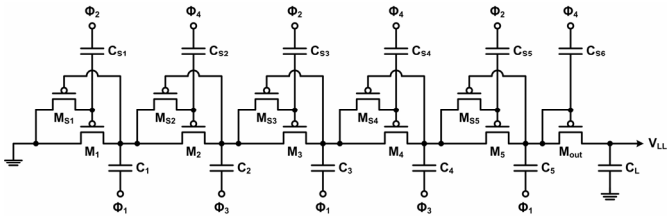


Fig. 2. Conventional negative high voltage generator with PMOS switches.

## II. Proposed Negative High Voltage Generator

The proposed negative high voltage generator consists of a 6-stage negative charge pump, a 4-phase clock generator, feedback, and buffers, as shown in Fig. 3. The 4-phase clock generator provides the charge pump with the adaptive control signal. The charge pump is controlled by the feedback. The feedback is built with many stages to reduce the supply current and to enhance the power efficiency. Different from the conventional feedback, this design adds two filtered

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capacitors for the noise-reduced input of the comparator and low dropout regulator (LDO) to guarantee the output voltage accuracy.

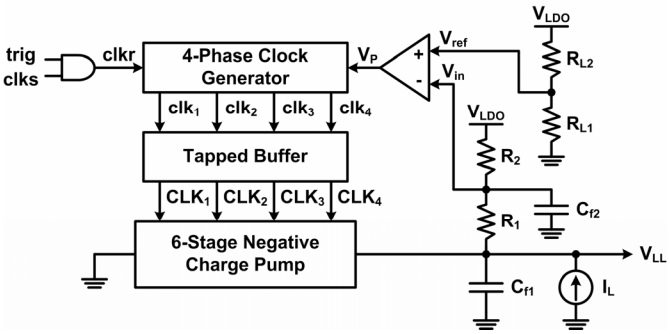


Fig. 3. Design of the negative high voltage generator.

The pumping decides in whether the output voltage of the negative generator achieves the target value. If the output voltage does not reach the target value, the feedback signal will be high (1.8 V). Therefore, the 4-phase clock generator outputs clock signals to make the charge pump pumping. When the output voltage reaches the target value, the feedback signal will be low (0 V), and the charge pump stops pumping. With clock gating, the negative high voltage generator turns on after the appropriate trigger signal.

The design and operation of each function blocks used in the proposed design will be discussed in following paragraphs.

### *A. 6-STAGE NEGATIVE CHARGE PUMP*

Fig. 4 shows the 6-stage negative charge pump which consists of NMOS switches with deep N-well. The P-well of each NMOS is isolated from P-substrate, so each NMOS has local bulk to bias. The deep N-well is biased at ground and the bulk of the NMOS is connected to the source. These NMOS with deep N-well can pump to negative high voltage without body effect and substrate leakage.

To ensure the reliability issue, the gate-source voltage (|Vgs|) and gate-drain voltage (|Vgd|) of each NMOS switches must be less than 1.8 V or 3.3 V in the 0.18-μm 1.8-V/3.3-V CMOS process. Since the |Vgs| of MN2 and MN4 exceeds 1.8 V, the 3.3-V transistors are used for MN2 and MN4, while the 1.8-V transistors are selected for MN1 and MN3. The NMOS switches are utilized to transfer charge from input to output in each stage, and clocks are out-of-phase.

The pumping and discharging of the charge pump in the negative high voltage generator are driven by the 4-phase clock signals (CLK1, CLK 2, CLK 3, and CLK 4). The clock diagrams are shown in Fig. 5. The non-overlapping clock phases prevent shoot-through current.

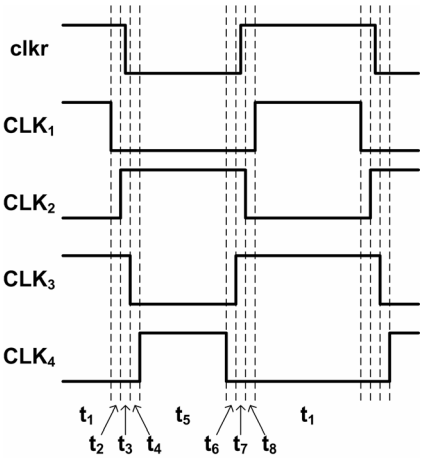


Fig. 5. The clock signals used for the negative charge pump.

### *B. 4-PHASE CLOCK GENERATOR AND TAPPED BUFFER*

The 4-phase clock generator is shown in Fig. 6. The reference clock signal (clkr) will be modulated to the 4-phase clock signals through the 4-phase clock generator. The tapped buffer can drive the loading capacitance between the 4-phase clock generator and the 6-stage negative charge pump.

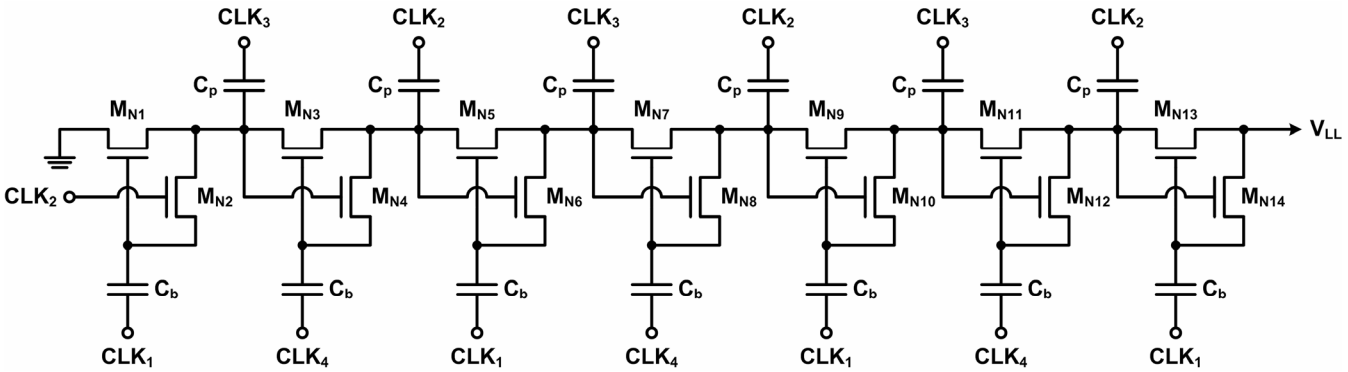


Fig. 4. Proposed 6-stage negative charge pump with NMOS realized in deep N-well.

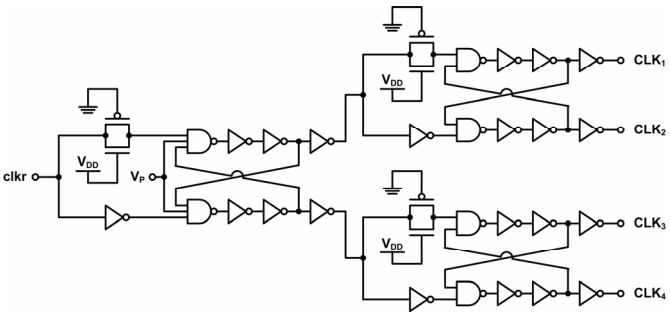


Fig. 6. The 4-phase clock generator.

### C. Comparator

The comparator plays an important role for the negative high voltage regulator. The comparator with high gain would enhance the output voltage accuracy, and it with high bandwidth would fit the load transient and slew rate demands. The comparator is based on an operational amplifier (OP), as shown in Fig. 7. The last-stage inverter is used to make output signal full-swing and reduce the output capacitance in the comparator. This comparator performs 60.518-dB dc gain, 197.52-MHz bandwidth, and 60° phase margin.

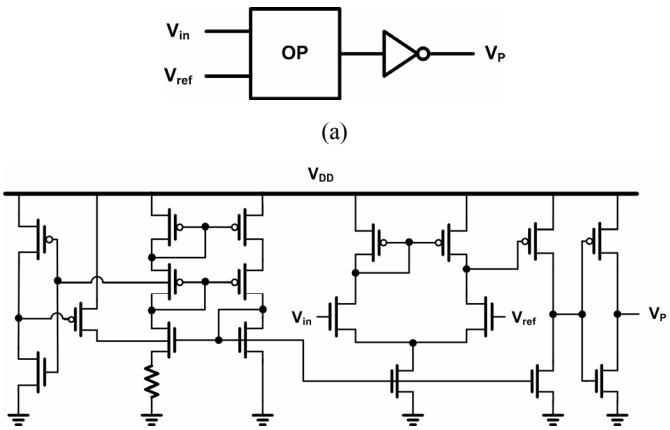


Fig. 7. (a) Block diagram and (b) schematic diagram of comparator design.

### D. Feedback

The feedback is built for the charge pump with many stages to reduce the supply current and enhance the efficiency. The design with two filtered capacitors is shown in Fig. 3. The LDO used in the feedback provides a stable reference voltage for the negative voltage generator to avoid 10% supply voltage variance [7]. The bandgap with 22 ppm/°C offers the reference voltage to avoid the temperature variance [8]. The output voltage ($V_{LL}$) of the negative high voltage generator can be calculated as

$$V_{LL} = \left( \frac{R_{L1}}{R_2} \cdot \frac{R_1 + R_2}{R_{L1} + R_{L2}} - \frac{R_1}{R_2} \right) \cdot V_{LDO} \quad (1)$$

## III. Measurement Results

The test circuit of negative high voltage generator has been fabricated in a 0.18-μm 1.8V/3.3V CMOS process. The die photograph is as shown in Fig. 8, which includes the 4-phase clock generator (A), the tapped buffer (B), the 6-stage negative charge pump (C), the comparator (D), the feedback (E), and the loading capacitor (F). All the function blocks occupy an area of 1.07×1.19 $mm^2$.

Fig. 9 shows the measured output voltage ($V_{LL}$). For higher clock frequency, the output voltage ($V_{LL}$) maintains -8 V at larger loading current while the power efficiency decreases. At 12.5 MHz, the maximum loading current for -8 V $V_{LL}$ is 100 μA and the power efficiency is 27%. At 33.25 MHz, the maximum current is 320 μA and the power efficiency is 42.26% at the loading current 200 μA. Since the target of the output current of negative high voltage generator in the SoC was ~200 μA, the measured power efficiency under 200-μA loading current is shown in Fig. 10. Table I summarizes the measurement results of the test chip.

TABLE I
Measurement Results

| | |
|---|---|
| $V_{DD}$ | 1.8 V |
| clkr | 0/1.8 V, 33.25 MHz |
| $V_{LL}$ | -8.04 V |
| $I_{max}$ | 320 μA |
| Error | 0.375% |
| Load Regulation | 0.194 mV/μA |
| Line Regulation | 0.166 V/V |
| Power Efficiency | 42.26% @ $I_{load}$ = 200 μA |
| Power | 3.8 mW @ $I_{load}$ = 200 μA |

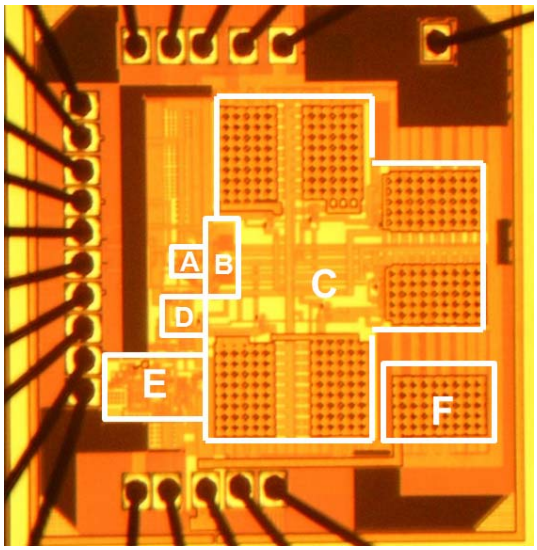


Fig. 8. Die photograph with A: 4-phase clock generator, B: tapped buffer, C: 6-stage negative charge pump, D: comparator, E: feedback, and F: loading capacitor.

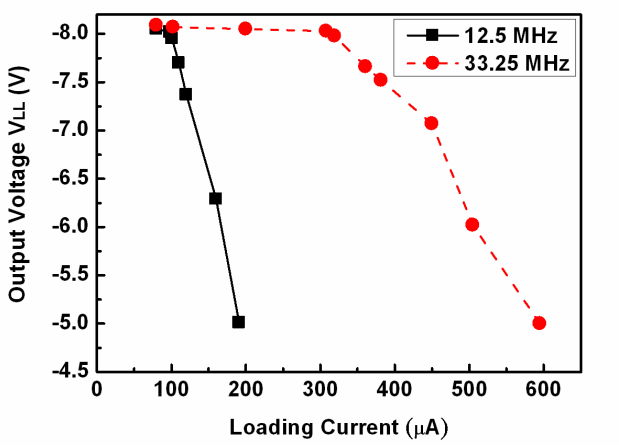


Fig. 9. The measured output voltage ($V_{LL}$) versus the loading current tested by different clock frequencies.

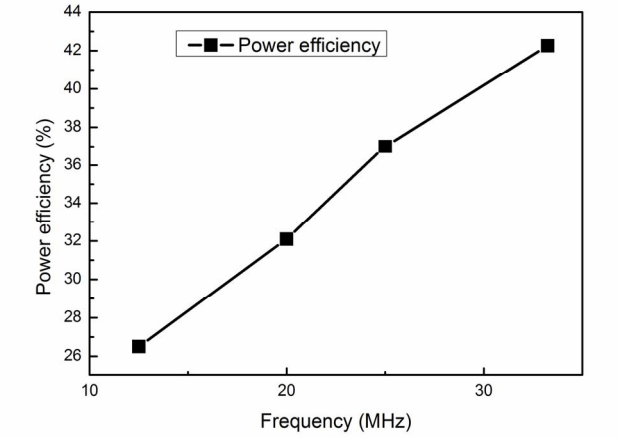


Fig. 10. The power efficiency versus clock frequency under 200-μA loading current.

TABLE II
COMPARISON

| | This work | [5] |
|---|---|---|
| $V_{DD}$ | 1.8 V | 1.8 V |
| Charge Pump Stage | 6 | 3 |
| $V_{LL}$ | -8 V | -9 V |
| Feedback Circuit | With | Without |
| Pumping Capacitance per Stage | 25 pF | 50 pF, 25pF double for the cross-couple charge pump |
| Power | 3.8 mW | 4.65 mW |
| Power Efficiency | 42.26% @ $I_{load}$ = 200 μA | 35.88% @ $I_{load}$ = 200 μA |
| Technology | 0.18-μm 1.8V/3.3V CMOS Process | 0.8-μm 5V/20V CMOS Process |

## IV. DISCUSSION AND COMPARISON

Table II illustrates the comparison between the proposed design and the prior art [5]. To provide the negative high voltage, the high-voltage processes are usually used. In this work, the negative high voltage generator has been designed to deliver the required $V_{LL}$ by using low-voltage CMOS process with low supply voltage ($V_{DD}$ = 1.8 V). Without using the high-voltage processes, the proposed design can be integrated with the other circuit blocks of the biphasic stimulator into a chip. Besides, the feedback loop used in this work guarantees the accuracy of $V_{LL}$ voltage.

## V. CONCLUSION

A negative voltage generator for SoC integration has been proposed and fabricated in a 0.18-μm 1.8V/3.3V CMOS process. By using the NMOS switches in deep N-well and modified feedback, the measurement results show the output voltage ($V_{LL}$) regulates at -8 V without substrate leakage, gate-oxide overstress, and lateral pn-junction breakdown concerns. The proposed design can be further integrated for an electronic prosthetic SoC.

## ACKNOWLEDGEMENT

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