Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process

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50 Words Abstract - An ESD protection cell consisted of a diode, a silicon-controlled rectifier (SCR), a PMOS, and inductors was proposed for dual-band radio-frequency (RF) ESD protection. The proposed ESD protection cell was suitable for RF circuit designers for them to easily apply ESD protection in the dual-band RF circuits.

I. Introduction

As CMOS technology advanced, millimeter-wave (MMW) circuits become more attractive for many applications such as automotive radar sensors at 24/77 GHz and wireless communications at 24/60 GHz [1,2]. To support the dual-band applications and to lower the fabrication costs, a dual-band radio-frequency (RF) ESD protection cell is needed. Several dual-band RF transceivers operated at these frequency bands have been realized [3,4]. Nanoscale CMOS technologies have been used to implement RF circuits with the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the ESD robustness of IC products. Therefore, an on-chip ESD protection circuit must be added at the first stage of the RF receiver. The ESD protection circuit is added to the input (RF_{IN}) pad of the low-noise amplifier (LNA) against ESD damages. ESD protection devices cause RF performance degradation with several undesired effects [5,6]. To minimize the impacts from the ESD protection circuit on RF performances, the ESD protection circuit at the input pads must be carefully designed. In this work, the dual-band RF ESD protection cell has been implemented with compact size. The proposed ESD protection cell can be used by RF circuit designers for them to easily apply ESD protection in the dual-band RF circuits.

II. Implementation of Dual-Band RF ESD Protection Cell

Among the ESD protection devices, silicon-controlled rectifier (SCR) device has been reported to be useful for RF ESD protection design due to its high ESD robustness within a small layout area and low parasitic capacitance [7]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage. The device structure of the SCR device used in RF input (RF_{IN}) pad is illustrated in Fig. 1. The SCR path between RF_{IN} and V_{SS} consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between RF_{IN} and V_{DD} consists of P+ and N-well/N+. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of an SCR device, the trigger signal can be sent to enhance the turn-on speed. Some design techniques have been reported to enhance the turn-on efficiency of SCR devices [7]. However, adding a trigger circuit to SCR device also increases the parasitic capacitance seen at the RF_{IN} pad, which is hard to tolerate for RF circuits.

In this work, a novel SCR design is proposed for dual-band RF ESD protection at 24/60 GHz. The proposed dual-band RF ESD protection cell is shown in Fig. 2, which consists of a diode, an SCR, a PMOS (M_1), inductors (L_1 and L_2), and a power-rail ESD clamp circuit. The L_1 is used to provide the trigger path between the RF_{IN} pad and the trigger port of the SCR device under ESD stress conditions. The resistor and capacitor used in the power-rail ESD clamp circuit are

used to control the M_1. The M_1 at the trigger path is also turned on under ESD stress conditions. When the trigger signal passes from the RF_{IN} pad to the trigger port of the SCR device, the SCR device can be quickly turned on to discharge the ESD current. Under normal power-on conditions, the M_1 is turned off to block the steady leakage current path from the RF_{IN} pad to the trigger port of SCR device. Under normal RF circuit operating conditions, the L_1 in series with the M_1 is used to compensate the parasitic capacitance of SCR (C_{SCR}) at 24 GHz, while the L_2 in series with the D_N is used to compensate the C_{SCR} at 60 GHz. The sizes of SCR and D_N depend on the required ESD robustness, while the size of M_1 depends on the required trigger current. Once the sizes of M_1, SCR, and D_N have been chosen, the required inductors (L_1 and L_2) can be determined.

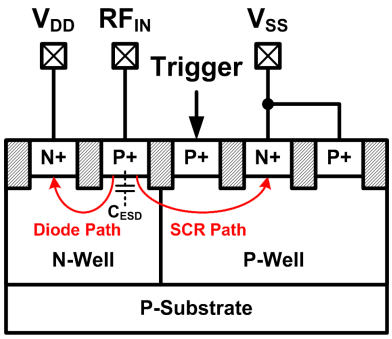

Figure 1: Device cross-sectional view of SCR device used in RF input pad.

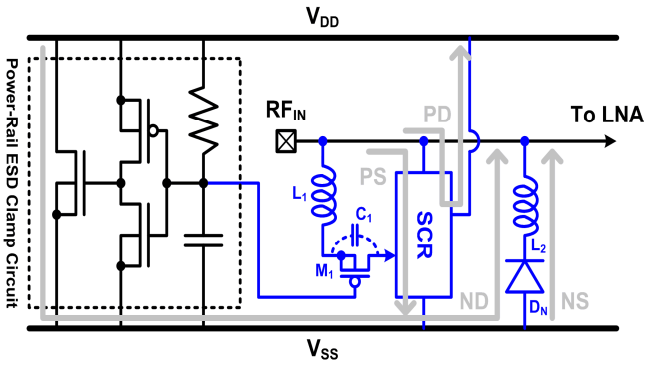

Figure 2: Proposed ESD protection scheme for RFIN pad with inductor-triggered SCR, DN, and power-rail ESD clamp circuit.

Fig. 2 also shows the ESD current paths under positive-to-V_{SS} (PS), positive-to-V_{DD} (PD), negative-to-V_{SS} (NS), and negative-to-V_{DD} (ND) ESD stress conditions. During PS ESD stress, ESD current will first pass through the L_1 and M_1 to trigger the SCR device. The major ESD current will be discharged by the SCR device from the RF_{IN} pad to V_{SS}. Under PD ESD stress, the ESD current will be discharged by the parasitic diode path embedded in the SCR device from the RF_{IN} pad to V_{DD}. During NS ESD stress, the ESD current will be discharged by the forward-biased D_N from the V_{SS} through L_2 to RF_{IN} pad. Under ND ESD stress, the ESD current will be discharged by the power-rail ESD clamp circuit, D_N, and L_2 from V_{DD} to RF_{IN} pad. The proposed ESD protection scheme in Fig. 2 can provide the corresponding current discharging paths with good ESD robustness.

III. Experimental Results

The test circuits have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. The test patterns include the test circuits A, B, C, and D. The device dimensions of the test circuits are listed in Table 1. The size of SCR device used in the test circuits A, B, C, and D are split as 8 μm, 15 μm, 23 μm, and 30 μm, respectively. The size of D_N in test circuits A, B, C, and D are also split as also 8 μm, 15 μm, 23 μm, and 30 μm, respectively. The width / length of M_1 in each test circuit is kept at 90 μm / 0.2 μm. Therefore, the required L_1 (L_2) are 0.58 nH (0.38 nH), 0.58 nH (0.27 nH), 0.58 nH (0.23 nH), and 0.58 nH (0.2 nH) for the test circuits A, B, C, and D, respectively. Fig. 3 shows the Chip photograph of one test circuit D with cell size of 100×180 μm^2.

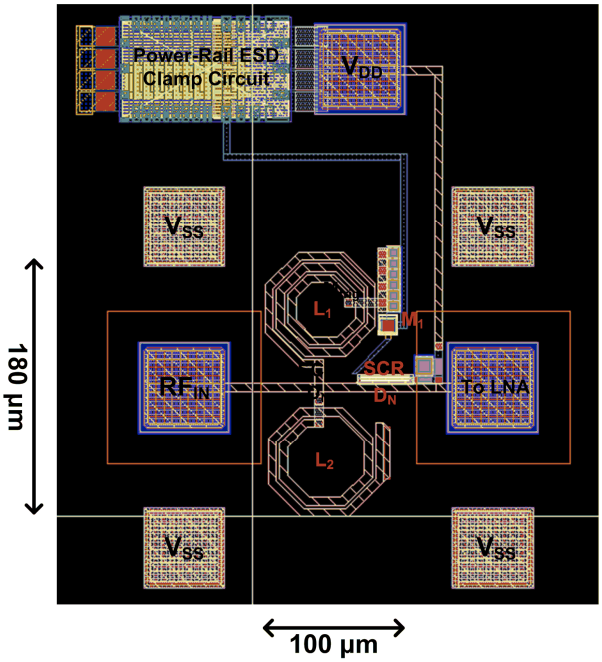

Figure 3: Layout top view of test circuit D.

A. RF Performances

With the on-wafer RF measurement, the S parameters of these four test circuits have been extracted from 0 to 67 GHz. The voltage supply of V_{DD} (V_{SS}) is 1 V (0

V), and the dc bias of RF_{IN} is 0.5 V ($V_{DD}/2$). The source and load resistances to the test circuits are kept at 50 Ω. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using de-embedding technique. The measured S_{11}-parameters and S_{21}-parameters versus frequencies among the four test circuits are shown in Figs. 4 and 5, respectively. As shown in Fig. 4, these ESD protection circuits exhibit good input matching (S_{11} parameters < -15 dB) around 24/60 GHz. At 24-GHz (60-GHz) frequency, the test circuits A, B, C, and D have about 1.29-dB (1.22-dB), 1.26-dB (1.28-dB), 1.28-dB (1.42-dB), and 1.35-dB (1.57-dB) power loss, respectively.

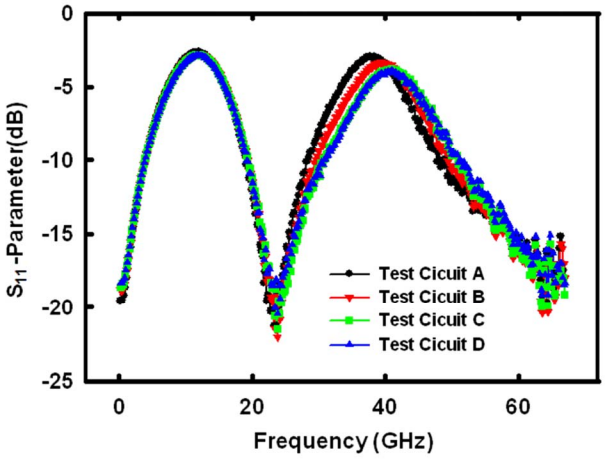

Figure 4: Measurement results of S_{11} parameters among the four test circuits with the proposed ESD protection scheme under different device dimensions.

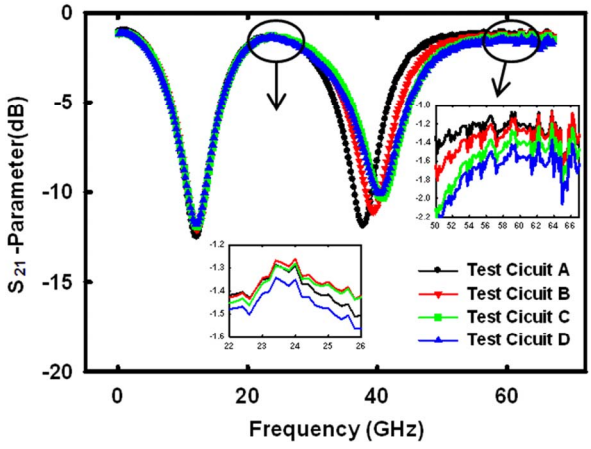

Figure 5: Measurement results of S_{21} parameters among the four test circuits with the proposed ESD protection scheme under different device dimensions.

B. ESD Robustness

The human-body-model (HBM) ESD pulses are stressed to each test circuit under PS, PD, NS, and ND ESD stress conditions. The failure criterion is defined as the I-V characteristics seen at RF_{IN} shifting over 30% from its original curve after ESD stressed at every ESD test level. The HBM ESD robustness among the four test circuits with the proposed ESD protection designs are listed in Table 1. The HBM ESD levels of the proposed ESD protection circuits A, B, C, and D can achieve 0.5 kV, 1.25 kV, 1.5 kV, and 2.25kV, respectively, which are obtained from the lowest levels among PS, PD, NS, and ND ESD tests. The HBM ESD robustness of the test circuits is almost proportional to the sizes of ESD protection devices.

Table 1: Device dimensions and measurement results of ESD protection cells with inductor-triggered SCR

	Test Circuits			
	A	**B**	**C**	**D**
SCR (μm)	**8**	**15**	**23**	**30**
D_N (μm)	**8**	**15**	**23**	**30**
L_1 (nH)	**0.58**	**0.58**	**0.58**	**0.58**
L_2 (nH)	**0.35**	**0.3**	**0.25**	**0.21**
M_1 (μm / μm)	**90/0.2**	**90/0.2**	**90/0.2**	**90/0.2**
Area (μm x μm)	**100x200**	**100x190**	**100x185**	**100x180**
S_{11} at 24 GHz (dB)	**-19**	**-19.7**	**-19.6**	**-18.5**
S_{11} at 60 GHz (dB)	**-15.6**	**-16.3**	**-16.1**	**-15.5**
S_{21} at 24 GHz (dB)	**-1.29**	**-1.26**	**-1.28**	**-1.35**
S_{21} at 60 GHz (dB)	**-1.22**	**-1.28**	**-1.42**	**-1.57**
PS HBM (kV)	**0.50**	**1.25**	**1.50**	**2.25**
PD HBM (kV)	**0.75**	**1.50**	**2.25**	**2.50**
NS HBM (kV)	**0.75**	**1.75**	**2.25**	**2.25**
ND HBM (kV)	**0.75**	**1.25**	**1.75**	**2.25**

To further investigate the effectiveness of the proposed dual-band ESD protection circuit in faster ESD-transient events, another very fast TLP (VF-TLP) system is also used with 0.2-ns rise time and 1-ns pulse width. The VF-TLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [8]. The tests circuits A, B, C, and D under PS-mode tests can achieve VF-TLP-measured It_2 of 1.3 A, 1.85 A, 2.3 A, and 2.88 A, respectively. These results show that the proposed dual-band ESD protection circuits with inductor-triggered SCR are fast enough to be turned on among fast impulse response.

IV. ESD Protection Cell Applied to LNA

One 24/60-GHz LNA is designed and fabricated in a 65-nm CMOS technology for verification purpose. The polysilicon resistors and metal-insulator-metal (MIM) capacitors are available in this process. Fig. 6 shows the circuit schematic of the 24/60-GHz LNA with the proposed dual-band ESD protection circuit. In order to implement 24/60-GHz LNA without additional MOS switches [9], two LNAs (24GHz and 60GHz) are designed in parallel using single RF_{IN} and RF_{OUT}. Each LNA consists of two-stages and the cascode configuration is applied to achieve high gain performance. Besides, the common-source and common-gate NMOS transistors are all with 56-μm gate width and 0.06-μm gate length. The gate bias of the designed 24/60-GHz LNA is 0.73V through bias tee at RF_{IN} and total DC power consumption is 88mW under 1V V_{DD} power supply.

ESD protection circuits A and D are applied to the 24/60-GHz LNA circuit in silicon chip. Fig. 7 shows a layout top view of of the 24/60-GHz LNA with the ESD protection circuit D. The layout size of one circuit is 800×750 μm^2, including all testing pads and dummy layers. The dummy layers are kept away from the signal paths, so they will not influence the RF signals. The stand-alone LNA without RF ESD protection is also fabricated for comparison. All the LNA circuits with and without ESD protection circuits are fabricated on the same wafer for comparison.

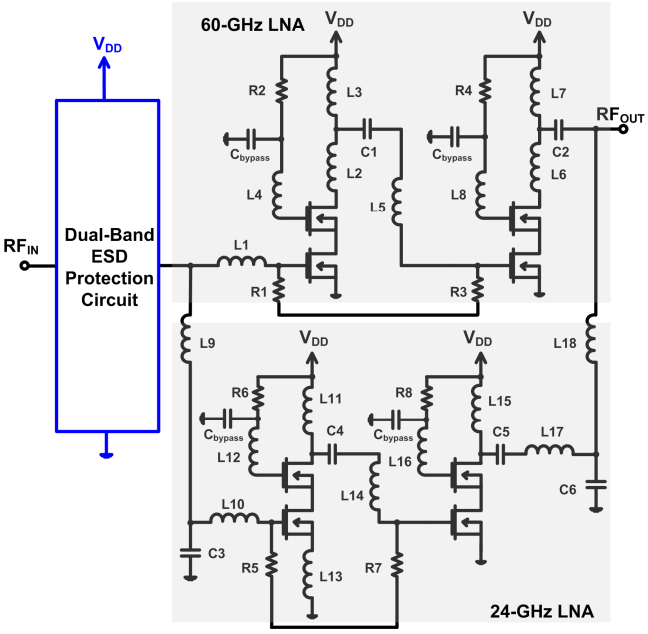

Figure 6: Circuit schematic of 24/60-GHz LNA with dual-band ESD protection circuit.

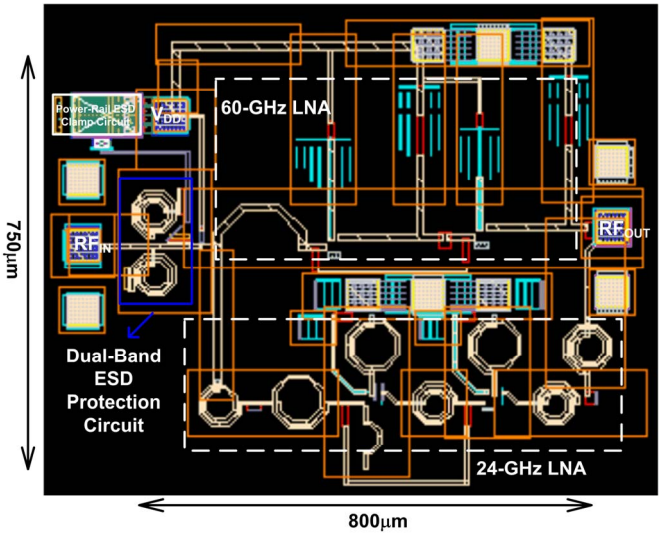

Figure 7: Layout top view of 24/60-GHz LNA with dual-band ESD protection circuit D.

The RF characteristics are measured on wafer through G-S-G microwave probes with 100-μm pitch. The short-open-load-thru calibration has been done before the measurements. The measured S_{11} and S_{21} parameters of the LNA circuits are shown in Figs. 8 and 9, respectively. Although the operating frequencies of LNA are shifted to lower frequencies, the ESD protection cells still can provide suitable ESD protection with only slight degradation on RF performances.

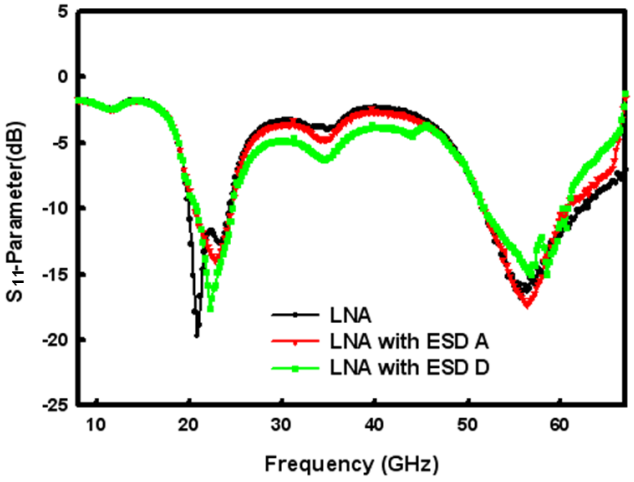

Figure 8: Measurement results of S_{11} parameters on dual-band LNA with and without ESD protection circuits.

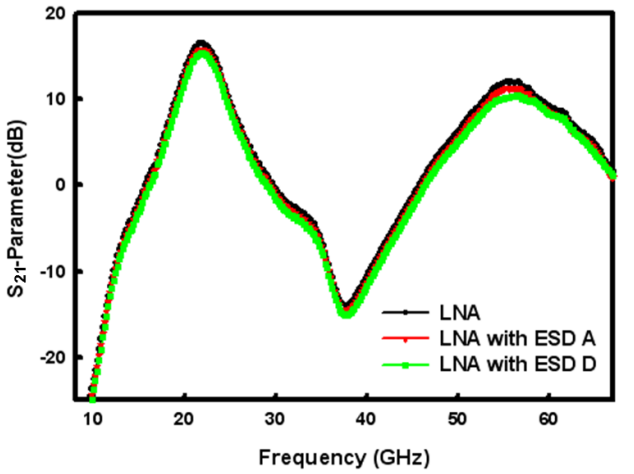

Figure 9: Measurement results of S_{21} parameters on dual-band LNA with and without ESD protection circuits.

V. Conclusion

The new ESD protection cell for 24/60 GHz dual-band RF applications has been designed, fabricated, and characterized in a 65-nm CMOS process. The proposed ESD protection design can be used to achieve good RF performance and ESD robustness simultaneously. Besides, the ESD protection cell can be further designed for other MMW circuits, such as 24/77 GHz application.

Acknowledgements

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