Design of AC-Coupled Circuit for High-speed Interconnects

Chun-Wei Huang, Kai-Jen Liu, Yu-Jung Huang
Dept. of Electronic Engineering, I-Shou University
Kaohsiung, Taiwan, R.O.C.
yjhuang@isu.edu.tw

Ming-Kun Chen, Yi-Lung Lin
Advanced Semiconductor Engineering Test RD, Kaohsiung Export Processing Zone,
Kaohsiung, Taiwan, R.O.C.
mkc_chen@aseglobal.com

Ming-Dou Ker
Dept. of Electronics Engineering, National Chiao Tung University
1001 University Road,
Hsinchu, Taiwan 300, R.O.C.

***Abstract*— The scaling of semiconductor technology together with 3D IC stacking integration make it possible for many portable electronics to process large amount of multimedia data. AC-coupling enables chip placed face-to-face for signal transmission using close-field capacitive coupling. A high performance system design using AC coupled interconnect (ACCI) technology not only achieves shorter and faster interconnection between dies but also increases packaging density. This paper describes a chip-to-chip circuit design suitable for high-speed 3DIC interconnected applications. The AC-Coupled face-to-face (F2F) chip was simulated using HSPICE with TSMC 0.18-μm 1P6M CMOS technology process file under a 1.8 V supply voltage. The simulation results indicated the proposed circuit with the self-test characteristics can achieve differential signal transmission up to 2.5 Gbps.**

***Index Terms*—three-dimensional integrated circuit (3D IC), AC-Coupled, high-speed interconnected, differential signal transmission**

I. INTRODUCTION

With CMOS technology continuing to scaling down, the conventional copper (Cu) based electrical interconnect cannot longer satisfy the IC and packaging design specifications for lower delay, lower power, higher bandwidth, and lower noise requirements. In addition, the complexity of ICs continually increases such that the metal wiring interconnect delay dominates the device speed performance. As the scale of CMOS manufacture technology increase significantly in each new technology node, interconnection delays have become dramatically significant for 0.18μm technology node [1]. In order to keep up with Moor's law scaling and to meet application demands, the three-dimensional integrated circuit (3DIC) integration has been an attractive solution to complex integration due to its higher number of I/O pin counts, wide communication parallelism and heterogeneous integration in the packaging. 3DIC integration enables multi-chips to be stacked vertically in a device and hence high-performance device can be realized even using less scaled CMOS technology. As interconnects have been a key limiting factor in chip design, a variety of novel interconnection concepts have been developed to address this challenge over the past decade. Wire bonding [2], micro bumps (μB) [3, 4] and through-Si vias (TSV) [5, 6] are adopted for 3D integration. A conventional bonding-wire interconnection limits the speed performance for data transfer rate due to its long metal line interconnection. The periphery bonding also restricts aggregate data rate bandwidth (BW) and induces higher power dissipation, inductance, and signal time delay with an increased number of input/outputs (I/Os) counts [2]. The connections of μB technology are made using copper, solder or gold bumps on the top surface of chip. In general, the bump pitch is around 30-500μm. Compared to wire bond technology, μB technologies provide greater vertical stacked density of interconnection. The heat of chips generated inside the cube limits the number of chips that can be stacked in the packaging [7]. TSV is a realizable metal interconnection structure to connect vertically stacked chips with the shortest interconnection. By using TSVs, it is possible to save the space that would be necessary for bonding wires and to make wiring lengths shorter. However, both μB and TSV require additional fabrication processes and result in considerable cost increase.

An alternative to metal wiring interconnections, proximity communication (PxC) or contactless communication can be realized with capacitive coupling interconnection (CCI) or inductive coupling interconnection (ICI) methods. An ICI [8] is the current driven and allows for long-distance communications between two chips. The communication capability of inductive coupling is increased the driven current or the layout area of inductor. In addition, the ICI basically requires stacked vertical structure and separate interfaces which also increase the area overhead [8]. In contrast, CCI is the voltage driven and its structures are applying the near-distance communications in face-to-face (F2F) stacking. [9-11].

A test-chip with a complete capacitive coupled serial link with a fully differential pulse receiver design is demonstrated in this paper. The general concept of CCI is discussed in session II. The circuit functionality used in the design process is presented in session III. Simulation results and measurements results acquired from a pseudo random binary sequence (PRBS) are shown in session IV and the conclusions are drawn in Session V.

978-1-4673-5085-3/12/$31.00 ©2012 IEEE

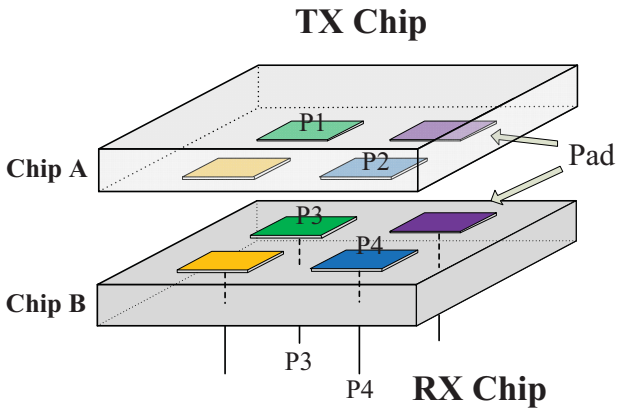


Fig. 1. Cross-section of a vertical link across two tiers.

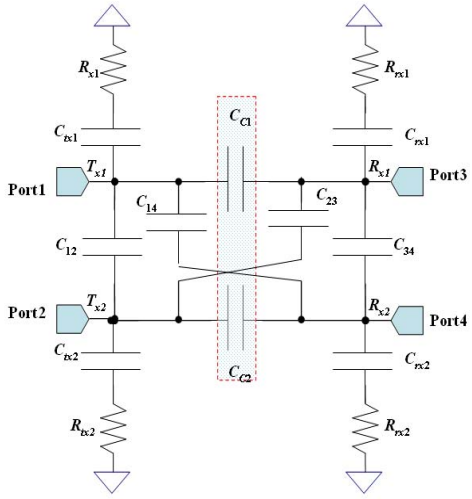


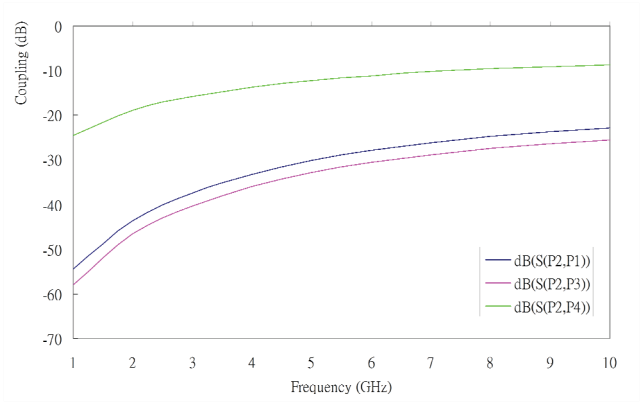
Fig. 2. Idealized model for analyzing the physics of capacitive coupling between two pads.

II. CAPACITIVE PROXIMITY INTERCONNECTS

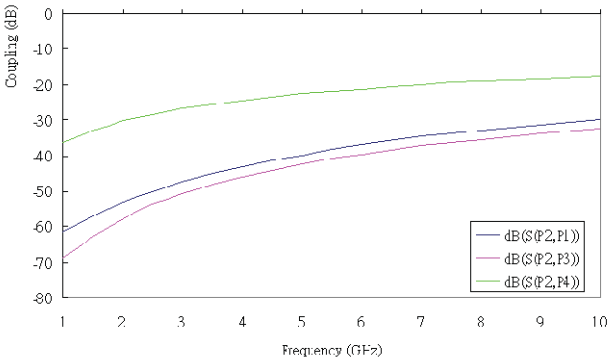
A. CCI Interface Modeling

The capacitance is the key component that controls the data link architecture of the CCI. To assure the signal quality between inter-chip communication, it is necessary to consider the electrical effects due to coupling pads alignments. CCI relies on capacitive coupling to transmit signals from one chip to another in extremely near proximity distance. Details of this technology have been described in [9-11]. Capacitive coupling along with the electrical impedance of the interconnection forms a high-pass filter. As shown in Fig. 1, this can be done by placing two chips F2F.

In designing a CCI; it is important to provide a correct electrical model for the coupling link capacitance. A lumped circuit depicted in Fig. 2 represents the equivalent circuit model of CCI system. This RLC circuit model can be used to predicted the time delay and noise crosstalk effects of CCI using SPICE circuit simulator. C_{tx1}, C_{tx2}, C_{rx1} and C_{rx2} are the self-capacitance of each coupling pads for the parasitic effects of the silicon substrate, R_{tx1}, R_{tx2}, R_{rx1} and R_{rx2} represent the resistor of the metal conductivity losses and the skin effect at



(a)



(b) cross-coupling transfer

Fig. 3. S-parameters simulation resulting of capacitive coupling pad for (a) data-link-coupling and (b) cross-coupling transfer.

high frequencies for each pad of data-link-coupling, and C_{12} and C_{34} are the cross-coupling capacitance present between the two pads of same chip, and C_{14} and C_{23} are the cross-coupling capacitance present between the parallel pads of two chip, and C_{c1} and C_{c2} are the cross-coupling capacitance present between the parallel pads of two chip.

The proposed 4-port structure is used to represent two adjacent capacitive coupling interconnection pads. The effects of the data links as well as cross-coupling to adjacent channel can then be observed using Ansoft High Frequency Structure Simulation (HFSS). The coupling effects were observed in Figure 3 by the simulation results of S-parameters. The range of the simulation frequency is from 1GHz to 10GHz. The adjacent path space is 2 μm and gap distance of interchips is 4 μm.

B. Data link architecture

A transceiver system using capacitive coupling technique is shown in Fig. 4. The fully differential signaling is applied to improve common mode noise rejection. The transmitter (T_X) and the receiver (R_X) are designed on two F2F stacked chips.

Chip 1 is designed as transmitter (T_x) chip and Chip 2 is the receiver (R_x) chip. The top metal layer of Chip 1 and Chip 2 is used to create coupling electrodes. Two chips are stacked F2F and transmitters (T_x) and receivers (R_x) are implemented on each chip and are coupled by the metal electrodes of capacitive. The effect of the parasitic capacitor is denoted as C_r. The coupling capacitor C_c determines the strength of the

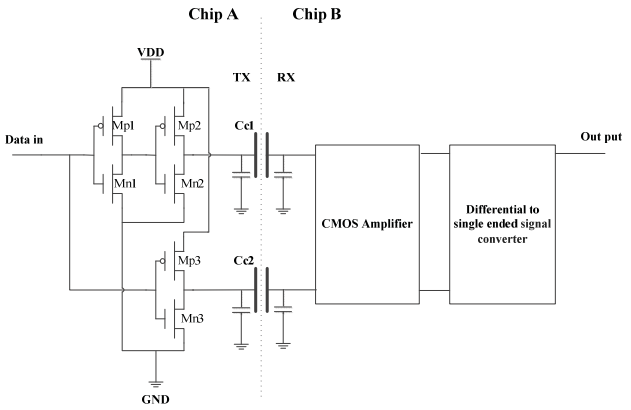


Fig. 4. Schematic for A capacitive coupling interconnection

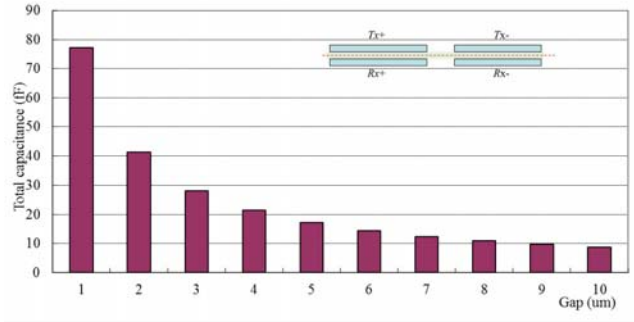


Fig. 5. Estimated equivalent capacitance values against different gap of coupling pad.

receiving signal at the input pad of receiver. The coupling capacitance can be estimated as parallel plate capacitors and is given as:

$$C_c = \varepsilon_r \varepsilon_0 \frac{A}{H} \quad (1)$$

where ε_r is the dielectric constant of the material between the pads, ε_0 is a constant called the "permittivity of free space" (There is a value of 8.85×10^{-12} C^2 / N-m^2 in SI units), A is the electrode area of the coupling pads, H is the gap distance between the two coupling pads. However, Eq. (1) is only valid when $A>>H$ and the coupling capacitance is sensitive to both the vertical gap distance (H) between the two coupled metal. In order to increase interconnection efficiency, an accurate alignment and a precise inter-electrode spacing are extremely important.

A coupling pad with a space of 2 μm and an area of 100 μm × 100 μm is used for the simulation. Figure 5 shows the estimated minimum C_{c1}/C_{c2} coupling capacitance against the different gap distance between a transceiver (Tx) and a receiver (Rx) circuit. It is obvious that an increase of gap distance leads to a weaker coupling effect due to the decrease in equivalent capacitance. The result has shown that decreasing the gap distance will increase the coupling capacitance and thus reduce the signal attenuation. The signal attenuation of receiver (Rx) due to the small coupling capacitance of a receiver circuit limits the maximum gap between two coupling pads.

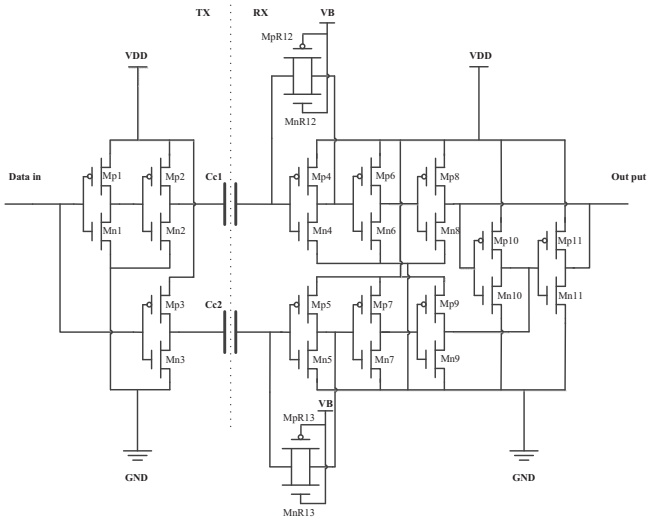


Fig. 6. Basic schematic of the proposed AC-coupled transceiver.

III. TRANSCEIVER CIRCUIT DESIGN

The schematic of the proposed CCI transceiver, which include a transmitter (Tx) and a receiver (Rx) is shown in Fig. 6. A three stage CCI is designed using 1P6M 0.18μm CMOS technology provided by TSMC with 1.8 volts power supply. The receiver (Rx) circuit consists of a pre-amplifier, input DC voltage bias (VB), a loopback transmission-gate, a digital signal amplifier, and a digital comparator. The input stage of the receive circuit includes CMOS pre-amplifier inverters (Mp4/Mn4, Mp5/Mn5) and transistors MP6~9 and MN6~9, senses differential signal pluses and converts them into single-end signal pulses. The CMOS pre-amplifier inverters have a large (negative) gain when its input is biased to 0.9 V (VDD/2). These four transistors (MpR12~13 and MnR12~13) perform as negative feedback resistors whose resistance value are adjusted by an input DC bias VB. In the stage, the transmission-gate function as negative feedback (MpR12~13 and MnR12~13) path can clamp the input bias at the point of half supply voltage such that inverter Mp4/Mn4 and Mp5/Mn5 can behavior as amplify and obtain the largest small-signal gain. The next stage, the receiver circuit of the cross CMOS inverter (Mp10/Mn10 and Mp11/Mn11) can be used to reduce the noise. The differential driver with tapped buffer inserted can drive the output pad around 1 pf and converts input signals into full swing digital signals for digital scope measurement.

IV. SIMULATION RESULTS

The CMOS inverter and feedback transmission-gate at the receiver-end can be used to control the high-gain signal effect of amplification. The simulation results are performed at VDD=1.8V and VB=0.69 at different temperatures -40 ^oC, 0 ^oC, 50 ^oC, 85 ^oC, 100 ^oC. The gain of the feedback amplifier is 17 dB. When the bias voltage (VB) is set to 0.69V, it can make the coupling signal obtain the maximum amplification

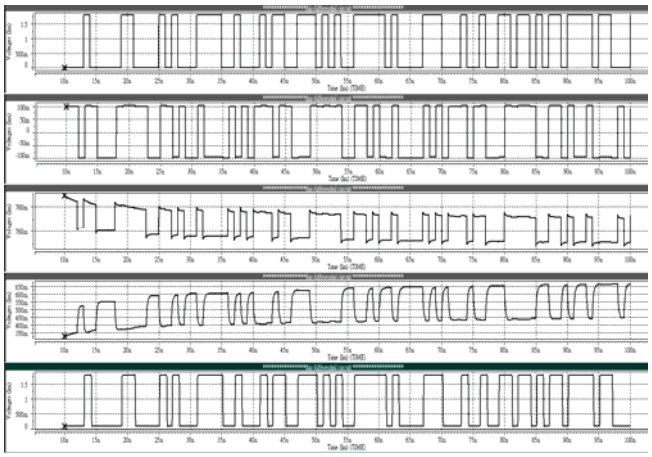


Fig. 7. Simulation results based on Fig. 6 at different node

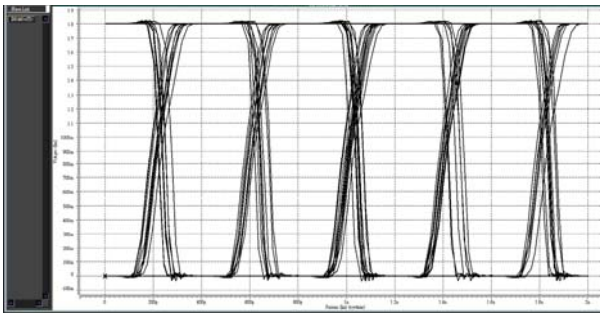


Fig. 8. Simulation results for eye diagram at 2.5G

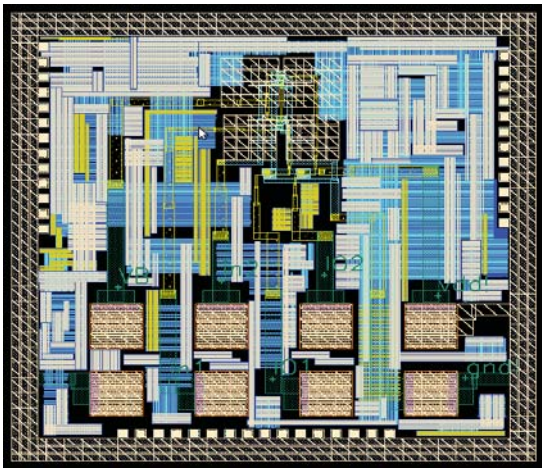


Fig. 9. Micrograph of the test chip layout.

efficiency. The testing signal input to the Tx node is transmitted to the Rx node using CCI coupling interconnection. The simulation results of the testing signals transmitted at different nodes are depicted in Figure 7. The input signals intend adding noise signal are subtracted away by the proposed circuit with a differential receiver.

For signal integrity analysis, the technology file 0.18μm TSMC library was used for the simulation of the eye diagram. The simulation result at 2.5 Gbps is depicted in Fig. 8. The static power consumption of the CMOS preamplifier is quite negligible. Total power dissipation is 80μW. Figure 9 shows the test chip layout using TSMC 1.8V 0.18um CMOS process. The estimated chip size is 1000μm × 1000μm.

V. Conclusion

In this work a difference CCI is designed using 0.18μm 1P6M CMOS technology provided by TSMC with 1.8 volts power supply. The power dissipation P_{avg} is 80μW for clock signal transmission with electrodes size of 100 × 100μm^2. The simulation results indicated the proposed circuit not only has the self-test characteristics but also is suitable for high-speed interconnected applications with differential signal transmission up to 2.5 Gbps.

Acknowledgment

This work was supported in part by the National Science Council, Taiwan, under Grants NSC 101-2221-E-214 -077 -.

References

[1] The International Technology Roadmap for Semiconductors (ITRS), Semiconductor Industry Association (SIA), 2007.

[2] B.W. Lee, J.Y. Tsai, H. Jin, C.K. Yoon, and R.R. Tummala, “New 3-D Chip Stacking Architectures by Wire-on-Bump and Bump-on-Flex,” IEEE Transactions on Advance Packaging, vol.31, 2008, pp.367-376.

[3] T. Ezaki, K. Kondo, H. Ozaki, N. Sasaki, H. Yonemura, M. Kitano, S. Tanaka, and T. Hirayama, “A160 Gb/s interface design configuration for multichip LSI,” IEEE International Digest of Technical Papers. ISSCC. 2004, Feb. 2004, pp. 140-141.

[4] K. Kumagai, C. Yang, H. Izumino, N. Narita, K. Shinjo, S. Iwashita, Y. Nakaoka, T. Kawamura, H. Komabashiri, T. Minato, A. Ambo, T. Suzuki, Z. Liu, Y. Song, S. Goto, T. Ikenaga, Y. Mabuchi, and K. Yoshida, “System-in-silicon architecture and its application to H.264/AVC motion estimation for 1080HDTV,” IEEE International Digest of Technical Papers. ISSCC. 2006, Feb. 2006, pp. 430–431.

[5] J. Burns, L. McIlrath, C. Keast, C. Lewis, A. Loomis, K. Warner, and P. Wyatt, “Three-dimensional integrated circuits for low-power, high-bandwidth systems on a chip,” IEEE International Digest of Technical Papers. ISSCC. 2001, Feb. 2001, pp. 268-269.

[6] R. Berger,J.A. Burns, C.K. Chen, J.M. Knecht, R.D. Lambert, K.L. Newcomb, D.M. O'Mara, D.D. Rathman, D.C. Shaver, A.M. Soares, C.N. Stevenson, B.M. Tyrrell, K. Warner, B.D. Wheeler, D.-R.W. Yost, and D.J. Young, “Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology,” Digest of Technical Papers. ISSCC. 2005 IEEE International, Feb. 2005, pp. 356–357.

[7] Demystifying 3D ICs: The pros and cons of going vertical, http://www.ece.ncsu.edu/muse/papers/dtoc2005.pdf, 9/5/2007

[8] J.Xu, J. Wilson, S. Mick, L. Luo, and P. Franzon, “2.8 Gb/s inductively coupled interconnect for 3D ICs,” Digest of Technical Papers. 2005 Symposium on VLSI Circuits, pp. 352-355, Jun. 2005.

[9] B. Su, P. Patel, S. Hunter, M. Caises, and P. Franzon, “AC coupled backplane communication using embedded capacitor,” Proceedings, IEEE Conference on Electrical Performance of Electronic Packaging, 2008, pp. 295-298.

[10] L. Luo, J. M. Wilson, S. E. Mick, J. Xu, L. Zhang, and P. Franzon, “3 Gbps AC coupled chip-to chip communication using a low swing pulse receiver,” IEEE Journal of Solid-State Circuits, Vol. 41, No. 1, 2006, pp. 287-296.

[11] G. S. Kim, M. Takamiya, and T. Sakurai, "A 25-mV-Sensitivity 2-Gb/s Optimum-Logic-Threshold Capacitive-Coupling Receiver for Wireless Wafer Probing Systems," IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 56, Sept. 2009, pp.709-713.