Failure Analysis on Gate-Driven ESD Clamp Circuit after TLP Stresses of Different Voltage Steps in a 16-V CMOS Process

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***Abstract* -- The ESD robustness of gate-driven ESD clamp circuit in a 16-V CMOS process was investigated by the stresses of transmission line pulse (TLP), human-body-model ESD test, and machine-model (MM) ESD test. After TLP stresses of different voltage steps, the same ESD clamp circuit got different secondary breakdown currents (It2). In order to understand such unusual phenomenon, the failure analysis on the TLP-stressed ESD clamp circuits was performed to find the failure mechanism.**

I. Introduction

Recently, the high-voltage (HV) CMOS technology has been developed and used to implement the display driver circuits, power switch, motor control systems, and so on [1], [2]. Among the various reliability specifications, electrostatic discharge (ESD) protection is an important issue in HV ICs. Therefore, circuits fabricated in high-voltage CMOS processes need the adequate protection design for high ESD reliability. In order to protect the internal circuits from ESD damage, ESD protection circuits must be applied to all input/output (I/O) pads and the power (VDD/VSS) pads. The typical whole-chip ESD protection design is shown in Fig. 1 realized with the power-rail ESD clamp circuit between the VDD and VSS power lines [3]. The internal circuits of an IC can be efficiently protected against ESD stress, due to the fast turn-on operation of the power-rail ESD clamp circuit.

With a high operating voltage, the fabrication cost and process complexity is increased in HV ICs. According to the extremely strong snapback phenomenon in the HV NMOS device during ESD stress, the traditional design using HV gate-grounded NMOS (GGNMOS) with a large device dimension was reported to suffer the non-uniform turn-on phenomenon [4]. Such a large device did not have a high ESD robustness after entering the snapback breakdown region. This is attributed to the current crowding effect among the multiple fingers and then inducing inhomogeneous triggering of the parasitic BJT to cause only several fingers of the device turned on under ESD stress [5]-[7]. Therefore, to efficiently improve the turn-on uniformity among those multiple fingers, the gate-driven design has been reported to increase ESD robustness of the device with large dimension [8], [9].

To verify the ESD protection capability, several methods have been commonly used, including transmission line pulse (TLP) [10], human-body-model (HBM) ESD test, and machine-model (MM) ESD test. Some studies on the correlation among those tests had been reported [11]. Based on the theoretical analysis and experimental data reported in the past, the TLP-measured It2 multiplied by the 1.5-kΩ resistance from the HBM model was approximately equal to the HBM voltage level of an ESD protection design.

In this work, a gate-driven ESD clamp circuit has been fabricated in a 16-V CMOS process and used to investigate its ESD robustness from the estimation of traditional correlation with It2. However, there is an obvious deviation of ESD robustness between TLP-measured It2 and HBM ESD test results. To further study this exceptionally un-correlated test result, the failure analysis on the gate-driven ESD clamp circuit after TLP stresses of different voltage steps was applied. After the stresses, the failure samples were de-layered to find the failure location on the ESD device with SEM pictures.

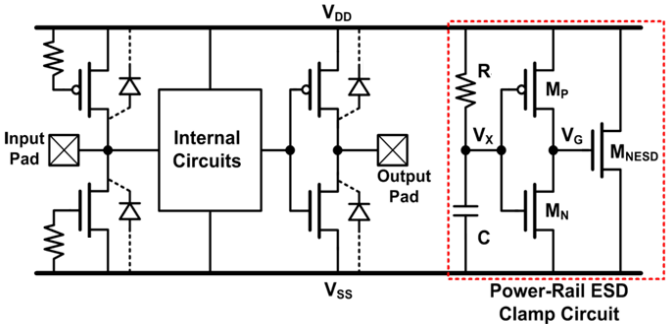


Fig.1. Typical whole-chip ESD protection design with the power-rail ESD clamp circuit.

II. Implantation of ESD Clamp Circuit in a HV Process

The device cross-sectional view of 16-V NMOS is shown in Fig. 2. In this structure, the n-type double diffusion (NDD) region is used to sustain the requested high operating voltage. The circuit scheme and the layout top view of the whole gate-driven ESD clamp circuit are shown in Figs. 3(a) and 3(b), respectively, where the *W/L* of HVM_{NESD} is drawn as 1500 μm /1.2 μm. The device dimensions in the ESD-transient detection circuit are chosen as R_1 = 200 kΩ, *C* of HVM_{CAP} = 1 pF, *W/L* of HVM_{P1} = 100 μm /1.3 μm, and *W/L* of HVM_{N1} = 20 μm /1.2 μm. The resistor of 200 kΩ is realized by a P+ poly resistance, and the capacitor of 1 pF is realized by a HV NMOS device. The *RC* time constant in the ESD-transient detection circuit is designed

around ~0.2 μs in this work to distinguish the ESD transient event from the power-on transition. Such a gate-driven ESD clamp circuit has been often used in the modern CMOS ICs.

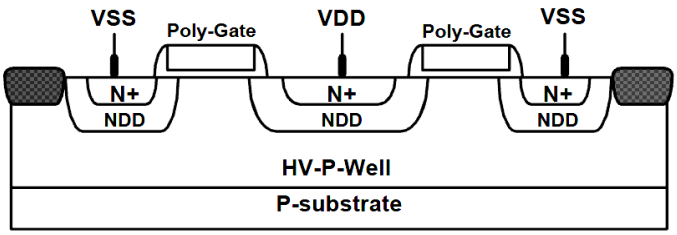
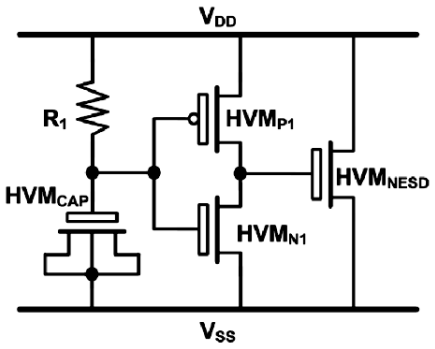
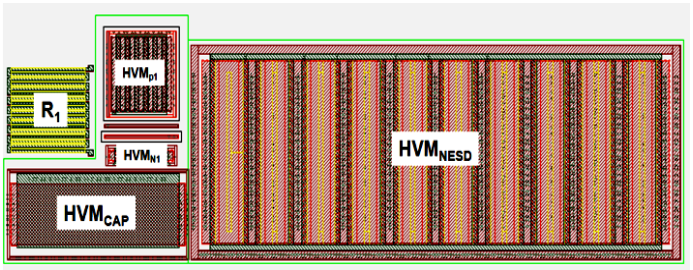


Fig.2. Device cross-sectional view of HV NMOS in a 16-V CMOS process.



(a)



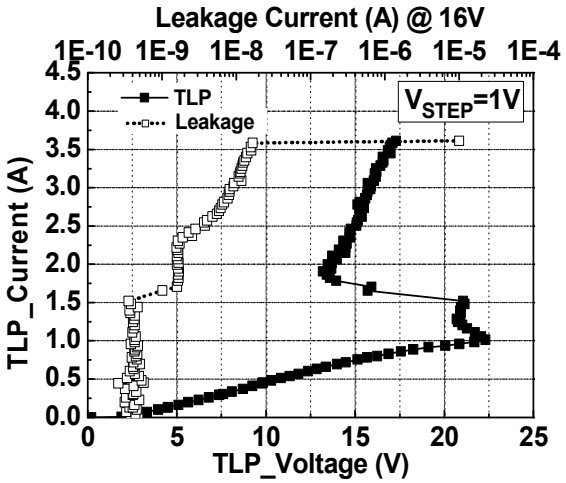
(b)

Fig.3. (a) The circuit scheme, and (b) the layout top view, of the gate-driven ESD clamp circuit in a 16-V CMOS process.

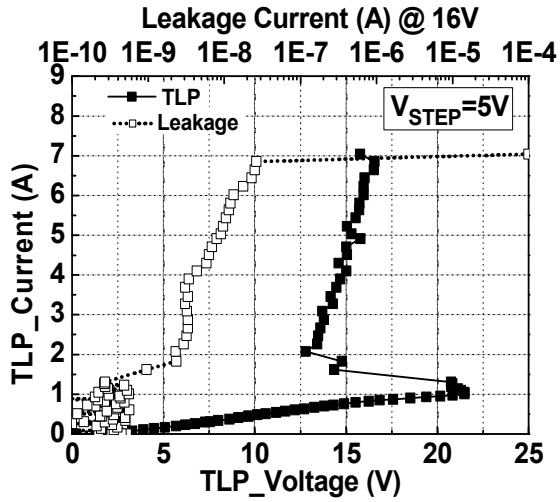
III. Experimental Results

A. ESD Robustness of ESD Clamp Circuit

ESD robustness of the ESD clamp circuit is measured by TLP, HBM, and MM tests. A pulse width of 100 ns and a rise time of 10 ns are used in the TLP measurement setup. The failure criterion for It2 measurement is determined by leakage current which is greater than 1 μA under voltage bias of 16 V. The voltage steps of TLP test are applied with 1 V, 5 V, and 10 V. The HBM and MM levels of the ESD clamp circuit are measured by the ESD tester, and the failure criterion is defined as the leakage current which is greater than 1 μA under voltage bias of 16 V. The voltage step of HBM test is 500 V, and the voltage step of MM test is 50 V. Fig. 4(a), 4(b), and 4(c) show the TLP-measured *I-V* characteristics of the gate-driven ESD clamp circuit with different voltage steps of 1 V, 5 V, and 10 V, respectively.



(a)



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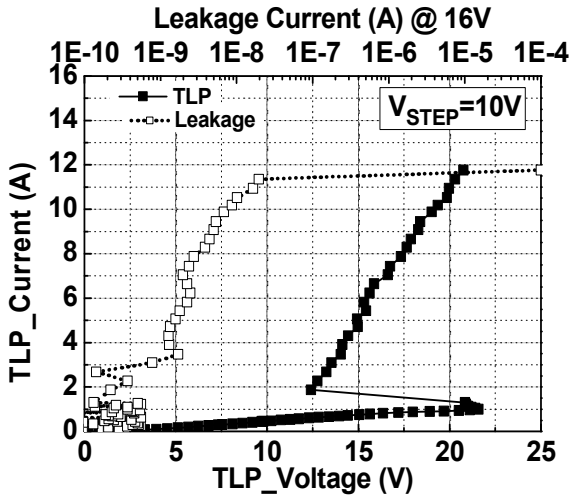

(c)

Fig.4. TLP-measured *I-V* characteristics of the gate-driven ESD clamp circuit with different voltage steps of (a) 1 V, (b) 5 V, and (c) 10 V.

From the TLP-measured *I-V* characteristics with different voltage steps in Fig. 4, the TLP-measured currents of the same ESD clamp circuit are ~1A before the HVM_{NESD} enters the snapback region. After the snapback occurs, the TLP-measured current is increased greatly when the applied TLP voltage is increased. However, the leakage current after snapback is also slightly increased (before the secondary breakdown point). When a 1-V voltage step is applied in the TLP test, the It2 is 3.58 A. When the voltage step is increased to 5 V, the It2 is increased to 7 A. Finally, with a 10-V voltage step, the It2 can be further increased up to 11.7 A. The dependency of TLP-measured It2 on the voltage step of TLP test is shown in Fig. 5. The TLP-measured It2 was increased when the voltage steps increasing.

The experimental results are summarized in Table I, including TLP, HBM, and MM tests. The ESD clamp circuit has ESD levels of over 8 kV in HBM and ~600 V in MM tests. From the correlation equation of 3.58 A × 1.5 kΩ = 5.37 kV, the TLP-measured It2 with 1-V voltage step has the estimated HBM level of 5.37 kV, which is lower than the ESD level (> 8kV) verified from the HBM ESD tester. The test results have an obvious deviation between TLP and HBM tests.

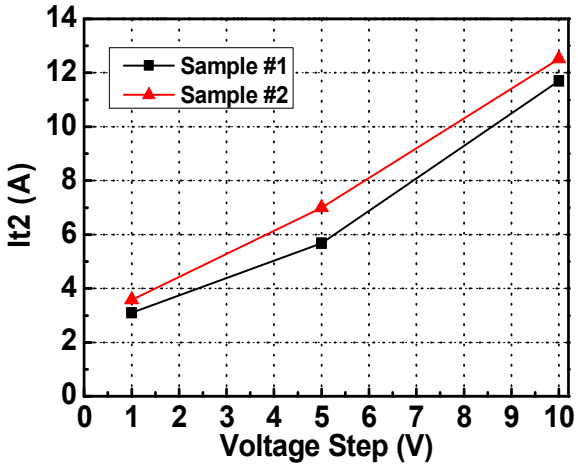

Fig. 5. Dependency of TLP-measured It2 on the voltage step of TLP test applied to the same ESD clamp circuit.

Table I
ESD ROBUSTNESS OF THE GATE-DRIVEN ESD CLAMP CIRCUIT

ESD Clamp Circuit	TLP			ESD tester	
				Positive mode	
	It2 (A) (V_{STEP}=1V)	It2 (A) (V_{STEP}=5V)	It2 (A) (V_{STEP}=10V)	HBM (kV)	MM (V)
Sample #1	3.58	7	12.52	>8	600
Sample #2	3.1	5.68	11.7	>8	650

B. Failure Analysis after TLP Stress

In order to investigate the physical failure mechanism of the identical ESD clamp circuits after TLP test of different voltage steps, the failure analysis is applied to seek the failure locations. In Fig. 6(a), with 1-V voltage step in TLP test, the failure locations are mainly located on few fingers of the HVM_{NESD} device near to the ESD detection circuit. In Figs. 6(b) and 6(c), with 5-V and 10-V voltage steps in TLP test, the failure locations are extended into more fingers of the HVM_{NESD} device. From the failure analysis pictures and TLP-measured results, non-uniform turn-on phenomenon among the multi-fingers of HVM_{NESD} device become worse, especially when the TLP test is applied with small voltage step.

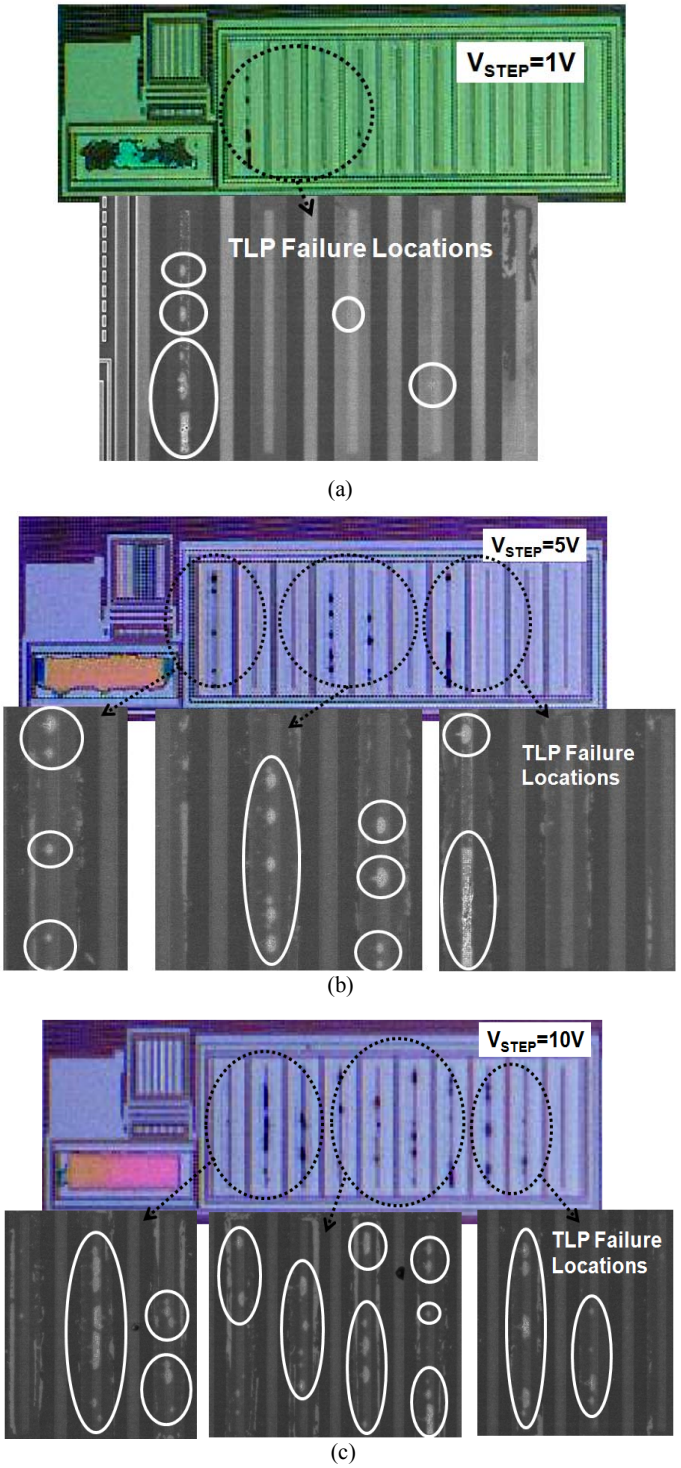

Fig.6. The OM and SEM pictures of the gate-driven ESD clamp circuit after TLP stresses with different voltage steps of (a) 1 V, (b) 5 V, and (c) 10 V.

One similar TLP test with different voltage steps on a single finger of HV GGNMOS was ever studied in a 0.5-μm 43-V process [12]. During snapback region, the impact ionization hot spot was located at N+ region which is close to the field oxide due to Kirk effect [13]. As a result, hot carriers could be injected into the oxide and trapped there easily. The increase of TLP-measured leakage current might reflect the device degradation due to charge trapping in gate oxide.

C. Failure Analysis after MM ESD Test

To further investigate the non-uniform turn-on phenomenon, the failure analysis on the ESD clamp circuit after MM ESD test is shown in Fig. 7. After a 650-V MM ESD stress, the failure locations are located at all the fingers of HVM_{NESD} device. Among the TLP, HBM, and MM tests, the obvious difference is the zapping times. The more zapping times was applied, the HVM_{NESD} device suffered the higher cumulative energy. As a result, the cumulative energy during the TLP stresses of small voltage step is larger than that in HBM and MM tests. The experimental results indicated that the cumulative energy induce such a variation of the TLP-measured It2.

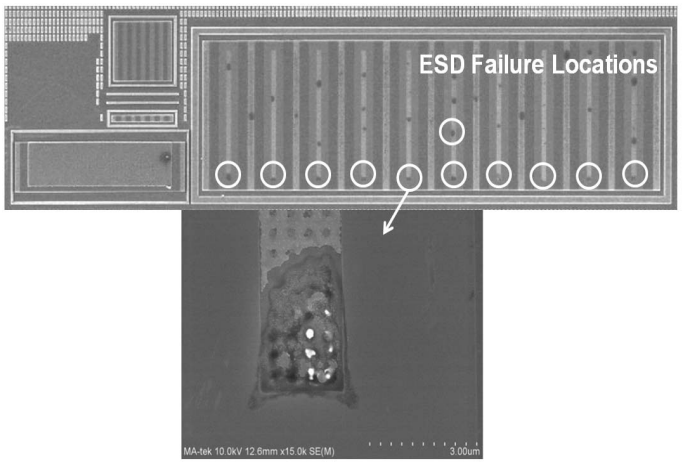

Fig.7. The SEM picture of ESD clamp circuit after 650-V MM ESD stress.

IV. CONCLUSION

The gate-driven ESD clamp circuit in a 16-V CMOS process has been fabricated to investigate its ESD robustness from the estimation of traditional correlation. From the failure analysis, the reason to cause a deviation between TLP and HBM tests has been found. With different cumulative energy caused by different voltage steps in TLP test, different It2 values are obtained on the same ESD clamp circuit. As the voltage step is increased from 1V to 10V, the circuit exhibits higher TLP-measured It2 and the failure sites become more evenly distributed among the multiple fingers of HV NMOS, indicating that the device has been uniformly turned on. This phenomenon can also be found in the failure analysis of MM test results. Therefore, in order to get the TLP-measured It2 with well HBM correlation, the voltage-step dependency should be taken into consideration during TLP measurement, especially in the high-voltage CMOS processes.

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