

ESD Protection Structure with Inductor-Triggered SCR for RF Applications in 65-nm CMOS Process

Chun-Yu Lin¹, Li-Wei Chu¹, Ming-Dou Ker¹, Ming-Hsiang Song², Chewn-Pu Jou², Tse-Hua Lu², Jen-Chou Tseng², Ming-Hsien Tsai², Tsun-Lai Hsu², Ping-Fang Hung², and Tzu-Heng Chang²

¹ National Chiao-Tung University, Hsinchu, Taiwan

² Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

Abstract — To protect radio-frequency (RF) integrated circuits from electrostatic discharge (ESD) damages, silicon-controlled rectifier (SCR) devices have been used as main on-chip ESD protection devices due to their high ESD robustness and low parasitic capacitance in nanoscale CMOS technologies. In this work, the SCR device assisted with an inductor to resonate at the selected frequency band for RF performance fine tune was proposed. Besides, the inductor can be also designed to improve the turn-on efficiency of the SCR device for ESD protection. Verified in a 65-nm CMOS process, the ESD protection design with the inductor-triggered SCR for 60-GHz RF applications can achieve good RF performances and high ESD robustness.

Keywords – Electrostatic discharge (ESD), radio-frequency (RF), silicon-controlled rectifier (SCR).

I. INTRODUCTION

Among the electrostatic discharge (ESD) protection devices, the silicon-controlled rectifier (SCR) device has been reported to be useful for ESD protection on radio-frequency (RF) integrated circuits due to its high ESD robustness within a small layout area and low parasitic capacitance [1]. The device structure of the SCR device is illustrated in Fig. 1. The SCR path between RF input (RF_{IN}) and V_{SS} consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between RF_{IN} and V_{DD} consists of P+ and N-well/N+. The equivalent circuit of the SCR consists of a PNP BJT and an NPN BJT. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To enhance the turn-on efficiency of SCR, some designs have been presented, such as the gate-coupled, substrate-triggered, GGNMOS-triggered, and diode-triggered techniques [2]. However, adding the traditional trigger design to SCR device also increases the parasitic capacitance seen at the RF_{IN} pad, which is hard to be tolerable for RF circuits, as the operating frequencies continuously increase [3]. Therefore, a novel trigger design for SCR device is needed.

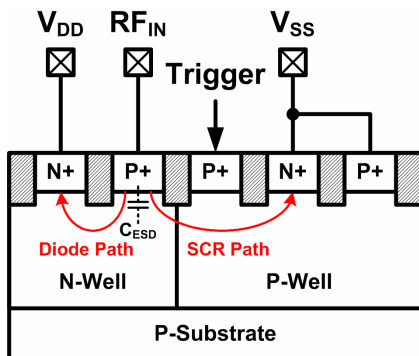


Figure 1. Device cross-sectional view of SCR device used in RF input pad.

II. REALIZATION OF INDUCTOR-TRIGGERED SCR

The new proposed inductor-triggered SCR (LTSCR) is shown in Fig. 2, which consists of an SCR device, an inductor (L_{trig}), and a MOS transistor (M_{trig}). The PMOS transistor is selected for M_{trig} since it exhibits the initial-on function for ESD protection, which can quickly pass the trigger signal to SCR device [4]. The resistor and capacitor used in the power-rail ESD clamp circuit can also be used to control the PMOS in LTSCR.

In this ESD protection scheme, the dimensions of the inductor, PMOS transistor, SCR device, and diode can be designed to minimize the RF performance degradation. Since the capacitor used in power-rail ESD clamp circuit is large enough (~ 10 pF) to keep the node between resistor and capacitor at ac ground under normal RF circuit operating conditions, the impedance of the trigger path (Z_{trig}) seen at the RF_{IN} pad to ground can be calculated as

$$Z_{\text{trig}} \approx j\omega L_{\text{trig}} + \frac{1}{j\omega C_{\text{trig}}} = j\omega \left(L_{\text{trig}} - \frac{1}{\omega^2 C_{\text{trig}}} \right) \quad (1)$$

where the ω is the angular frequency and the C_{trig} can be expressed as

$$C_{\text{trig}} \approx C_{\text{gs}} + C_{\text{gb}} + C_{\text{db}}. \quad (2)$$

The C_{gs} , C_{gb} , and C_{db} denote the gate-to-source capacitance, gate-to-body capacitance, and drain-to-body capacitance of the M_{trig} , respectively. The resonance angular frequency (ω_0), which is designed to be the operating frequency of RF signal, can be obtained by

$$\omega_0 = \frac{1}{\sqrt{\left(L_{\text{trig}} - \frac{1}{\omega_0^2 C_{\text{trig}}} \right) C_{\text{ESD}}}} \quad (3)$$

where the C_{ESD} is the parasitic capacitance contributed by the SCR and D_N . The sizes of SCR and D_N depend on the required ESD robustness, while the size of M_{trig} transistor depends on the required trigger current. Once the sizes of M_{trig} transistor, SCR, and D_N have been chosen, the required L_{trig} can be determined.

The inductor is also used to provide the trigger path between the RF_{IN} pad and the trigger port of SCR device under ESD stress conditions. The PMOS transistor at the trigger path, which is controlled by the RC-based ESD detection circuit, is also turned on under ESD stress conditions. The M_{trig} is turned

off to block the steady leakage current path from the RF_{IN} pad to the trigger port of SCR device under normal RF circuit operating conditions. Under ESD stress conditions, the trigger signal can pass from the RF_{IN} pad to the trigger port of SCR device, so the SCR device can be fast turned on to discharge ESD current. Fig. 2 also shows the ESD current paths under positive-to- V_{SS} (PS), positive-to- V_{DD} (PD), negative-to- V_{SS} (NS), and negative-to- V_{DD} (ND) ESD stress conditions. The proposed ESD protection scheme can provide the corresponding current discharging paths.

A commercial 65-nm CMOS technology is used to implement the test circuits in this work. The device dimensions of the test circuits are listed in Table I. The ESD protection circuit with the inductor-triggered SCR is designed for 60-GHz RF applications. The test patterns include the test circuits A, B, C, and D. The size of SCR device used in the test circuits A, B, C, and D are split as 8 μm , 15 μm , 23 μm , and 30 μm , respectively. The size of D_N in test circuits A, B, C, and D are split as also 8 μm , 15 μm , 23 μm , and 30 μm , respectively. The parasitic capacitance (C_{ESD}) of ESD protection devices in test circuits A, B, C, and D at 60 GHz are estimated as ~ 25 fF, ~ 50 fF, ~ 75 fF, and ~ 100 fF, respectively. The width / length of PMOS (M_{trig}) in each test circuit is kept at 100 μm / 0.2 μm , and the equivalent C_{trig} is ~ 50 fF at 60 GHz. Therefore, the required inductors (L_{trig}) are ~ 0.38 nH, ~ 0.27 nH, ~ 0.23 nH, and ~ 0.2 nH for the test circuits A, B, C, and D, respectively.

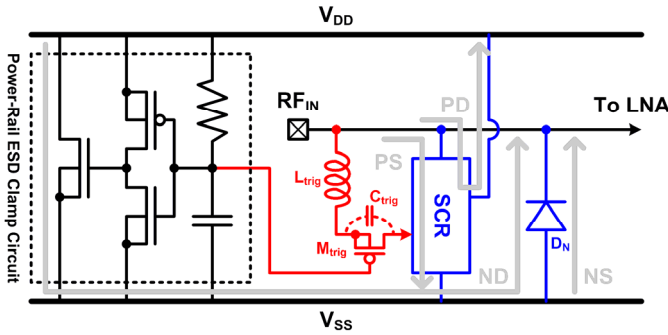


Figure 2. Proposed inductor-triggered SCR for RF ESD protection.

III. SIMULATION RESULTS

A. RF Performances

The RF characteristics of the test circuits are simulated by using the microwave circuit simulator ADS with the designed device dimensions. Since the SCR model is not provided in the given CMOS process, diodes with P+/N-well, N+/P-well, and N-well/P-well junctions are used to simulate the SCR devices. A signal source with 50- Ω impedance drives the port 1 (RF_{IN} pad) of the test circuit, and a 50- Ω load is connected to the port 2 to simulate the RF receiver. The voltage supply of V_{DD} (V_{SS}) is 1 V (0 V), and the dc bias of RF_{IN} is 0.5 V ($V_{DD}/2$). The simulated transmission (S_{21}) parameters are shown in Fig. 3(a). At 60-GHz frequency, the test circuits A, B, C, and D have about 0.5-dB, 0.8-dB, 1.2-dB, and 1.5-dB power loss, respectively. Although the parasitic capacitance of the ESD protection devices can be resonated out, the losses are still contributed by the parasitic resistance of the SCR and D_N . The

reflection (S_{11}) parameters are compared in Fig. 3(b). These ESD protection circuits exhibit good input matching (S_{11} -parameters < -10 dB) around 60 GHz. Since these test circuits exhibit good RF performances between 57–65 GHz, they can be operated at 60 GHz even if some variation happens on device values.

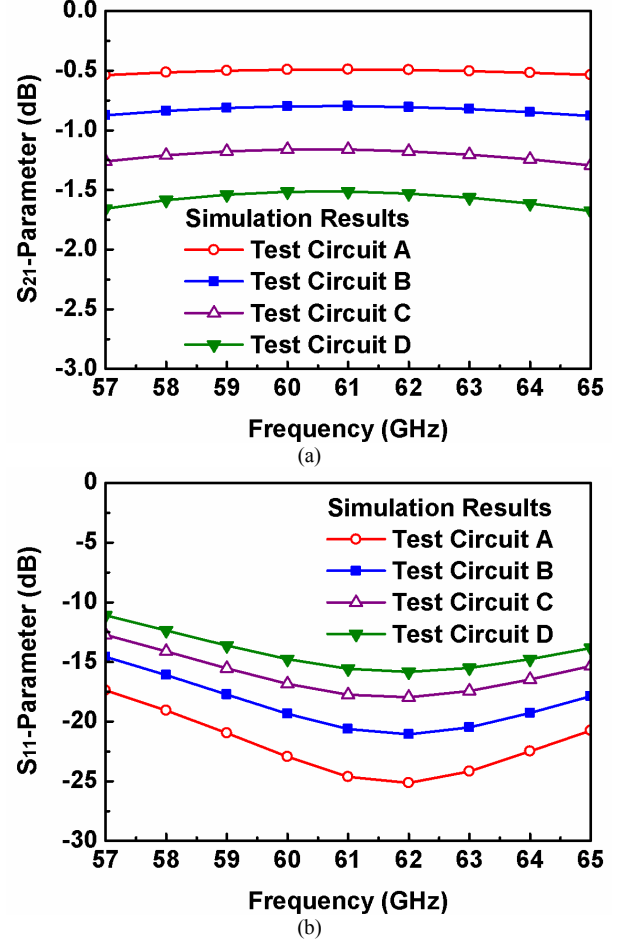


Figure 3. Simulation results of proposed ESD protection scheme on (a) S_{21} -parameter and (b) S_{11} -parameter.

B. ESD Transient Events

When a positive fast-transient ESD voltage is applied to RF_{IN} with V_{SS} grounded, the RC delay in the ESD detection circuit keeps the gate of M_{trig} at a relatively low voltage level compared to the fast rising voltage level at RF_{IN} . The M_{trig} can be quickly turned on by the ESD energy to generate the trigger signal into the trigger port of the SCR device. Finally, the SCR device can be fully turned on to discharge ESD current from RF_{IN} to V_{SS} . Figs. 4(a) and 4(b) show the simulated voltage waveforms of the test circuit D under the ESD transition events, where two 0-to-5 V voltage pulses with 10-ns and 0.1-ns rise time are applied to RF_{IN} to simulate the fast transient voltage of human-body-model (HBM) and charged-device-model (CDM) ESD events. With the limited voltage height of 5 V in the voltage pulse, the simulation results can check the desired trigger function before the RF circuit breakdown.

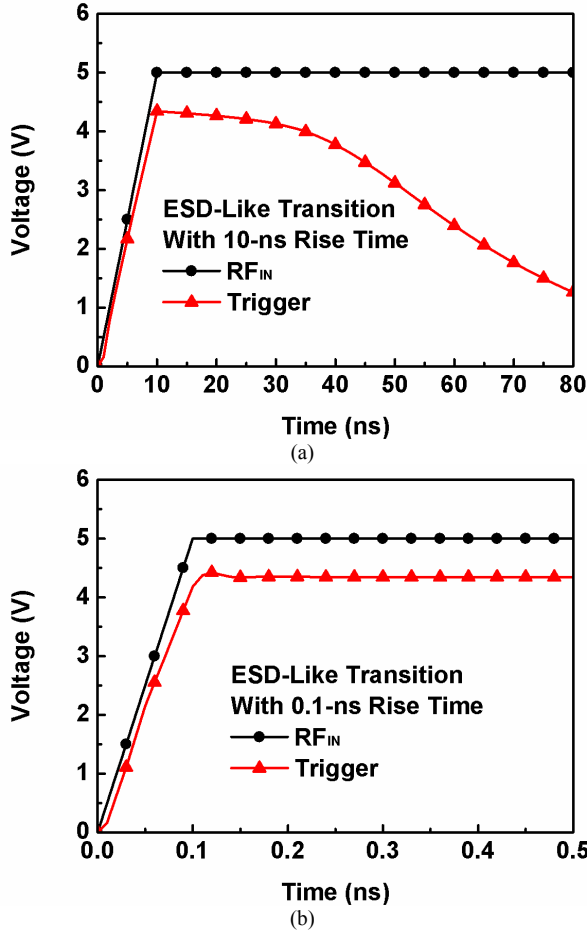


Figure 4. Simulated waveforms of proposed ESD protection scheme under ESD-like transition with (a) 10-ns and (b) 0.1-ns rise time.

IV. EXPERIMENTAL RESULTS

The test circuits of inductor-triggered SCR have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. One set of the test circuits are implemented with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port S-parameters measurement. The other set of the test circuits are implemented with the RF-NMOS emulators for ESD tests [5]. The RF-NMOS emulator, which consisted of one RF NMOS with gate terminal connected to the RF_{IN} pad, and the drain, source, and body terminals connected to V_{SS} pad, is used to simulate the RF receiver under ESD stress condition. The ESD robustness of the test circuits can be estimated by the test patterns with the RF-NMOS emulators.

In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the de-embedding technique. With the on-wafer RF measurement, the S-parameters of these four test circuits have been extracted from 0 to 67 GHz. The voltage supply of V_{DD} (V_{SS}) is 1 V (0 V), and the dc bias of RF_{IN} is 0.5 V (V_{DD}/2). The source and load resistances to the test circuits are kept at 50 Ω. The measured S₂₁-parameters and S₁₁-parameters versus frequencies among the four test circuits are shown in Figs. 5(a) and 5(b), respectively. As shown in Fig. 5(a), the test circuits A, B, C, and D have about 1.2-dB, 1.4-dB,

1.6-dB, and 1.8-dB power loss at 60-GHz frequency, respectively. These ESD protection circuits exhibit good input matching (S₁₁-parameters < -15 dB) around 60 GHz.

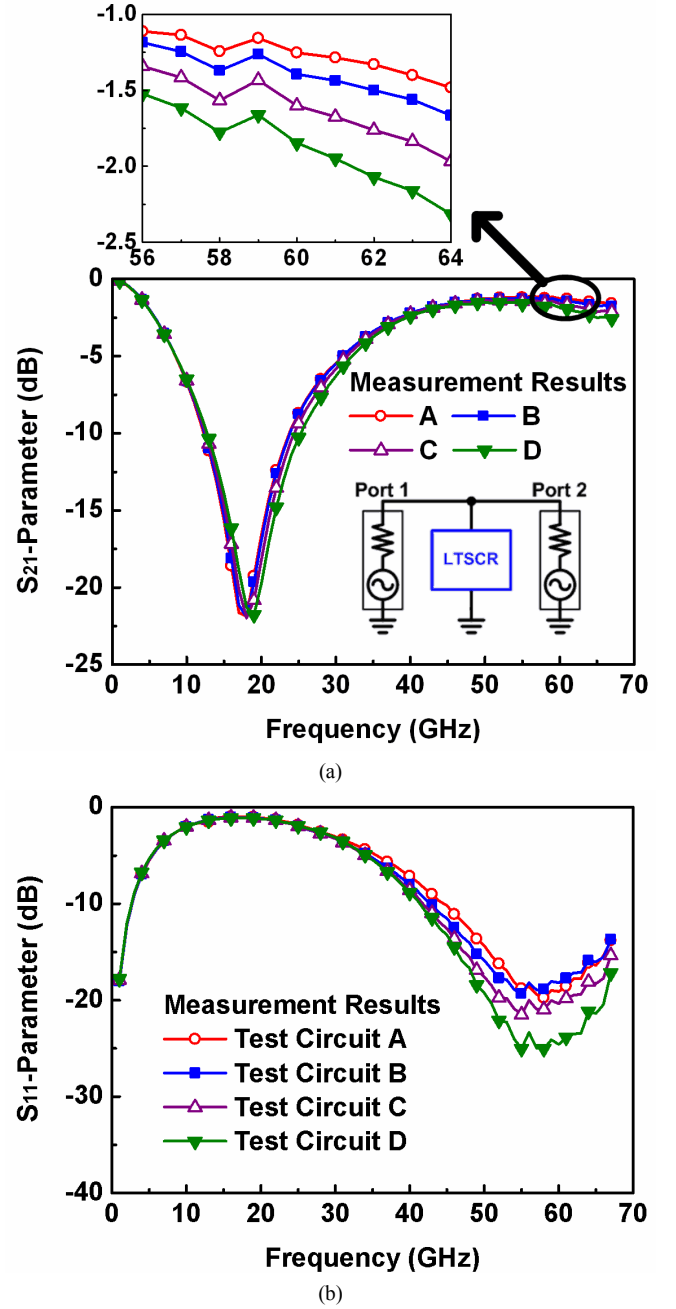


Figure 5. Measurement results of proposed ESD protection scheme on (a) S₂₁-parameter and (b) S₁₁-parameter.

To evaluate the ESD robustness, the human-body-model (HBM) ESD pulses are stressed to each test circuit under PS, PD, NS, and ND ESD stress conditions. The failure criterion is defined as the I-V characteristics seen at RF_{IN} shifting over 30% from its original curve after ESD stressed at every ESD test level. In other words, the leakage current under 1-V bias at RF_{IN} will not increase over 30 % if the test circuit is not failed after ESD stresses. The HBM ESD robustness among the four

test circuits with the proposed ESD protection designs are listed in Table I. The HBM ESD levels of the test circuits A, B, C, and D can achieve 0.75 kV, 1.5 kV, 2.25 kV, and 2.75 kV, respectively, which are obtained from the lowest levels among PS, PD, NS, and ND ESD tests. The HBM ESD robustness of the test circuits is almost proportional to the sizes of ESD protection devices (SCR and D_N). Fig. 6 shows the photograph of the test circuit D after 3-kV HBM ESD stress under PS mode. The failure point can be seen at the SCR since the SCR can sustain 2.75-kV HBM ESD stress.

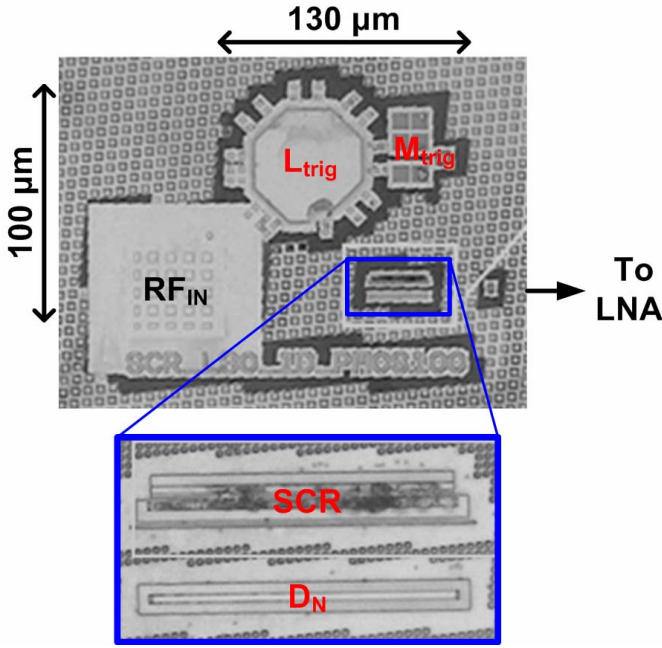


Figure 6. Photograph of test circuit D after 3-kV HBM ESD test under PS mode.

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the LTSCR, the transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulse width is used. The TLP-measured I-V curves of the test circuits A, B, C, and D under PS, PD, NS, and ND stress conditions are tested. Fig. 7 shows the PS-mode TLP-measured I-V curves. Once the ESD pulses stressed to the test circuits, all SCR devices can be quickly triggered on to discharge ESD currents. The secondary breakdown current (I_{t2}), which indicated the current-handling ability of ESD protection circuit, can also be obtained from the TLP-measured I-V curve. These secondary breakdown currents measured by TLP system are summarized in Table I. The turn-on behavior and the I_{t2} values of the ESD protection circuits can ensure the effective ESD protection capability of the proposed LTSCR.

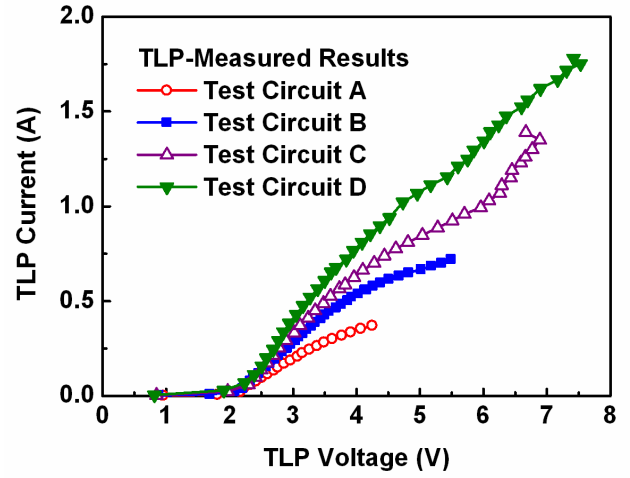


Figure 7. TLP-measured I-V characteristics among the four test circuits under PS mode.

Table I. Device dimensions and measurement results of ESD protection cells with inductor-triggered SCR.

			Test Circuits			
			A	B	C	D
Device Dimensions	SCR (μm)		8	15	23	30
	D_N (μm)		8	15	23	30
	L_{trig} (nH)		0.38	0.27	0.23	0.2
	M_{trig} ($\mu\text{m} / \mu\text{m}$)		100 / 0.2	100 / 0.2	100 / 0.2	100 / 0.2
	Area ($\mu\text{m} \times \mu\text{m}$)		120 x 150	110 x 140	105 x 135	100 x 130
Measurement Results	RF Performances	S_{11} at 60 GHz (dB)	-19.1	-18.2	-20.4	-24.6
		S_{21} at 60 GHz (dB)	-1.24	-1.39	-1.60	-1.84
	ESD Robustness	PS HBM (kV)	0.75	1.5	2.25	2.75
		PD HBM (kV)	1	1.5	2.25	2.75
		NS HBM (kV)	0.75	1.5	2.25	3
		ND HBM (kV)	0.75	1.5	2.25	3
		PS TLP-Measured I_{t2} (A)	0.37	0.72	1.39	1.78
		PD TLP-Measured I_{t2} (A)	0.41	0.81	1.38	1.72
		NS TLP-Measured I_{t2} (A)	0.49	0.82	1.45	1.75
		ND TLP-Measured I_{t2} (A)	0.48	0.82	1.39	1.73
		PS VF-TLP-Measured I_{t2} (A)	0.96	1.72	2.14	2.21

To evaluate the effectiveness of the proposed ESD protection circuit in faster ESD-transient events, another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulse width is also used in this study. The VF-TLP system can be used to capture the transient behavior of ESD protection circuit in the time domain of charged-device-model (CDM) ESD event [6]. The VF-TLP-measured I_{t2} of the four test circuits are also listed in Table I. The tests circuits A, B, C, and D with the RF-NMOS emulator can achieve VF-TLP-measured I_{t2} of 0.96 A, 1.72 A, 2.14 A, and 2.21 A, respectively. The proposed inductor-triggered SCR is fast enough to be turned on under such a fast-transient pulse.

V. CONCLUSION

The new ESD protection structure of the inductor-triggered SCR has been designed, fabricated, and characterized in a 65-nm CMOS process. The inductor-triggered SCR is designed to achieve low trigger voltage and high turn-on speed. Moreover, the inductor-triggered SCR can reach the input/output matching with low S_{11} -parameters and high S_{21} -parameters. This ESD protection structure is developed to support RF circuit designers for them to easily apply ESD protection in the 60-GHz RF circuits. Verified in a commercial 65-nm CMOS process, the test circuits A, B, C, and D have about 1.2-dB, 1.4-dB, 1.6-dB, and 1.8-dB power loss at 60 GHz, respectively. Besides, they can sustain 0.75-kV, 1.5-kV, 2.25-kV, and 2.75-kV HBM ESD tests, respectively. Therefore, the proposed ESD protection structure can be used to achieve good RF performance and high ESD robustness simultaneously.

ACKNOWLEDGEMENTS

This work was supported by Taiwan Semiconductor Manufacturing Company (TSMC), by National Science Council (NSC), Taiwan, under Contract of NSC 100-2221-E-009-048, and by the "Aim for the Top University Plan" of National Chiao-Tung University and Ministry of Education, Taiwan.

REFERENCES

- [1] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device and Materials Reliability*, vol. 5, no. 2, pp. 235-249, Jun. 2005.
- [2] M. Mergens, C. Russ, K. Verhaege, J. Armer, P. Jozwiak, R. Mohn, B. Keppens, and C. Trinh, "Diode-triggered SCR (DTSCR) for RF-ESD protection of BiCMOS SiGe HBTs and CMOS ultra-thin gate oxides," in *IEEE Int. Electron Devices Meeting Dig. Tech. Papers*, 2003, pp. 515-518.
- [3] S. Thijs, K. Raczkowski, D. Linten, M. Scholz, A. Griffoni, and G. Groeseneken, "CDM and HBM analysis of ESD protected 60 GHz power amplifier in 45 nm low-power digital CMOS," in *Proc. EOS/ESD Symp.*, 2009, pp. 329-333.
- [4] M.-D. Ker and S.-H. Chen, "Implementation of initial-on ESD protection concept with PMOS-triggered SCR devices in deep-submicron CMOS technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1158-1168, May 2007.
- [5] C.-Y. Lin, L.-W. Chu, and M.-D. Ker, "Design and implementation of configurable ESD protection cell for 60-GHz RF circuits in a 65-nm CMOS process," *Microelectronics Reliability*, vol. 51, no. 8, pp. 1315-1324, Aug. 2011.
- [6] C. Chu, A. Gallerano, J. Watt, T. Hoang, T. Tran, D. Chan, W. Wong, J. Barth, and M. Johnson, "Using VF-TLP data to design for CDM robustness," in *Proc. EOS/ESD Symp.*, 2009, pp. 286-291.