# Compact and Low-Loss ESD Protection Design for V-Band RF Applications in a 65-nm CMOS Technology

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***Abstract* — Nanoscale CMOS technologies have been widely used to implement radio-frequency (RF) integrated circuits. However, the thinner gate oxide and silicided drain/source in nanoscale CMOS technologies seriously degrade the electrostatic discharge (ESD) robustness of RF circuits. Against ESD damage, on-chip ESD protection design must be included in RF circuits. As the RF circuits operating in the higher frequency band, the parasitic effect from ESD protection devices and/or circuits must be strictly limited. To provide the effective ESD protection for a 60-GHz low-noise amplifier (LNA) with less RF performance degradation, a new ESD protection design was studied in a 65-nm CMOS process. Such ESD-protected LNA with simulation/measurement results has been successfully verified in silicon chip to to achieve the 2-kV HBM ESD robustness with the lower power loss in a smaller layout area.**

***Index Terms* — Electrostatic discharge (ESD), radio frequency (RF), V band.**

## I. Introduction

The radio-frequency (RF) integrated circuits have been widely designed and fabricated in CMOS processes due to the advantages of high integration and low cost for mass production. However, nanoscale CMOS technologies seriously degraded the electrostatic discharge (ESD) robustness of integrated circuits. ESD protection must be taken into consideration during the design phase of integrated circuits, especially the RF circuits [1]. In the RF circuits, the input and output pads are usually connected to the gate terminal or silicided drain/source terminal of the MOS transistor, which leads to a very low ESD robustness if no appropriate ESD protection design is applied. Once the RF circuit is damaged by ESD event, it can not be recovered and the RF functionality is lost. Therefore, on-chip ESD protection design must be provided for all input and output pads in RF circuits.

The ESD protection design for low-noise amplifier (LNA) is shown in Fig. 1, where an ESD protection circuit at RF input was assisted with the power-rail ESD clamp circuit to prevent LNA from ESD damage [2]. However, adding ESD protection circuit at RF input causes RF performance degradation with several undesired effects. The parasitic capacitance of ESD protection device is one of the most important design considerations for RF circuits. The parasitic capacitance of ESD protection device causes signal loss from the RF input to ground. A typical specification for a giga-Hz LNA on human-body-model (HBM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV and 200 fF, respectively [3]. To mitigate the performance degradation caused by ESD protection circuit, some design techniques had been developed to reduce the signal loss from ESD protection circuit [4]-[6]. As the operating frequencies of RF circuits increase, the parasitic capacitance was more strictly limited. In this paper, two new designs of the compact ESD protection circuits for V-band RF applications are proposed. Such ESD protection circuits have been designed for 60-GHz RF applications and verified in a 65-nm CMOS process.

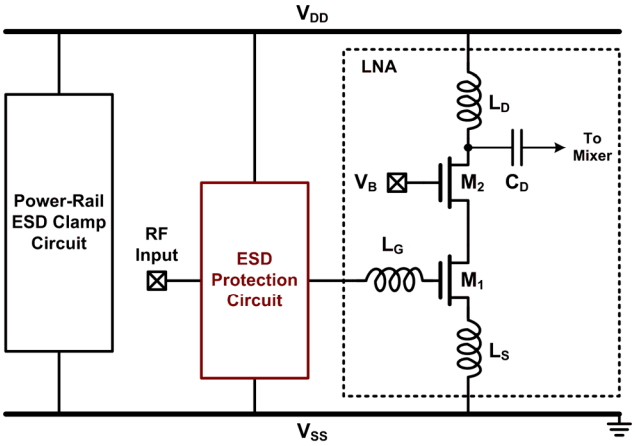


Fig. 1. ESD protection design for LNA.

## II. Proposed ESD Protection Circuits

Fig. 2(a) shows the circuit of one proposed ESD protection design, where a pair of the ESD protection diodes ($D_P$ and $D_N$) and a series inductor and capacitor ($L_N$ and $C_N$) are placed beside the RF input. The ESD protection diodes provide the ESD current paths between input and $V_{DD}$/$V_{SS}$. The power-rail ESD clamp circuit is also needed to provide the ESD current paths between $V_{DD}$ and $V_{SS}$.

The inductor in series with the capacitor can block the dc leakage path from RF input to $V_{SS}$ under normal circuit operating conditions. Besides, the series inductor and capacitor are designed to resonate at low frequency. As

the frequency is lower (higher) than the resonant frequency of the series inductor and capacitor, the capacitance (inductance) dominated the impedance. The equivalent inductance of the series inductor and capacitor ($L_{eq}$) can be expressed as

$$L_{eq} = L_N - \frac{1}{\omega^2 C_N} \quad (1)$$

At operating frequency of input RF signal, the inductance ($L_{eq}$) can be used to eliminate the parasitic capacitance of ESD protection diodes ($C_{Diodes}$). The resonant frequency of parallel $L_{eq}$ and $C_{Diodes}$, which is designed to be the operating frequency of RF circuit, can be obtained by

$$\omega_o = \frac{1}{\sqrt{L_{eq} C_{Diodes}}} \quad (2)$$

From Eq. (1) and (2), the equations can be held once the inductor, capacitor, and ESD protection diodes satisfy

$$\omega_o L_N - \frac{1}{C_N} = \frac{1}{C_{Diodes}} \quad (3)$$

Once the design parameters have been chosen, including the size of ESD protection diodes and operating frequency of RF circuit, the required inductor and capacitor for resonation can be calculated. Therefore, the RF input port will see a large impedance through the ESD protection circuit to ground, where the parasitic capacitance ($C_{Diodes}$) has been eliminated, and the parasitic resistance ($R_{Diodes}$) remains large.

To reduce the inductance used in $L_N$, another supplement capacitor ($C_S$) can be added to connect in parallel with ESD protection diode. In other words, the parasitic capacitance of ESD protection diodes ($C_{Diodes}$) is increased by adding the parallel capacitor ($C_S$). It is better to add the supplement capacitor rather then increase the diode size, because the supplement capacitor provides the purely capacitance, while increasing diode size lowers the parasitic resistance, which leads to the lower parasitic impedance and higher insertion loss.

Fig. 2(b) shows the circuit of another proposed ESD protection design. A pair of the ESD protection diodes ($D_P$ and $D_N$) is still used to provide ESD current paths, but the series inductor and capacitor ($L_P$ and $C_P$) are placed between RF input and $V_{DD}$. The operation of proposed design B is similar to that of proposed design A. The design parameters can be calculated by using

$$\omega_o L_P - \frac{1}{C_P} = \frac{1}{C_{Diodes}} \quad (4)$$

The proposed designs are simulated by using the ideal devices. A 0.11-nH inductor and a 300-fF capacitor are used for the series inductor and capacitor. The ESD protection diodes are simplified to be an 80-fF capacitor. Since the ideal devices are used, the proposed designs A and B have the same simulation results. The simulated $S_{21}$ parameter of the proposed design is shown in Fig. 3. The $S_{21}$ value at 60 GHz can be designed to be 0 dB, which means that insertion loss from ESD protection circuit is also 0 dB.

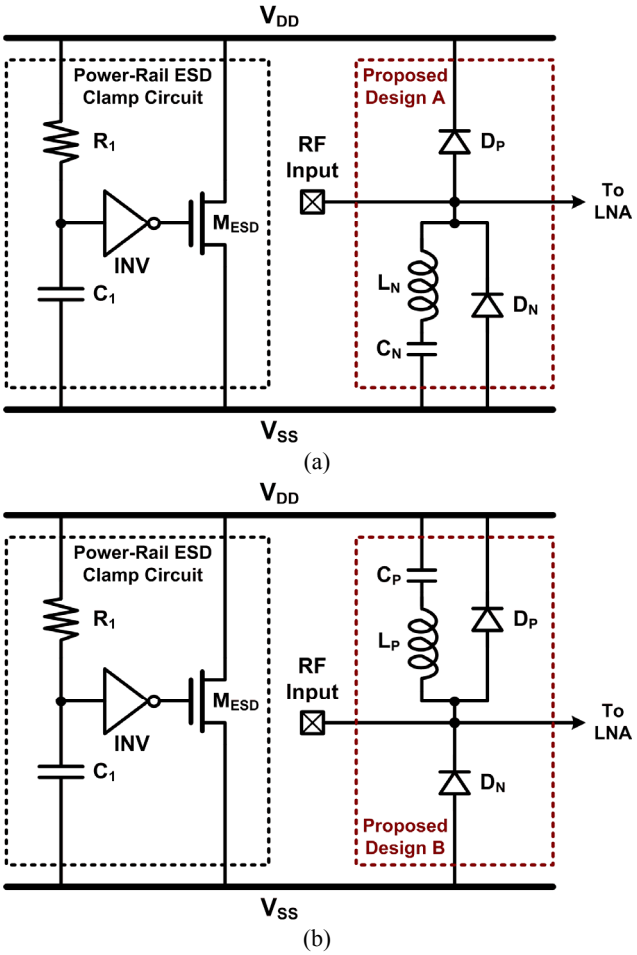


Fig. 2. (a) Proposed ESD protection design A and (b) proposed ESD protection design B.

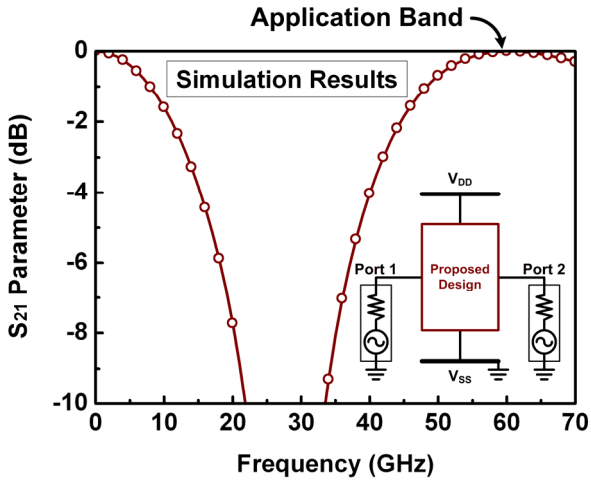


Fig. 3. Simulated $S_{21}$ parameter of proposed design.

## III. Measurement Results

The test circuits of the proposed ESD protection designs have been fabricated in a 65-nm CMOS process. Both proposed designs are split to 4 test circuits with different sizes of ESD protection diodes. The device dimensions of the test circuits are listed in Table I. The width of $D_P$ or $D_N$ in test circuits A1 (B1), A2 (B2), A3 (B3), and A4 (B4) are split as 8 μm, 15 μm, 23 μm, and 30 μm, respectively, while the length of $D_P$ or $D_N$ are kept at 0.6 μm. In this configuration, the $C_{Diodes}$ of test circuits A1 (B1), A2 (B2), A3 (B3), and A4 (B4) are 21 fF, 40 fF, 61 fF, and 80 fF, respectively. Therefore, the supplement capacitors ($C_S$) with 60 fF, 40 fF, and 20 fF are added to the test circuits A1 (B1), A2 (B2), and A3 (B3), respectively, to keep the size of series inductor and capacitor.

With the on-wafer measurement, the RF characteristics of the test circuits have been extracted. The two-port S-parameters of the test circuits from 0 to 67 GHz were measured by using the vector network analyzer. During the S-parameter measurement, the port 1 and port 2 were biased at 0.5 V, which is $V_{DD}/2$ in the given 65-nm CMOS process. The dc bias of 1-V $V_{DD}$ was also supplied to the test circuits. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the de-embedding technique. The source and load resistances to the test circuits are kept at 50 Ω.

The measured $S_{21}$ parameters versus frequencies among the test circuits are shown in Figs. 4 and 5. As shown in Fig. 4, the proposed design A can reduce the insertion loss at designed frequency band. The insertion loss of the proposed design can not be ideally 0 dB, since the parasitic resistance of ESD protection diodes ($R_{Diodes}$), which can not be eliminated by inductance, also loses the RF signals. At 60-GHz, the test circuits A1, A2, A3, and A4 have about 1.3-dB, 1.4-dB, 1.6-dB, and 1.8-dB insertion loss, respectively, which are summarized in Table I. Besides, all test circuits exhibit good input matching ($S_{11}$ < -15 dB) at 60 GHz.

The proposed design B can also reduce the insertion loss at 60 GHz, as shown in Fig. 5. At 60-GHz, the test circuits B1, B2, B3, and B4 have about 1.4-dB, 1.6-dB, 2.0-dB, and 2.3-dB insertion loss, respectively. The slightly increased insertion loss in this design may be due to the more complex metal routing in layout when the series inductor and capacitor connected to $V_{DD}$.

The positive-to-$V_{SS}$ (PS-mode), positive-to-$V_{DD}$ (PD-mode), negative-to-$V_{SS}$ (NS-mode), and negative-to-$V_{DD}$ (ND-mode) human-body-model (HBM) ESD robustness of all ESD test circuits are measured. The failure criterion is defined as the I-V characteristics seen at RF input shifting over 30% from its original curve after ESD stressed at every ESD test level. The HBM ESD robustness of all ESD test circuits can be obtained from the lowest level of PS-mode, PD-mode, NS-mode, and ND-mode ESD robustness, as listed in Table I. The test circuits A1, A2, A3, and A4 (B1, B2, B3, and B4) have 0.25-kV, 1.25-kV, 1.75-kV, and 2-kV (0.25-kV, 1-kV, 1.75-kV, and 2.25-kV) HBM ESD robustness, respectively.

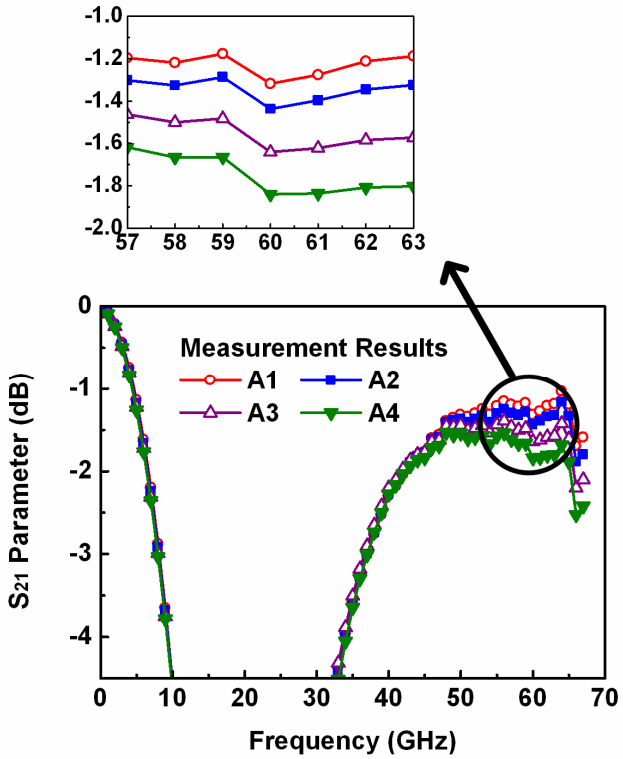


Fig. 4. Measured $S_{21}$ parameters of proposed design A.

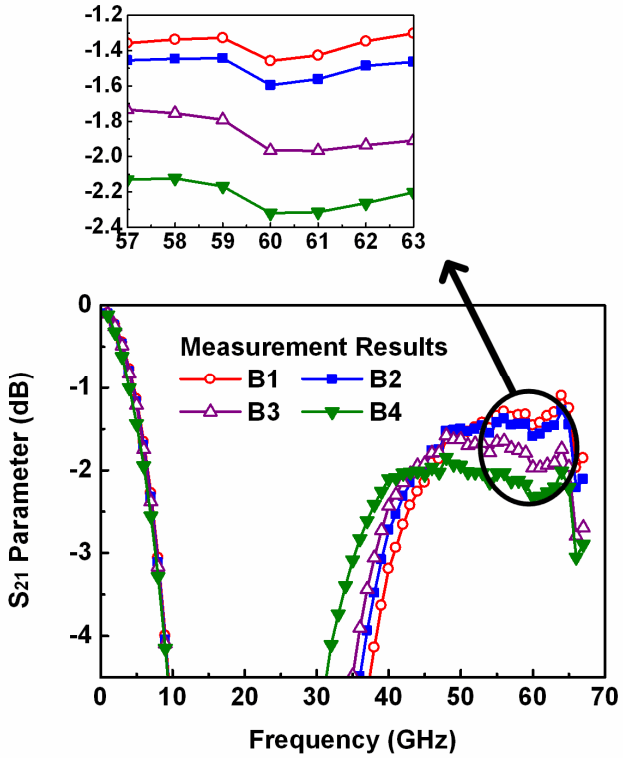


Fig. 5. Measured $S_{21}$ parameters of proposed design B.

TABLE I
DESIGN PARAMETERS AND MEASUREMENT RESULTS OF PROPOSED ESD PROTECTION CIRCUITS

| Test Circuit | Proposed Design A | | | | Proposed Design B | | | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A2 | A3 | A4 | B1 | B2 | B3 | B4 |
| $L_P$ | N/A | N/A | N/A | N/A | 0.11 nH | 0.11 nH | 0.11 nH | 0.11 nH |
| $C_P$ | N/A | N/A | N/A | N/A | 300 fF | 300 fF | 300 fF | 300 fF |
| $D_P$ | 8x0.6 μm$^2$ | 15x0.6 μm$^2$ | 23x0.6 μm$^2$ | 30x0.6 μm$^2$ | 8x0.6 μm$^2$ | 15x0.6 μm$^2$ | 23x0.6 μm$^2$ | 30x0.6 μm$^2$ |
| $L_N$ | 0.11 nH | 0.11 nH | 0.11 nH | 0.11 nH | N/A | N/A | N/A | N/A |
| $C_N$ | 300 fF | 300 fF | 300 fF | 300 fF | N/A | N/A | N/A | N/A |
| $D_N$ | 8x0.6 μm$^2$ | 15x0.6 μm$^2$ | 23x0.6 μm$^2$ | 30x0.6 μm$^2$ | 8x0.6 μm$^2$ | 15x0.6 μm$^2$ | 23x0.6 μm$^2$ | 30x0.6 μm$^2$ |
| $C_S$ | 60 fF | 40 fF | 20 fF | N/A | 60 fF | 40 fF | 20 fF | N/A |
| $S_{21}$ at 60 GHz | -1.3 dB | -1.4 dB | -1.6 dB | -1.8 dB | - 1.4 dB | - 1.6 dB | - 2.0 dB | - 2.3 dB |
| HBM ESD Level | 0.25 kV | 1.25 kV | 1.75 kV | 2 kV | 0.25 kV | 1 kV | 1.75 kV | 2.25 kV |

## IV. ESD PROTECTION CIRCUIT APPLIED TO LNA

The LNA circuit shown in Fig. 1 is simulated. Besides, by using the extracted RF characteristics in Section III, the LNA with the proposed ESD protection design is also simulated. The measured S-parameters of the test circuit A4 are inserted at the input port of the 60-GHz LNA.

Fig. 6 shows the simulated $S_{21}$-parameters of the 60-GHz LNA. The LNA without ESD protection circuit achieves 14.6-dB gain ($S_{21}$) at 60 GHz. With the ESD protection circuit A4 adding in the LNA, the simulated gain becomes 12.8 dB at 60 GHz. Besides, both the stand-alone LNA and the LNA with proposed ESD protection circuit achieve good input matching ($S_{11}$ < -15 dB) at operating frequency. Although the ESD protection circuit slightly degrades the RF gain of LNA, it can provide suitable ESD protection. The proposed ESD protection design in this work has been proved to achieve the required ESD robustness in a compact layout size with little RF performance degradation.

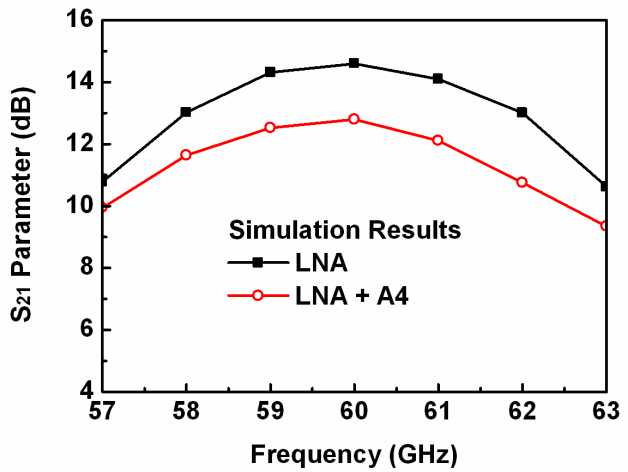


Fig. 6. Simulation results on $S_{21}$ parameters of 60-GHz LNA with and without ESD protection.

## V. CONCLUSION

The proposed compact and low-loss ESD protection designs for V-Band RF applications have been designed, fabricated, and characterized in a 65-nm CMOS process. These ESD protection circuits are developed to support RF circuit designers for them to easily apply ESD protection in the 60-GHz RF circuits. Such compact ESD protection circuits can achieve the 2-kV HBM ESD robustness with 1.8-dB loss and small layout area, which is the useful solution for on-chip ESD protection design for 60-GHz RF applications in 65-nm CMOS process. This ESD protection scheme can be further applied to higher frequency and smaller generation's technology.

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