New Design of Transient-Noise Detection Circuit with SCR Device for System-Level ESD Protection

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Abstract -- **A new SCR-based transient detection circuit for on-chip protection design against system-level ESD-induced electrical transient disturbance is proposed and verified in silicon chip. The experimental results in a 0.18-μm CMOS process have confirmed that the new proposed detection circuit can successfully memorize the occurrence of system-level ESD-induced electrical transient events. The detection output can be cooperated with firmware operation to automatically execute system recovery procedure, therefore the immunity of microelectronic systems against system-level ESD test can be effectively improved.**

I. INTRODUCTION

The reliability issue of CMOS ICs against system-level electrical transient disturbance becomes worse due to the strict requirements of reliability tests specified by IC industry, including the system-level electrostatic discharge (ESD) test of IEC 61000-4-2 standard [1] and the electrical fast transient (EFT) test of IEC 61000-4-4 standard [2]. In order to meet the system-level ESD specifications, there are two main methods [3], [4]. One effective method is to add some discrete noise-bypassing components or board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD or EFT tests. The immunity of microelectronic system (equipped with CMOS ICs) against electrical transient disturbance can be enhanced by choosing proper noise filter networks. The other method is to regularly check the system abnormal conditions by using an external hardware timer, such as watch dog timer. The additional hardware timer is often designed with registers or flip flops as a reference clock for system operation if the main program was locked or frozen after ESD test. However, during system-level ESD test, the logic states stored in the registers or flip flops of hardware timer would be also destroyed, still causing malfunction or upset condition in the system operation. Recently, some on-chip detection circuits were developed to detect ESD-induced transient disturbance for protection design in microelectronics systems [5], [6].

In this work, a new on-chip SCR-based transient detection circuit is proposed to detect the system-level electrical transient disturbance under the system-level ESD or EFT tests. A p-type substrate-triggered SCR (P_STSCR) device is used as the storage cell to memorize the occurrence of system-level ESD or EFT events. Using an SCR-based circuit to detect the electrical transient disturbance is first reported in the literature.

II. NEW ON-CHIP SCR-BASED TRANSIENT DETECTION CIRCUIT

The new on-chip SCR-based transient detection circuit is designed to detect the fast electrical transients during the system-level ESD or EFT tests.

A. Silicon Controlled Rectifier (SCR)

The silicon controlled rectifier (SCR) was often used as the on-chip ESD protection device due to its high ESD robustness within small layout area [7]. The anode of SCR is connected to the P+ and N+ diffusions in N-well (NW), whereas the cathode of SCR is connected to the N+ and P+ diffusions in P-well (PW). The original switching voltage of the SCR device is decided by the avalanche breakdown voltage of the N-well/P-well junction. It has been reported that the turn-on mechanism of SCR device is essentially a current triggering event [8]. While a current is applied to the base or substrate of SCR device, it can be quickly triggered into its latching state. The device cross-sectional view and the layout top view of the p-type substrate-triggered SCR (P_STSCR) used in this work are shown in Fig. 1(a) and Fig. 1(b), respectively.

An extra P+ diffusion is inserted into the P-well of the P_STSCR device structure and connected out as the p-trigger node of the P_STSCR device. The geometrical parameters such as D and W represent the distance between the anode and cathode, and the distance between the adjacent well contacts, respectively. The SCR in this work is not used as on-chip ESD protection device, but used as the memory unit to memorize the occurrence of electrical transient disturbance.

The setup to measure the dc current–voltage (I-V) curves of the fabricated P_STSCR device under substrate-triggered current (I_{bias}) is shown in Fig. 2(a). The measured dc I-V curves of the P_STSCR under different substrate-triggered currents are shown in Fig. 2(b).

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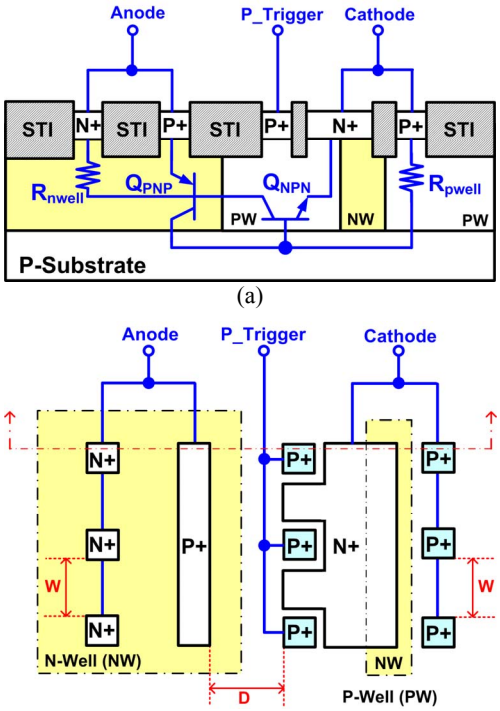


Fig. 1. (a) Device cross-sectional view and (b) layout top view, of the p-type substrate-triggered SCR (P_STSCR) with layout parameters of D=0.86μm and W=3.8μm realized in a 0.18-μm CMOS process.

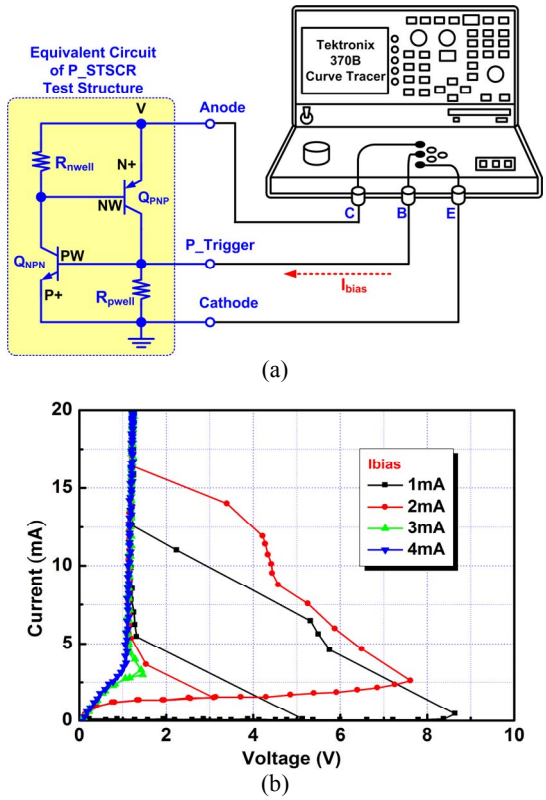


Fig. 2. (a) Measurement setup of P_STSCR device under different trigger currents. (b) The measured I-V characteristics of P_STSCR device under different trigger currents.

When the substrate-triggered current applied to the p-trigger node is increased from 1 mA to 4 mA, the switching voltage of P_STSCR is reduced from 8.6 V to 1.5 V. With the substrate-triggered current, the P_STSCR structure can be triggered into the latching state without involving the avalanche junction breakdown.

B. SCR-Based Transient Detection Circuit

The new proposed on-chip SCR-based transient detection circuit of this work is shown in Fig. 3. The P_STSCR device shown in Fig. 1 is used as the memory unit to memorize of the occurrence of system-level electrical transient disturbance. The anode of P_STSCR is connected to the drain of PMOS (M_{pr}) device. The gate of PMOS (M_{pr}) is connected to V_{SS} by the initial reset signal (V_{RESET}) to set the initial output voltage (V_{OUT2}) at 3.3 V.

The RC-delay circuit and the inverter are designed to provide the SCR triggering current. Under the system-level ESD events, the transient voltage has a fast rise time in the order of nanosecond (ns). The voltage level of V_X in the RC-delay circuit has much slower voltage response than the transient voltage coupling to V_{DD} because the RC-delay circuit is designed with a time constant in the order of microsecond (μs). Due to the longer delay of the voltage increase at the node V_X, the PMOS device (M_{p1}) can be turned on by the overshooting voltage at V_{DD} and conduct trigger current to the p-trigger node. The SCR device is therefore turned on to pull down the output voltage (V_{OUT1}) level to the SCR holding voltage of ~1.2 V. In the two-inverter buffer stage, the logic threshold voltage of inverter1 (INV_1) is designed at ~2.3 V and that of inverter2 (INV_2) is ~1.7 V. Therefore, after electrical transient disturbance, the V_{OUT2} of the proposed detection circuit will be changed from 3.3 V to 0 V to memorize the occurrence of system-level ESD-induced transient disturbance. The reset function (V_{RESET}) is used to release the turn-on state of SCR device by turning M_{pr} off, and then reset the output voltage (V_{OUT2}) back to 3.3 V again for detecting the next system-level transient event.

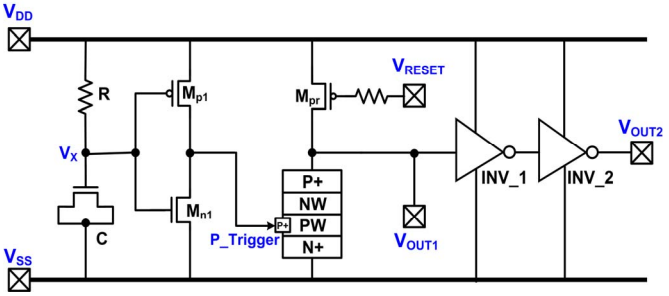


Fig. 3. The new proposed on-chip SCR-based transient detection circuit. The P_STSCR is used as memory cell to memorize the occurrence of electrical transient disturbance.

III. Experimental Results

The proposed detection circuit has been fabricated in a 0.18-μm CMOS process with 3.3-V devices. The fabricated

test chip with the silicon area of 542 µm x 240 µm is shown in Fig. 4.

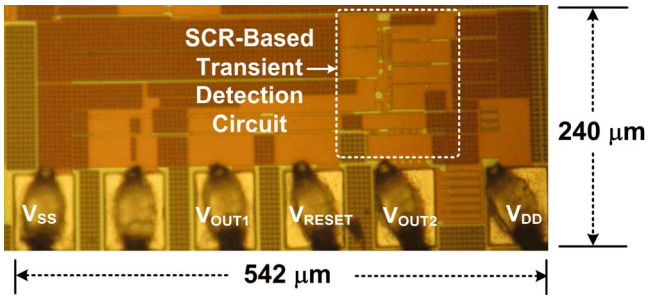


Fig. 4. Chip photo of the new proposed on-chip SCR-based transient detection circuit fabricated in a 0.18-µm CMOS process with 3.3-V devices.

A. System-Level ESD Test

In IEC 61000-4-2, two test modes have been specified, which are the air-discharge and contact-discharge test modes. The contact discharge is applied to the conductive surfaces of the EUT (direct application) or to the coupling planes (indirect application). Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to the horizontal or vertical coupling planes. Fig. 5 shows the measurement setup of the system-level ESD test standard with indirect contact-discharge test mode, where the horizontal coupling plane (HCP) are connected to the grounded reference plane (GRP) with two 470 kΩ resistors in series [1]. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from ESD gun will be coupled into all CMOS ICs inside the EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

With such a measurement setup, the circuit function of the proposed detection circuit during system-level ESD test can be evaluated. Monitoring in the oscilloscope, the transient responses on power lines of CMOS ICs can be recorded and analyzed. Before each system-level ESD test, the initial output voltages (V_{OUT1} and V_{OUT2}) of the proposed detection circuit are all reset to 3.3 V. After each system-level ESD test, the output voltages (V_{OUT1} and V_{OUT2}) are monitored to check their final voltage levels. Thus, the function of the proposed detection circuit can be evaluated by system-level ESD test.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of +0.35 kV zapping on the HCP are shown in Fig. 6(a). V_{DD} begins to increase rapidly from the normal voltage level of 3.3 V. Meanwhile, V_{OUT1} and V_{OUT2} begin to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD}, V_{OUT1}, and V_{OUT2} are influenced simultaneously. Finally, V_{OUT1} is pulled down to 1.2 V, which is corresponding to the holding voltage of the SCR device. Through buffer stages, V_{OUT2} of the proposed detection circuit transits from 3.3 V to 0 V.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of -0.2 kV zapping on the HCP are shown in Fig. 6(b). During the ESD-induced transient disturbance, V_{DD} begins to decrease rapidly from the original voltage level of 3.3 V. Finally, the output voltage (V_{OUT2}) of the proposed transient detection circuit is changed from 3.3 V to 0 V. So, the new proposed on-chip SCR-based transient detection circuit can successfully detect the electrical transients under system-level ESD tests with positive or negative ESD voltages.

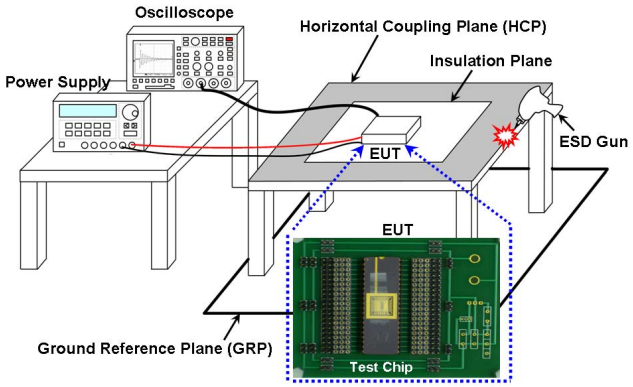
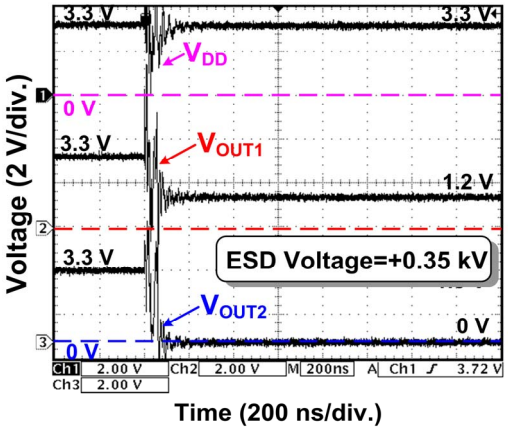
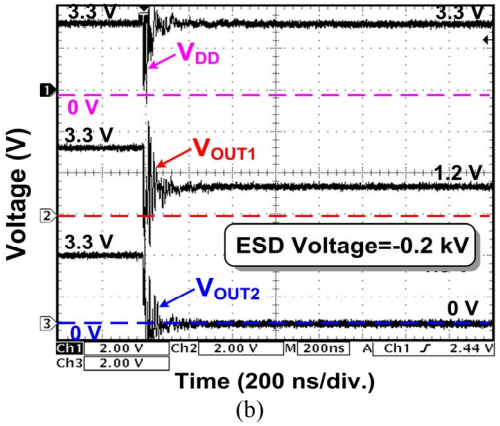


Fig. 5. Measurement setup for system-level ESD test with indirect contact-discharge test mode to evaluate the detection function of the on-chip SCR-based transient detection circuit.



(a)



(b)

Fig. 6. Measured V_{DD} and V_{OUT} transient voltage waveforms of the on-chip SCR-based transient detection circuit under system-level ESD tests with ESD voltage of (a) +0.35 kV and (b) -0.2 kV.

B. Application in Display Panels

In IEC 61000-4-2 standard, four classifications of system-level ESD test results have been defined, as listed in Table I. In order to solve the frozen states caused by system-level ESD test, microelectronic products can be manually reset by operator intervention, which only meets the criterion of "Class C" in the IEC 61000-4-2 standard. However, most microelectronic products are required to automatically recover the system functions without operator intervention to meet the "Class B" criterion by IC industry. By cooperating with the proposed SCR-based transient detection circuit, a hardware/firmware co-design solution can be provided to release the locked states caused by electrical transient disturbance without additional manual operations.

For display system with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power supplies are needed for electrical display functions, as shown in Fig. 7. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and the digital power line (VDDD) is used for shifter register and memory units. In the hardware/ firmware co-design method, the proposed detection circuit is connected to the 3.3-V VDDD power line to detect and memorize the occurrence of ESD-induced transient disturbance coupled on digital subsystems of display panels. The detection results can be temporarily stored as the system index for firmware check. In the beginning, the output state (V_{OUT2}) of the proposed detection circuit is set to logic "1" by the power-on reset circuit or start-up procedures. When the electrical transients happen, the proposed transient detection circuit can detect the occurrence of system-level electrical disturbance to pull down the output state (V_{OUT2}) from logic "1" to logic "0". At this moment, the firmware recovery index is therefore changed to logic "0" to initiate the automatic recovery operation to restore the display panels to a desired stable state as soon as possible.

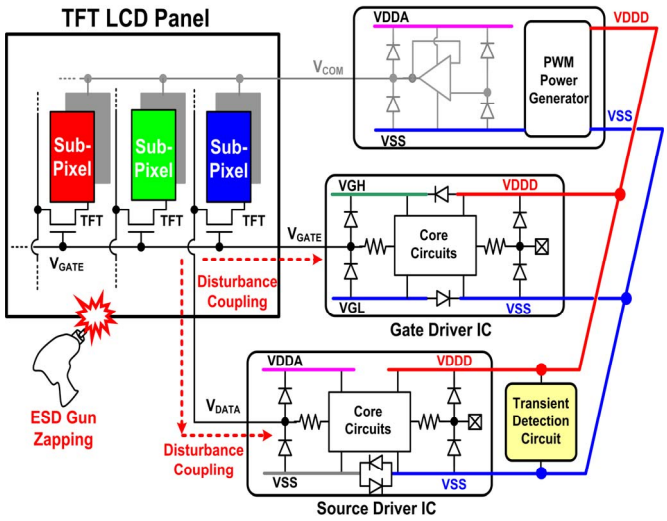


Fig. 7. Hardware/firmware co-design in a display system with TFT-LCD panel and the proposed transient detection circuit.

TABLE I

CLASSIFICATIONS OF SYSTEM-LEVEL ESD TEST

Criterion	Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. (Automatic Recovery)
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. (Manual Recovery)
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

IV. CONCLUSION

By using SCR device and RC-delay circuit, a new on-chip transient detection circuit has been developed to detect the fast electrical transients during system-level ESD test. Experimental results in silicon chip have verified that the proposed detection circuit can successfully memorize the occurrence of electrical transients during system-level ESD test. With hardware/firmware co-design method, the output state of the proposed on-chip SCR-based transient detection circuit can be used as the firmware index to provide an effective solution against the system malfunction caused by system-level ESD-induced electrical transient disturbance.

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