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Design of High-Voltage-Tolerant Stimulus Driver for Epileptic Seizure Suppression in a 0.18- μm CMOS Process

Chun-Yu Lin, Yi-Ju Li, Ya-Chun Huang, and Ming-Dou Ker
National Chiao-Tung University, Taiwan

It has been demonstrated that the abnormal discharge signal to cause epilepsy can be suppressed by electrical stimulation as the epileptic seizure happens. Due to the potential for mass production, CMOS technologies are more attractive to realize the implantable stimulator. However, the required voltage for stimulation is usually higher than the operation voltage of low-voltage CMOS process, so a stimulator with high-voltage tolerance in low-voltage CMOS process is needed.

A novel design of high-voltage-tolerant stimulus driver for epileptic seizure suppression with low power design and adaptive loading consideration is proposed in this work. The proposed design consists of the high-voltage-tolerant stimulus driver, V_{CC} controller, and high voltage generator. The proposed design can deliver the required stimulus current within a specific range of loading impedance. Besides, this design with 1.8-V and 3.3-V transistors can operate with high supply voltage (V_{CC}) of 5~10 V without electrical overstress issues. Without using the high-voltage transistors, the stimulator can be integrated into a chip in low-voltage CMOS process for an electronic epilepsy prosthetic system-on-chip (SoC).

The fabricated chip of the proposed stimulus driver has been further integrated into the closed-loop epileptic seizure monitoring and controlling system for animal tests. After stimulation, the intensive and rapidly brain activity in Long-Evans rat with epileptic seizure is suppressed. According to the animal test results, the functionalities of the proposed stimulus driver have been successfully verified.

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