New Design on 2×VDD-Tolerant Power-Rail ESD Clamp Circuit with Low Standby Leakage in 65nm CMOS Process

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***Abstract*-A 2×VDD-tolerant power-rail electrostatic discharge (ESD) clamp circuit with only thin gate oxide 1V devices and silicon-controlled rectifier (SCR) as main ESD clamp device has been proposed and verified in a 65nm CMOS process. The proposed power-rail ESD clamp circuit has an ultra-low standby leakage current by reducing the voltage drop across the gate oxide of the devices in the ESD detection circuit. From the measured results, the proposed design with SCR dimension of 50μm in width can achieve 6.5kV human-body-model (HBM), 300V machine-model (MM) ESD levels, and an ultra-low standby leakage current of 34.1nA at room temperature under the normal circuit operating condition with 1.8V bias.**

I. Introduction

With the continuously progressed CMOS technology, the number of transistors in a chip is aggressively increasing. Therefore, the system-on-a-chip (SoC) has become popular. For SoC integration, the input/output (I/O) circuits may receive or drive high-voltage signals to communicate with other integrated circuits (ICs) in a microelectronic system. However, the nanoscale device with thinner gate oxide and shallower diffusion junction depth arises several serious problems when it is implemented in the I/O circuits with mixed-voltage interfaces [1]. These problems include the gate oxide reliability [2], [3] and the undesirable leakage current paths [4], [5].

In 45nm CMOS technologies and beyond, the high-K materials have gradually replaced the silicon dioxide to reduce the equivalent oxide thickness (EOT) and the gate leakage current [6], [7]. However, the 90nm and 65nm CMOS technologies, which currently do not use the high-K materials as gate oxide layer, still suffer enormous gate leakage current issue. In order to solve the gate oxide reliability in the ESD protection circuit for the mixed-voltage I/O interfaces, the stacked-MOS configuration has been reported [8]. Other design strategies on high-voltage-tolerant power-rail ESD clamp circuit were also revealed to reduce the standby leakage current in nanometer CMOS technologies [9], [10].

In this work, a new low-leakage 2×VDD-tolerant power-rail ESD clamp circuit realized with only thin gate oxide devices for mixed-voltage I/O applications is proposed and verified in a 65nm CMOS technology. According to the experimental results, the standby leakage current of the proposed design can achieve the order of nano-ampere under the normal circuit operating condition.

II. New Proposed 2×VDD-Tolerant Power-Rail ESD Clamp Circuit with Low Standby Leakage

A. Gate Leakage Current in Nanoscale CMOS

When the gate oxide thickness continuously scales down in advanced CMOS technology, the gate leakage current has become an inevitable issue. Based on the BSIM4 model [11] with the device parameters provided from foundry, the gate currents of the nMOS capacitors in 65nm and 90nm CMOS technologies are compared in Fig. 1. The gate currents of the nMOS capacitors with W/L of 5μm/5μm and 10μm/10μm are 217nA and 878nA (1.61μA and 6.48μA) at 1V in 90nm (65nm) technology, respectively. The gate current of the nMOS capacitor is directly dependent on the poly-gate area and the gate oxide thickness. Therefore, the gate leakage issue in 65nm CMOS technology is much worse than that in 90nm CMOS technology due to thinner gate oxide.

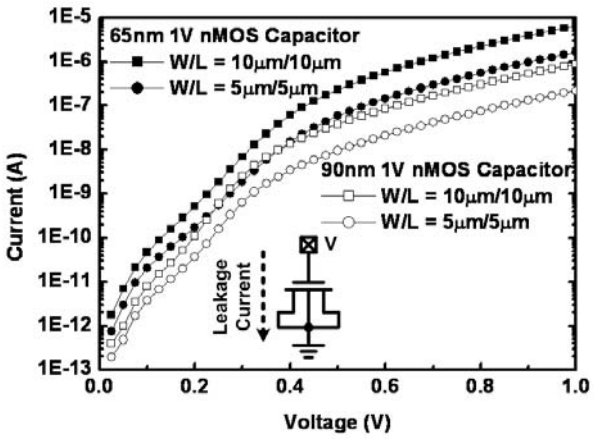

Fig. 1. Simulated gate currents of the nMOS capacitors in 65nm and 90nm CMOS technologies.

B. Design Concept of New Proposed 2×VDD-Tolerant Power-Rail ESD Clamp Circuit

The proposed 2×VDD-tolerant power-rail ESD clamp circuit with the substrate-triggered SCR device [12] as the main ESD clamp device is shown in Fig. 2. The cross-sectional view of the substrate-triggered SCR device is also illustrated in Fig. 3. The SCR device without the poly-gate structure has very small leakage current. The ESD detection circuit is necessary to improve the turn-on speed of the SCR device under ESD stress condition. Therefore, the proposed ESD detection circuit with only thin gate oxide 1V devices for

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2×VDD-tolerant applications has to be designed with considerations of gate oxide reliability. The main design concept is to reduce the voltage drop across the gate oxide of the devices in the ESD detection circuit. By following this main design concept, the gate leakage currents of the nMOS and pMOS in the ESD detection circuit can be well controlled to minimize the total standby leakage current.

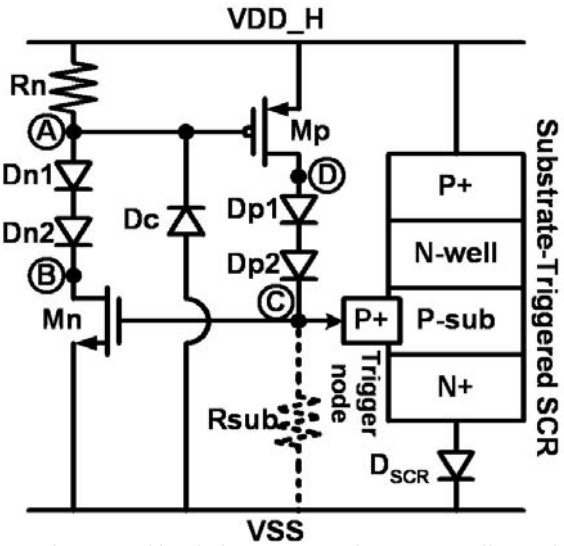

Fig. 2. The proposed low-leakage 2×VDD-tolerant power-rail ESD clamp circuit with the substrate-triggered SCR as the ESD clamp device.

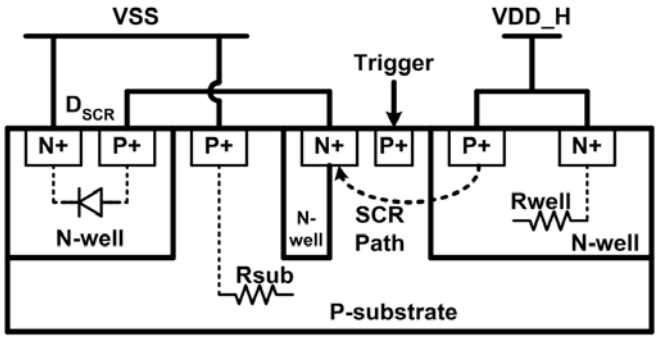

Fig. 3. Cross-sectional view of the ESD clamp device composed of the substrate-triggered SCR device with the cascode diode D_{SCR}.

In Fig. 2, the Mp is used to generate the substrate-triggered current into the trigger node (node C in Fig. 2) of the SCR device during the ESD stress event. Under the normal circuit operating condition, the Mp is kept off and the trigger node is kept at VSS through the parasitic p-substrate resistor Rsub. Therefore, the SCR device is turned off during the normal circuit operating condition. The *RC*-based ESD-transient detection mechanism is realized by the Rn and the reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. Compared to the thin gate oxide of MOS in the traditional *RC* circuit, the reverse-biased diode Dc in the ESD detection circuit has no gate leakage current issue. The cascode diode D_{SCR} is used to increase the holding voltage of the ESD clamp device to avoid the transient-induced latchup issue. The other diodes, Dn1, Dn2, Dp1, and Dp2, are used to reduce the voltage drop across the gate oxide of the Mn and Mp in the ESD detection circuit.

C. Operation under the Normal Circuit Operating Condition

During the normal circuit operating condition with VDD_H of 1.8V and grounded VSS, the gate voltage of Mp is biased at 1.8V through the resistor Rn. The gate voltage of Mn is biased at 0V through the p-substrate resistor Rsub of the SCR device. Because Mp is turned off, no trigger current is generated into the trigger node of the SCR device. By inserting the diode strings into the ESD detection circuit, the drain-to-gate and drain-to-source voltages of Mp and Mn can be less than 1V to effectively reduce the standby leakage current. Therefore, all 1V devices in the proposed ESD detection circuit are free from the gate oxide reliability issue under the normal circuit operating condition.

According to the device dimensions listed in Table I, the simulated voltage waveforms of the proposed ESD detection circuit during the normal power-on transition are shown in Fig. 4. VDD_H is powered on from 0V to 1.8V with a rise time of 1ms. In Fig. 4, the gate-to-drain and drain-to-source voltages of all devices do not exceed the 1×VDD 1V range. Therefore, the proposed ESD detection circuit would not suffer the gate oxide reliability issue under the normal circuit operating condition.

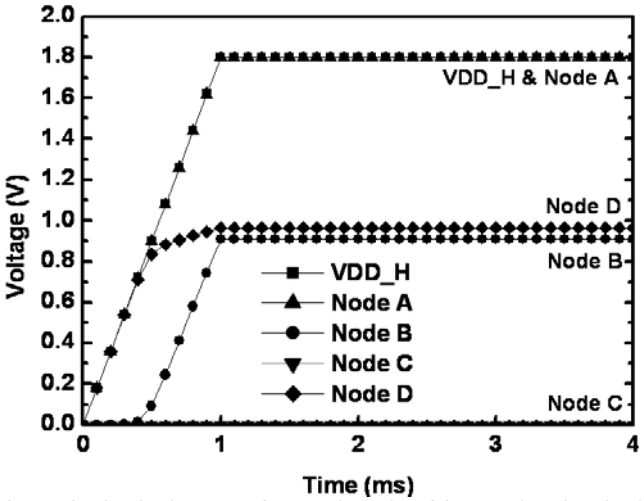

Fig. 4. Simulated voltage waveforms at the nodes of the ESD detection circuit under the normal power-on condition with VDD_H of 1.8V and a rise time of 1ms.

Table I Design Parameters of the Proposed Power-Rail ESD Clamp Circuit

Design Parameters			
Rn (Ω)	25k		
Mp (W/L)	40μm / 0.12μm		
Mn (W/L)	8μm / 0.12μm		
Dp1 & Dp2 (μm^2)	24.40		
Dn1 & Dn2 (μm^2)	1.14		
Dc (μm^2)	156.75		
Widths of D_{SCR} (μm)	30	40	50
Widths of SCR (μm)	30	40	50

D. Operation under the ESD Transient Event

When a positive ESD-like transient voltage is applied to VDD_H with grounded VSS, the *RC* time delay keeps the node A at a relatively low voltage level as compared with that at VDD_H. Mp can be quickly turned on to generate the

trigger current into the trigger node (node C in Fig. 2) of the SCR device.

In order to simulate the transient edge of the HBM ESD event before the breakdown on the ESD protection devices, a 5V voltage pulse with a rise time of 10ns is applied to VDD_H. The simulated transient voltage and the trigger current of the ESD detection circuit during the ESD transition are illustrated in Fig. 5. In the figure, Mp can be successfully turned on to generate the trigger current into the SCR device. Finally, the SCR device can be turned on to discharge the ESD current from VDD_H to VSS.

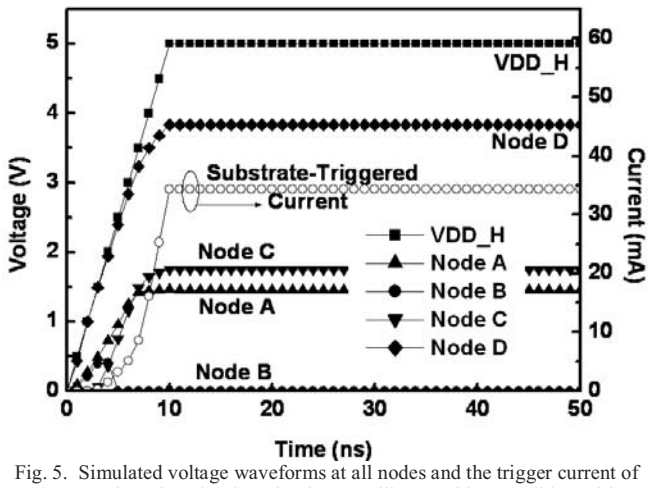

Fig. 5. Simulated voltage waveforms at all nodes and the trigger current of the ESD detection circuit under the ESD-like transition condition with VDD_H of 5V and a rise time of 10ns.

III. Experimental Results

The new proposed 2×VDD-tolerant power-rail ESD clamp circuits have been fabricated in a 65nm fully silicided CMOS process by using only 1V devices. In order to avoid the ESD failure location occurring at D_{SCR}, the junction width of D_{SCR} and the width of SCR are the same. The microphotograph of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit with the SCR device of 40μm in width is shown in Fig. 6.

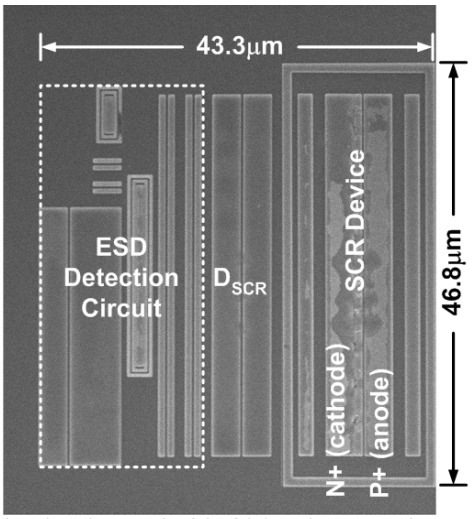

Fig. 6. The microphotograph of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit with the SCR device of 40μm in width.

A. DC I-V Measurement

The DC I-V characteristic of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit is shown in Fig. 7. At 1.8V normal operating voltage, the leakage currents of the proposed 2×VDD-tolerant power-rail ESD clamp circuits are 32.7, 33.1, and 34.1nA for the SCR widths of 30, 40, and 50μm, respectively, at the room temperature. In Fig. 7, the SCR device obviously contributes very small part to the total leakage current. In addition, the leakage current of the ESD detection circuit is reduced to the order of nano-ampere because the voltage drop across the gate oxide has been reduced by inserting the diode strings.

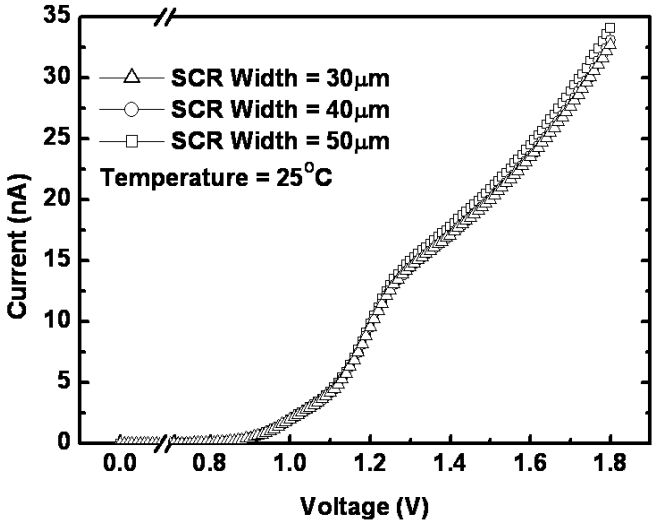

Fig. 7. The measured DC I-V curves of the 2×VDD-tolerant power-rail ESD clamp circuit with different SCR widths.

B. TLP Measurement and ESD Robustness

The transmission line pulsing (TLP) generator [13] with a pulse width of 100ns and a rise time of ~2ns is used to measure the second breakdown current (It2) of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit. The measured results are shown in Fig. 8. The power-rail ESD clamp circuit with the SCR device of 50μm in width achieves the It2 value of 3.29A. In Fig. 8, the measured curves rise up after 2.1V, which is higher than the normal operating voltage VDD_H of 1.8V. Therefore, the proposed 2×VDD-tolerant power-rail ESD clamp circuit has no latchup issue.

The It2, HBM, and MM ESD levels of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit are listed in Table II. The proposed design with the SCR device of 50μm in width can achieve 6.5kV HBM and 300V MM ESD levels.

Table II ESD Robustness of the Fabricated Proposed Power-Rail ESD Clamp Circuit with Different SCR Widths

2×VDD-Tolerant Power-Rail ESD Clamp Circuit	SCR Width (μm)		
	30	40	50
It2 (A)	2.05	2.68	3.29
HBM ESD Level (kV)	3.5	5.0	6.5
MM ESD Level (V)	150	250	300

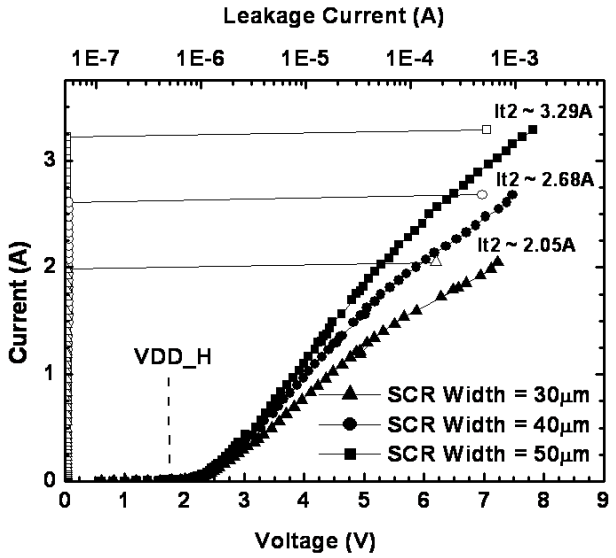

Fig. 8. TLP-measured curves of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit with different SCR widths.

C. Turn-On Verification

In order to observe the turn-on efficiency of the proposed power-rail ESD clamp circuit, an ESD-like voltage pulse with a rise time of 10ns and a pulse height of 5V is applied to the VDD_H with the grounded VSS to simulate the rising edge of the HBM ESD pulse. The ESD detection circuit would be started to trigger on the SCR device. The triggered-on SCR device can provide a low impedance path from VDD_H to VSS. The measured voltage waveforms on VDD_H power line under ESD-like stress condition are shown in Fig. 9. In Fig. 9, the applied 5V voltage pulse is quickly clamped down to a low voltage level of ~2.4V. The turn-on time is ~5ns, which is estimated from the maximum voltage peak to the clamped low voltage level in Fig. 9. According to the measured voltage waveforms, the fabricated 2×VDD-tolerant power-rail ESD clamp circuit has been successfully verified with high turn-on efficiency during the ESD stress event.

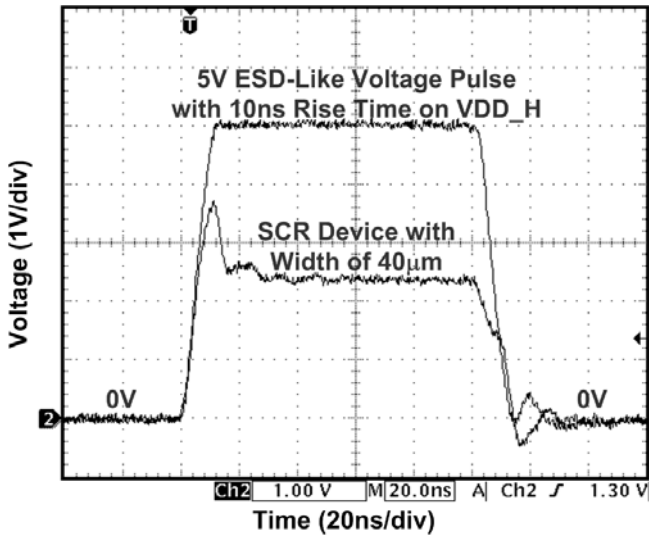

Fig. 9. Measured voltage waveforms of the 2×VDD-tolerant ESD clamp circuit under ESD-like condition with 5V voltage pulse and 10ns rise time.

IV. Conclusion

New design of 2×VDD-tolerant power-rail ESD clamp circuit with low standby leakage current has been proposed and successfully verified in a 65nm fully-silicided CMOS technology. The new proposed ESD detection circuit is realized with only 1V devices without suffering the gate oxide reliability issue under 1.8V (2×VDD) applications. According to the measured results, the proposed 2×VDD-tolerant power-rail ESD clamp circuit with the consideration of gate leakage current demonstrates a very small standby leakage current of only 34.1nA for the SCR device with a width of 50μm under 1.8V bias at 25°C. Moreover, the proposed power-rail ESD clamp circuit also performs excellent turn-on efficiency. The new proposed 2×VDD-tolerant power-rail ESD clamp circuit with low standby leakage current is considerably suitable for on-chip ESD protection in the mixed-voltage I/O interfaces.

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