On-Chip ESD Protection Designs in RF Integrated Circuits for Radio and Wireless Applications

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***Abstract* — CMOS technology has been used to implement the radio and wireless integrated circuits. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness. Therefore, on-chip ESD protection designs must be added at all input/output pads in CMOS chip. To minimize the impacts from ESD protection design on circuit performances, ESD protection at input/output pads must be carefully designed. A review on ESD protection designs with low parasitic capacitance for radio and wireless applications is presented in this paper. The comparisons among these ESD protection designs are also discussed.**

***Index Terms* — Electrostatic discharge (ESD), low capacitance, radio-frequency (RF).**

I. Introduction

All wireless communication products must meet the reliability specifications during mass production. Electrostatic discharge (ESD), which was one of the most important reliability issues during mass production, must be taken into consideration [1]. All integrated circuits used in the wireless communication products need to be equipped with ESD protection designs. However, ESD protections cause radio-frequency (RF) performance degradation with several undesired effects. Parasitic capacitance is one of the most important design considerations for RF ICs. A typical specification for an RF circuit on human-body-model (HBM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV and 200 fF, respectively [2], [3]. As the operating frequencies of RF circuits increase, the parasitic capacitance was more strictly limited.

In this paper, several ESD protection designs on ICs with very low parasitic capacitance for wireless communication applications are reviewed and compared.

II. ESD Protection Designs With Low Parasitic Capacitance

A. ESD Protection Diodes

Fig. 1 shows the ESD protection scheme with diodes (D_{ESD}) at I/O pad and the power-rail ESD clamp circuit between V_{DD} and V_{SS} [4]. Under positive-to-V_{DD} (PD) or negative-to-V_{SS} (NS) ESD stresses, ESD current is discharged through the forward-biased D_{ESD}. During positive-to-V_{SS} (PS) ESD stress, ESD current is discharged from the I/O pad through the forward-biased D_{ESD} to V_{DD}, and discharged to the grounded V_{SS} through the power-rail ESD clamp circuit. Similarly, during negative-to-V_{DD} (ND) ESD stress, ESD current is discharged from the V_{DD} through the power-rail ESD clamp circuit and the forward-biased D_{ESD} to the I/O pad. However, the parasitic capacitance of the ESD protection diodes is directly contributed at the I/O pad, which may be too large to be tolerated for RF circuits.

B. Stacked ESD Protection Diodes

The ESD protection diodes in stacked configuration had been presented, as shown in Fig. 2 [5]. With two stacked ESD protection diodes, the overall parasitic capacitance theoretically becomes half. More stacked ESD diodes leads to more significant parasitic capacitance reduction. However, this technique is adverse to ESD protection because the turn-on resistance and the clamping voltage of the stacked ESD protection diodes during ESD stresses are increased as well.

C. Parallel LC Resonator

The parallel LC resonator can be realized as shown in Fig. 3 [6]. The inductor (L_{ESD}) can resonate with the parasitic capacitance of D_{ESD}. The inductor also serves as an ESD protection device between I/O pad and V_{DD}. The placement of the inductor and the ESD protection diode can be interchanged to provide the same function. Since the inductor is dc short, a dc blocking capacitor (C_{block}) is required to provide a separated dc bias for the internal circuits.

D. ESD Protection Inductor

ESD protection design for RF circuits by using inductor as the ESD protection device had been reported, as shown in Fig. 4 [7]. Since the frequency component of ESD current is much lower than that of the RF signal, the inductor can pass the ESD current while block the RF signal. To efficiently sink the ESD current, the metal width of the L_{ESD} should be wide enough to enhance the current handling capability. Besides, a dc blocking capacitor (C_{block}) is needed to provide a separated dc bias for the internal circuits.

E. Series LC Resonator

ESD protection design utilizing the series LC resonator is shown in Fig. 5 [8]. At high frequencies, the L_{ESD} dominates the impedance of the series resonator. Thus, wideband ESD protection can be achieved by designing the application band of the series LC resonator to cover the frequency band of the RF signal. During ESD stresses, the ESD current can be discharged through the L_{ESD} and D_{ESD}. However, the transient

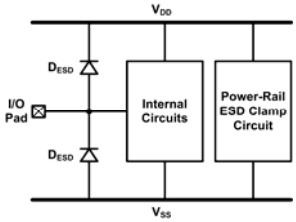

Fig. 1. ESD protection design by diodes.

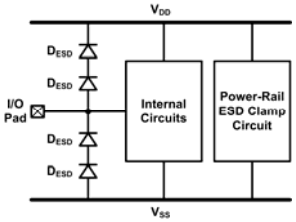

Fig. 2. ESD protection design by stacked diodes.

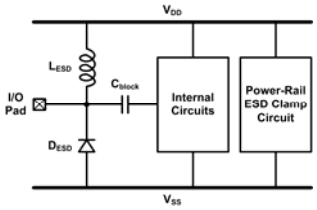

Fig. 3. ESD protection design by parallel LC resonator.

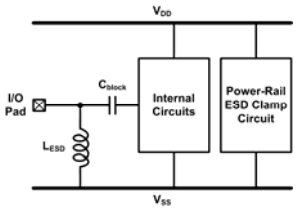

Fig. 4. ESD protection design by inductor.

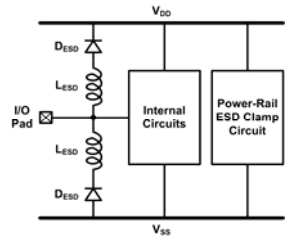

Fig. 5. ESD protection design by series LC resonator.

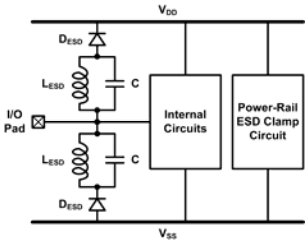

Fig. 6. ESD protection design by LC-tank.

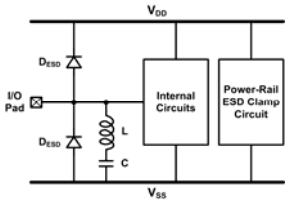

Fig. 7. ESD protection design by modified LC-tank.

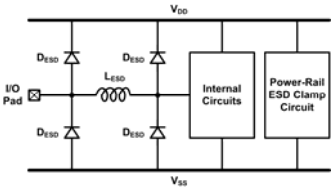

Fig. 8. Distributed ESD protection scheme.

voltage across the series L_{ESD} and D_{ESD} should be reduced to improve the ESD robustness.

F. LC-Tank

As shown in Fig. 6, a pair of the LC-tanks is placed at the I/O pad [9]. At the resonant frequency of the LC-tank, there is ideally infinite impedance from the signal path to the ESD protection diodes. Consequently, the parasitic capacitances of the ESD diodes are isolated, which can mitigate the parasitic effects from the ESD protection diodes. However, the transient voltage across the LC-tank ESD protection circuit should be reduced to improve the ESD robustness.

G. Modified LC-Tank

Fig. 7 shows the circuit design of modified LC-tank ESD protection [10]. The series LC is designed to resonate at low frequency. At the frequency above the resonant frequency, the inductance dominates the impedance of the series LC, and then the inductance can eliminate the parasitic capacitance of the ESD protection diodes.

H. Distributed ESD Protection Diodes

The distributed ESD protection scheme had been presented, as shown in Fig. 8 [11]. With the ESD protection diodes divided into small sections and matched by the inductor, such a distributed ESD protection scheme can achieve wideband impedance matching. The number of ESD protection diodes can be varied to optimize the performance.

III. Conclusion

A comprehensive review in the field of ESD protection design with low parasitic capacitance for RF integrated circuits is presented. The on-chip ESD protection designs for RF circuits will continuously be an important design task, as the operating frequencies of RF circuits increase.

Acknowledgement

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