SCR Device for On-Chip ESD Protection in RF Power Amplifier

Chun-Yu Lin and Ming-Dou Ker

Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

***Abstract* — To protect a radio-frequency (RF) power amplifier from electrostatic discharge (ESD) damages, a low-capacitance, high-robust, and good-latchup-immune ESD protection device was proposed in this work. The proposed design has been realized in a compact structure in a 65-nm CMOS process. Experimental results of the test devices have been successfully verified, including RF performances, I-V characteristics, and ESD robustness.**

***Index Terms* — Electrostatic discharge (ESD), power amplifier (PA), radio-frequency (RF), silicon-controlled rectifier (SCR).**

I. Introduction

In wireless communication systems, a power amplifier (PA) is usually provided at a transmission side for amplifying signals to be transmitted. The power amplifier realized in CMOS technology is susceptible to an electrostatic discharge (ESD) event which may damage the IC products. Diode or silicon-controlled rectifier (SCR) devices have been generally used for giga-Hz radio-frequency (RF) circuits, since it can meet the typical specification on human-body-model (HBM) and machine-model (MM) ESD robustness and the maximum parasitic capacitance [1]-[3]. However, the signal swing at output pads of some PAs may be as high as two to three times the supply voltage (V_{DD}). The conventional diode or SCR ESD protection devices limit the maximum signal swing at RF output [4]. Therefore, a novel ESD protection device with low parasitic capacitance, high ESD robustness, and good latchup immunity for the RF PA is needed.

II. Proposed Design

The new proposed ESD protection device utilizes an SCR as main ESD-current-discharging paths. The cross-sectional view of the proposed design is shown in Fig. 1. The equivalent circuit of the SCR consists of a cross-coupled PNP BJT (Q_{PNP}) and NPN BJT (Q_{NPN}), as shown in Figs. 1 and 2(a). The positive-feedback regenerative mechanism of PNP and NPN BJTs results in the SCR device becoming highly conductive to make the SCR very robust against ESD stresses. To control the turn-on voltage of SCR, a trigger diode (D_T) is embedded in the SCR. The D_T is realized by N+/P-ESD junction, where the P-ESD denotes the p-type ESD implantation [5]. Once ESD stresses from anode to cathode of the SCR, the D_T will breakdown first, and then the breakdown current through the R_N and R_P makes the SCR turn on. Besides, as ESD stresses from cathode to anode of the SCR, the ESD currents can be discharged through the parasitic P-well/N-well diode in SCR.

Under normal RF circuit operating conditions, the D_T is kept off. The SCR is also kept off to prevent from the signal loss.

III. Realization

The test devices with different R_N and R_P are implemented in this work. The lengths of L_A and L_C are split as 0.3 μm, 1 μm, and 2 μm. The anode-to-cathode lengths (L_{AC}) are kept at 1.5 μm, and the OD regions (L_{OD}) are kept at 0.8 μm. All device widths are 40 μm. The dimensions of test devices are summarized in Table I. The test devices have been fabricated in a 65-nm CMOS process. Fig. 2(b) shows the chip photograph of one test device. The test devices are implemented with G-S-G pads to facilitate on-wafer two-port RF measurement.

IV. Experimental Results

The parasitic capacitances are extracted from the two-port S-parameters. The parasitic effects of the G-S-G pads have been removed by using the de-embedding technique. The intrinsic parasitic capacitances (C_{ESD}) of the test devices between 0 and 10 GHz are shown in Fig. 3. The maximum parasitic capacitances of the test circuits are about 90 fF.

The dc I-V curves of the test devices are shown in Fig. 4. If the dc holding voltages (V_{hold}) of the test devices exceed V_{DD} (2.5 V, in this work), they will be free from latchup event.

The I-V characteristics of the test devices in high-current regions are investigated by a transmission-line-pulsing (TLP) system. The TLP I-V curves are shown in Fig. 5. The trigger voltages (V_{t1}) of the test devices are 7~8 V, which means they can sustain up to 7-V RF signal swing. The secondary breakdown current (I_{t2}) of the test devices are about 1.7 A.

The HBM and MM ESD robustness of the test devices are evaluated by the ESD tester. All these data are summarized in Table I.

V. Conclusion

The new ESD protection device has been designed, realized, fabricated, and characterized in a 65-nm CMOS process. The proposed ESD protection design can be used to achieve low parasitic capacitance, high ESD robustness, and good latchup immunity for the RF power amplifier.

ACKNOWLEDGEMENT

This work was supported by Taiwan Semiconductor Manufacturing Company, by National Science Council, Taiwan, under Contract NSC 101-2221-E-009-141, and by the "Aim for the Top University Plan" of National Chiao Tung University and Ministry of Education, Taiwan.

REFERENCES

[1] W. Soldner, M. Kim, M. Streibl, H. Gossner, T. Lee, and D. Schmitt-Landsiedel, "A 10GHz broadband amplifier with bootstrapped 2kV ESD protection," *ISSCC Dig. Tech. Papers*, pp. 550-551, Feb. 2007.

[2] D. Linten, S. Thijs, M. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1434-1442, Jul. 2005.

[3] M.-D. Ker, J.-J. Peng, and H.-C. Jiang, "ESD test methods on integrated circuits: an overview," in *Proc. IEEE Int. Conf. Electronics, Circuits and Systems*, 2001, pp. 1011-1014.

[4] M. Ruberto, O. Degani, S. Wail, A. Tendler, A. Fridman, and G. Goltman, "A reliability-aware RF power amplifier design for CMOS radio chip integration," in *Proc. IEEE Int. Reliability Physics Symp.*, 2008, pp. 536-540.

[5] M.-D. Ker, C.-H. Chuang, and W.-Y. Lo, "ESD implantations for on-chip ESD protection with layout consideration in 0.18-μm salicided CMOS technology," *IEEE Trans. Semiconductor Manufacturing*, vol. 18, no. 2, pp. 328-337, May 2005.

Table I. Device dimensions and measurement results of test devices.

		Test Devices		
		I	II	III
Design	Width (μm)	40	40	40
	L_{OD} (μm)	0.8	0.8	0.8
	L_A (μm)	0.3	1	0.3
	L_C (μm)	1	1	2
	L_{AC} (μm)	1.5	1.5	1.5
Measurement	Max. C_{ESD} (fF)	89.2	89.9	89.3
	DC V_{hold} (V)	2.89	2.48	2.55
	TLP V_{t1} (V)	7.75	7.80	7.21
	TLP I_{t2} (A)	1.64	1.74	1.73
	HBM Level (kV)	3	3.25	3.25
	MM Level (V)	200	200	200

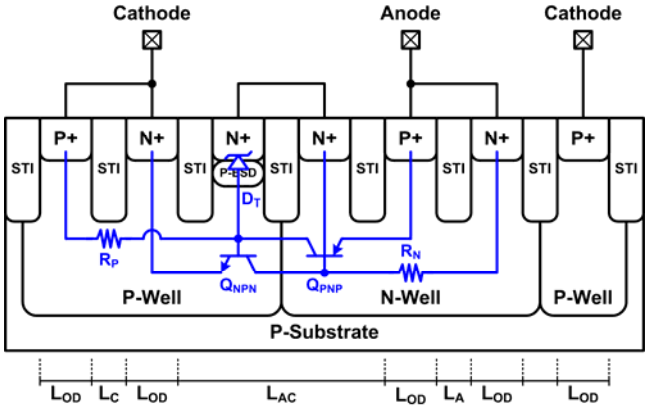

Fig. 1. Cross-sectional view of proposed SCR device.

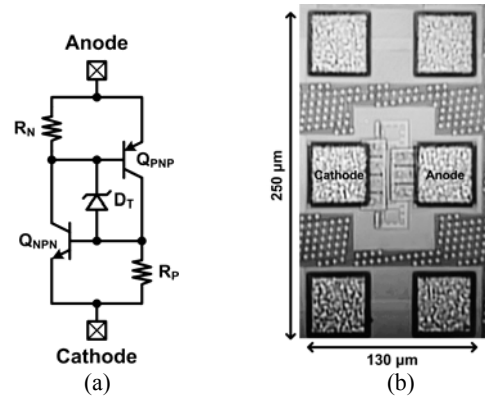

Fig. 2. (a) Equivalent circuit of proposed SCR device. (b) Chip photograph of one test device.

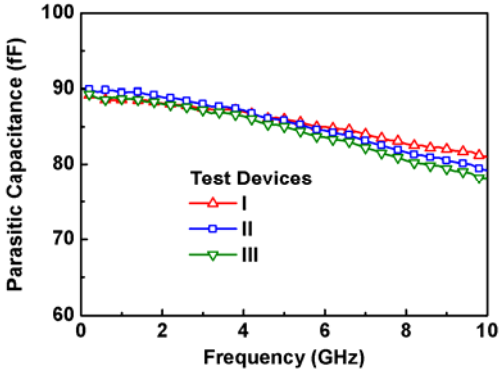

Fig. 3. Measured parasitic capacitances of test devices.

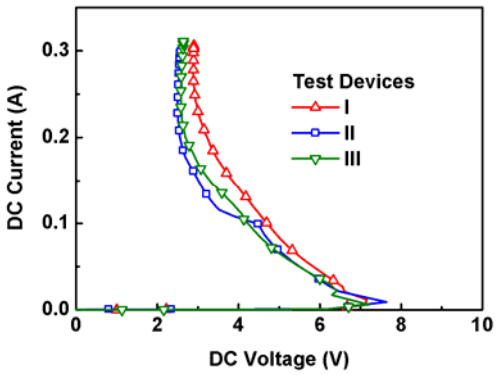

Fig. 4. DC I-V curves of test devices.

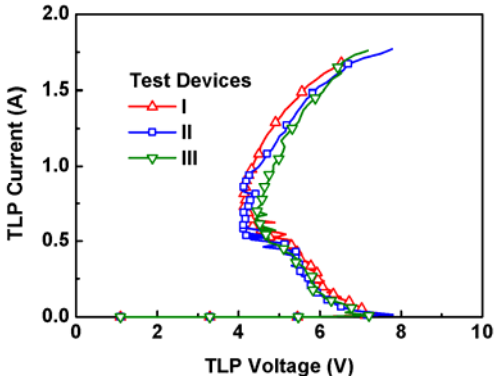

Fig. 5. TLP-measured I-V curves of test devices.