Investigation on Safe Operating Area and ESD Robustness in a 60-V BCD Process with Different Deep P-Well Test Structures

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***Abstract*—Safe operating area (SOA) is one of the noticeable reliability concerns for power MOSFETs during the normal circuit operating conditions. Besides, electrostatic discharge (ESD) reliability is another important reliability issue for the power IC products. To save the silicon area of power IC with high-voltage (HV) devices, it is preferable for HV MOSFET to be self-protected without any additional ESD protection device, and to behave wide SOA region. In this work, the impact of deep P-Well (DPW) structure to the electrical SOA (eSOA) and ESD robustness of HV MOSFET has been investigated in a 0.25-µm 60-V BCD process. DPW structure is used to implement the RESURF (reduced surface field) in MOSFET, which make it be able to sustain the high operating voltage. From the experimental results in silicon chip, the ESD robustness and eSOA of HV MOSFET can be improved by the modified DPW structure.**

I. Introduction

Nowadays, the smart power technology with HV MOSFET devices has been developed and used to fabricate the display driver circuits, power switch, motor control systems, and so on [1]. Among the various reliability specifications, safe operating area (SOA) is a noticeable reliability concern during normal circuit operating conditions for power IC with the HV MOSFET [2]. The SOA region of HV MOSFET must be well characterized for using in circuit design to meet the specification of applications, which defines the operating limitation without damaging the IC products. In a HV n-type MOSFET, there is a parasitic n-p-n BJT inherent in the device structure. Once the parasitic BJT was triggered on to initiate a snapback, the gate control over the HV n-type MOSFET would be lost, and the current crowding effect would damage the HV device violently [3]. Thus, the SOA boundary has been defined without triggering on the parasitic BJT. In Fig. 1, SOA region is depicted as the shadow region, and the dotted line represented the SOA boundary. To minimize the self-heating effect under SOA measurement, device under test (DUT) is usually stressed by the pulses with a short pulse width. A transmission line pulse (TLP) system that delivers square pulses with a 100-ns pulse width is usually applied for the measurement of electrical SOA (eSOA) [4], [5]. The eSOA boundary is acquired when thermal effect is not strongly involved during operation.

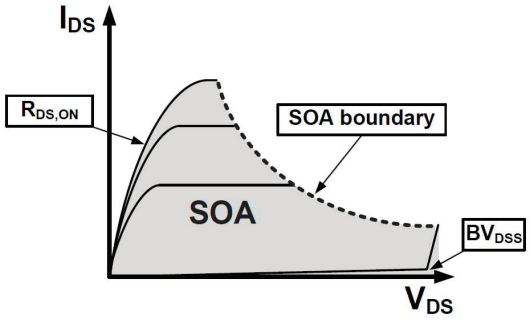
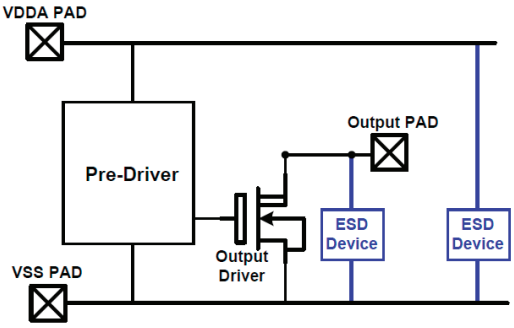
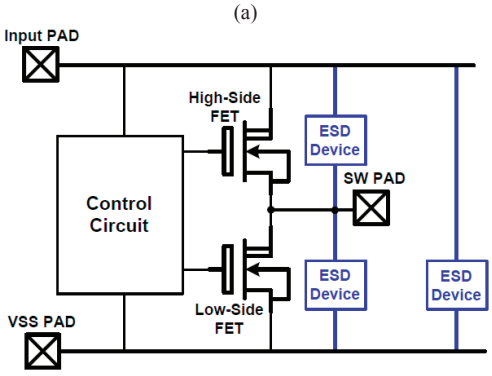


Fig. 1. A diagram showing on-resistance ($R_{DS,\ ON}$), SOA region, and breakdown voltage (BV_{DSS}) of a HV MOSFET.

Besides, on-chip electrostatic discharge (ESD) protection has been known as one of the important issues in high-voltage (HV) integrated circuits [6], [7]. ESD is an accidental event during fabrication, packaging, and testing processes of integrated circuits. In order to protect the internal circuits from ESD damage, on-chip ESD protection devices are applied to all input/output (I/O), power (V_{DD}/V_{SS}) and switch (SW) pads. For example, the circuit diagram of ESD protection scheme for LED driver and DC-DC buck converter are shown in Fig. 2(a) and 2(b).



(a)



(b)

Fig. 2. ESD protection for the applications of (a) output pad of LED driver and (b) switch (SW) pad of DC-DC buck converter.

To save the silicon area, it is preferable for HV MOSFETs to have high ESD robustness and wide SOA region simultaneously without any ESD protection device added into the HV integrated circuits. In this work, the HV MOSFET in a 0.25-µm 60-V BCD process is investigated with different Deep-P-Well (DPW) structures to improve both of ESD robustness and SOA region.

II. Test Device Structures in 60-V BCD Process

Fig. 3(a) and Fig. 4(a) show the device cross-sectional view and layout top view of the standard 60-V n-channel lateral diffused MOSFET (nLDMOS), respectively. The normal operating voltage of the HV MOSFET is V_{DS} = 0 ~ 60 V and V_{GS} = 0 ~ 5V. Such HV device is surrounded by N-buried layer (NBL), which is connected to drain. The deep P-well (DPW) is used for RESURF (reduced surface field) technique to increase the breakdown voltage (BV_{DSS}) without paying wider layout distance for low on-resistance ($R_{DS,ON}$)

consideration [8]. In this work, the DPW structure in nLDMOS was modified to investigate the impact of DPW structure to eSOA and ESD robustness. Three test devices investigated in the silicon chip include the standard HV device (nLDMOS_S), the modified HV device (nLDMOS_A), and the 2nd modified HV device (nLDMOS_B).

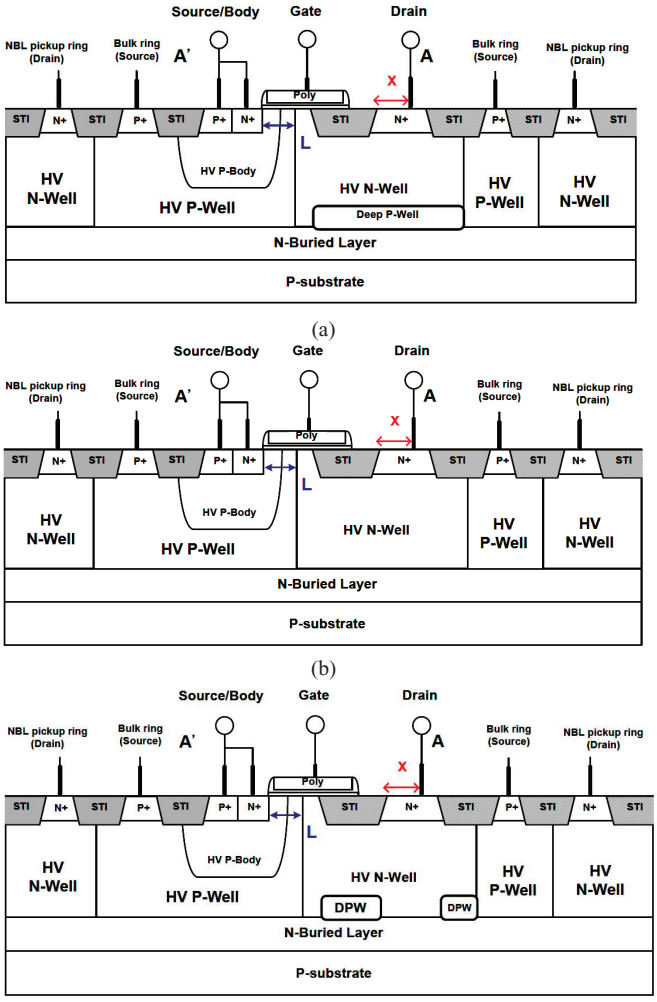


Fig. 3. The cross-sectional view of (a) the standard nLDMOS_S, (b) the modified nLDMOS_A, and (c) the 2nd modified nLDMOS_B, high-voltage devices in a 0.25-µm 60-V BCD process.

As shown in Fig. 3(b) and Fig. 4(b), the DPW structure under drain side is totally erased in the nLDMOS_A. Based on the prior study [9], the vertical BJT path can be induced where ESD current could flow into NBL region without DPW structure. The vertical ESD current path was spread almost along the entire region underneath the device, resulting in a significant reduction of the power density in the drain side, therefore to improve ESD robustness. The 2nd modified test device structure of nLDMOS_B is shown in Fig. 3(c) and Fig. 4(c), whose DPW structure is slotted under the drain N+ region. It is expected that such nLDMOS_B device can sustain high ESD robustness without lowering breakdown voltage. All the test devices are drawn with the same device dimension of W/L = 320 µm/1 µm in the silicon chip. With a large drain N+ region, it is expected that power density under ESD stress can be further reduced. Therefore, the range of drain N+ region, represented by the distance X marked in the figures, is split with 0.14, 5, and 10 µm, respectively (0.14 µm is the minimum distance in this HV process). Fig. 5 shows the test chip of total test devices fabricated in a 0.25-µm 60-V BCD process.

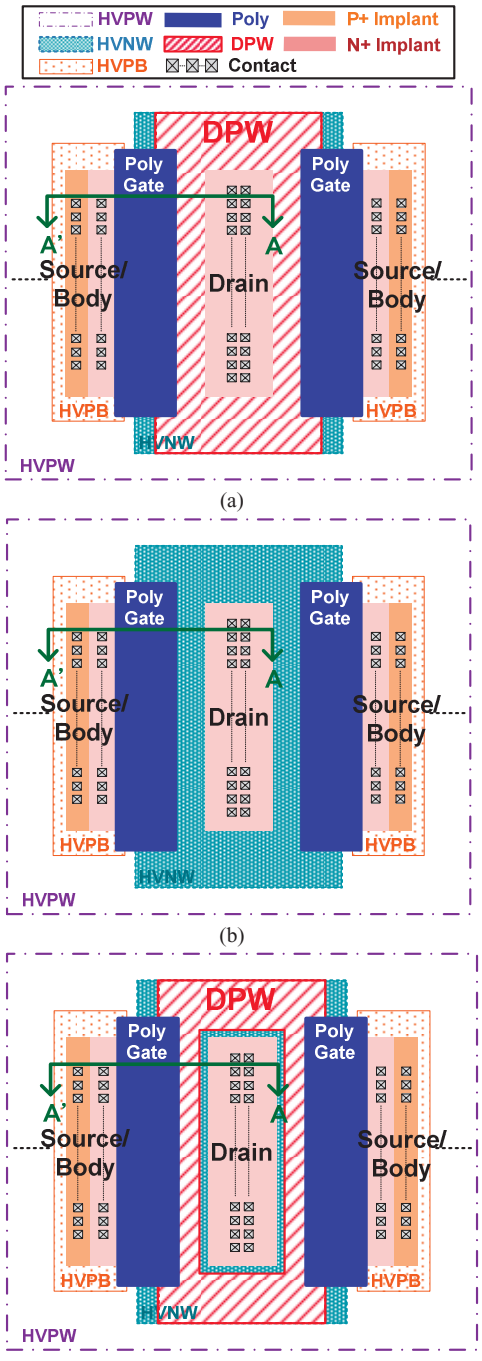


Fig. 4. The corresponding layout top view of (a) the standard nLDMOS_S, (b) the modified nLDMOS_A, and (c) the 2nd modified nLDMOS_B, HV devices in a 0.25-µm 60-V BCD process.

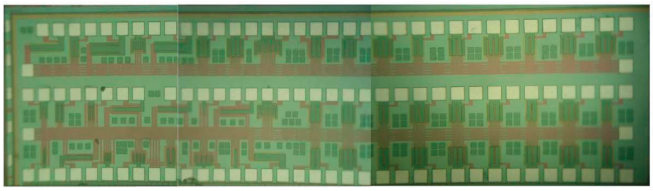


Fig. 5. The test chip of total test devices fabricated in a 0.25-µm 60-V BCD process.

III. Experimental Results

A. Measurement Results of Electrical SOA

To investigate the impact of DPW structure to device ruggedness under normal circuit operating conditions, the

characterization of eSOA is measured by 100-ns TLP pulses when giving a DC voltage for gate bias. The measurement setup was shown in Fig. 6. The gate bias is varied from 0 V to 5 V. TLP-measured I-V characteristics under different gate biases and the eSOA boundary of nLDMOS_S with distance X of 0.14μm are shown in Fig. 7, which is acquired by connecting the last *I–V* points under different DC gate biases before snapback.

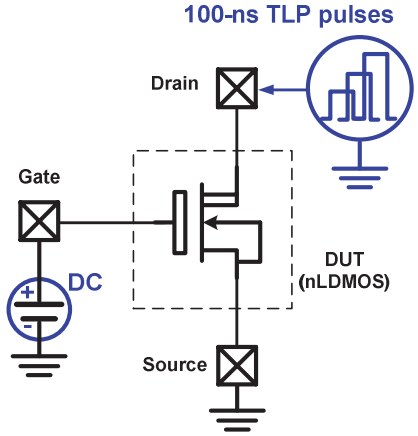


Fig. 6. Test setup for eSOA measurement by 100-ns TLP pulses.

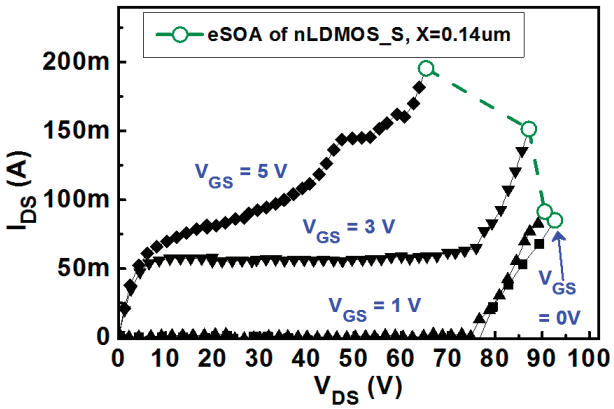
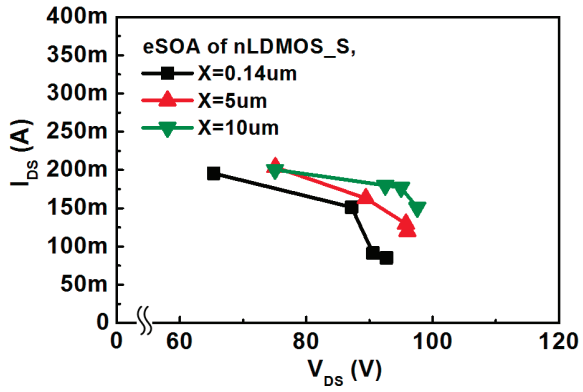


Fig. 7. The measured eSOA boundary of nLDMOS_S with distance X of 0.14 μm by 100-ns TLP pulses.

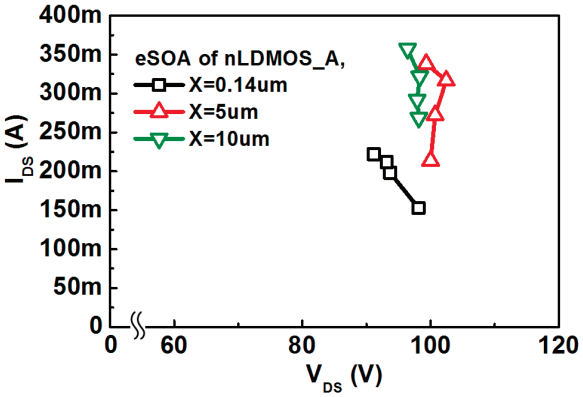
TABLE I
THE BREAKDOWN VOLTAGE (BV_{DSS}) AMONG DIFFERENT TEST DEVICES

Device (V_{GS}=0V)	BV_{DSS} (V) (X=0.14μm)	BV_{DSS} (V) (X=5μm)	BV_{DSS} (V) (X=10μm)
nLDMOS_S	77	78	78
nLDMOS_A	53	56	56
nLDMOS_B	74	75	75

The breakdown voltage of the test devices are summarized in Table I. Fig. 8 shows the measured eSOA boundary of nLDMOS_S, nLDMOS_A, and nLDMOS_B with different distances X of 0.14, 5, and 10 μm, respectively. The test devices are measured under gate biases of 0, 1, 3, and 5 V, respectively, where the last *I-V* points before snapback are acquired for eSOA boundary. According to the comparison of different eSOA in Fig. 8, the eSOA of nLDMOS_A is the widest one, while that of the nLDMOS_S is the worst. The eSOA of all test devices are slightly extended with a wide drain region when a large distance X is used. Although the eSOA of nLDMOS_A is the widest one, its breakdown voltage is lower than 60 V, which cannot be used in 60-V applications. However, the test results of nLDMOS_B can have a better eSOA than nLDMOS_S, as well as its breakdown voltage is about 75 V which is almost not degraded by the slotted DPW structure.



(a)



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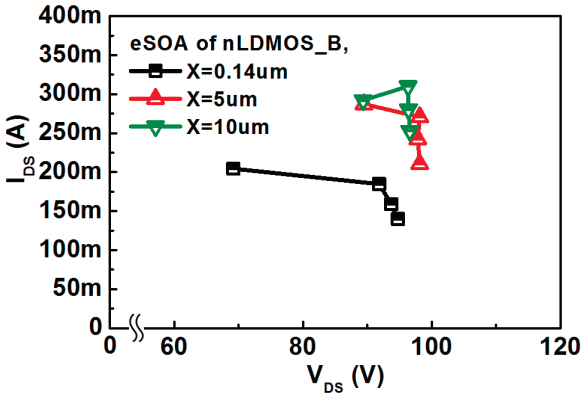

(c)

Fig. 8. The measured eSOA boundary of (a) nLDMOS_S, (b) nLDMOS_A, and (c) nLDMOS_B, with different distances X of 0.14, 5, and 10 μm, respectively.

B. TLP-Measured Results and ESD Robustness

Fig. 9 shows the TLP-measured characteristics under the same condition of V_{GS} = 0 V. The data of secondary breakdown current (I_{t2}) are extracted from the TLP-measured *I-V* curves. The TLP-measured results and ESD robustness among the three HV test devices are summarized in Table II. From the measurement results, the test devices immediately failed as the snapback happened. It indicated that the parasitic n-p-n BJT in test devices were not triggered on during ESD stress. Thus, the ESD current was totally discharged through the reverse diode path. Although the BJT path was not triggered on during ESD stress, the ESD robustness of all test devices can still be improved with a large distance X due to reduction of power density. Moreover, the ESD performance of nLDMOS_A is the greatest, while that of nLDMOS_S is

the worst. It demonstrates that the ESD current can be spread underneath the device, therefore reducing the power density and improving the ESD robustness. Similarly, the nLDMOS_B with slotted DPW structure can have better ESD robustness than that of nLDMOS_S.

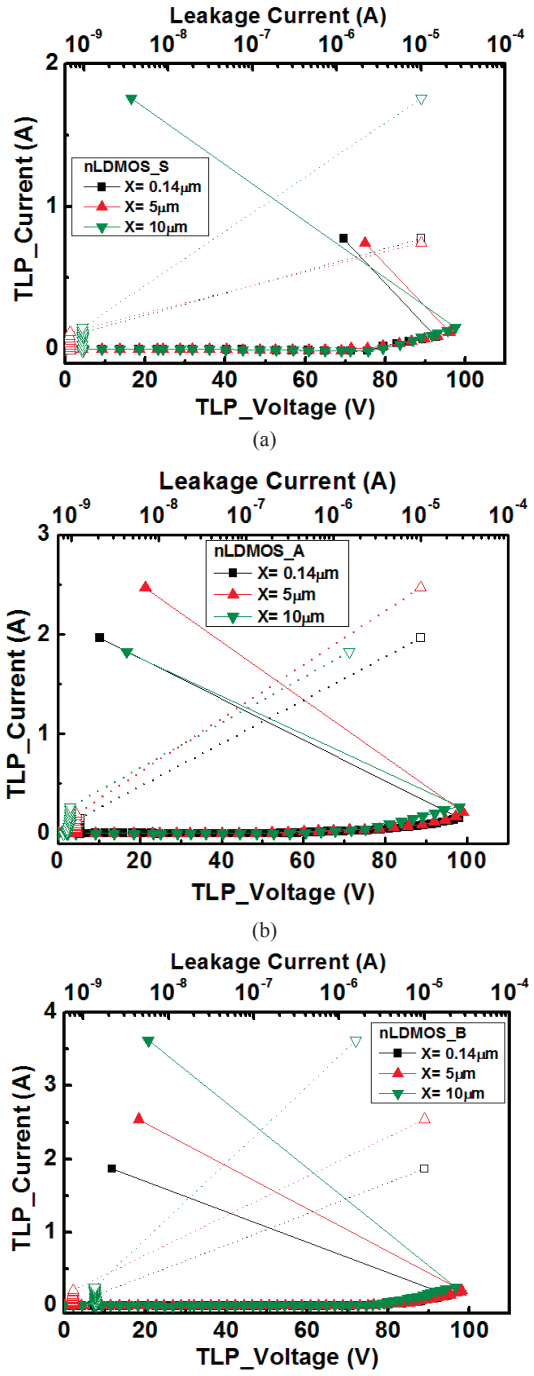

Fig. 9. The TLP-measured *I-V* characteristics of (a) nLDMOS_S, (b) nLDMOS_A, and (c) nLDMOS_B, with different distances X of 0.14, 5, and 10 μm, respectively.

IV. Conclusion

The test devices for self-protected HV MOSFET have been investigated with different DPW test structures in a 0.25-μm 60-V BCD process. According to the measurement results, the nLDMOS_B with slotted DPW structure can maintain high breakdown voltage for wide eSOA and get better ESD robustness at the same time. Therefore, nLDMOS with the appropriate drain-side engineering is a useful technique for self-protection ESD design in HV integrated circuits.

TABLE II
The Measured Results among Different Test Devices

Device (V_{GS}=0V)	TLP measurement	ESD tester	
	I_{t2} (A)	HBM (kV)	MM (V)
nLDMOS_S (X=0.14μm)	0.09	0.3	< 50
nLDMOS_S (X=5μm)	0.12	0.4	50
nLDMOS_S (X=10μm)	0.15	0.5	50
nLDMOS_A (X=0.14μm)	0.16	0.5	50
nLDMOS_A (X=5μm)	0.21	0.6	100
nLDMOS_A (X=10μm)	0.27	0.8	100
nLDMOS_B (X=0.14μm)	0.14	0.5	50
nLDMOS_B (X=5μm)	0.21	0.6	100
nLDMOS_B (X=10μm)	0.25	0.7	100

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References

[1] B. Murari, F. Bertoti, and G. A. Vignola, *Smart Power ICs: Technologies and Applications*. Berlin, Germany: Springer-Verlag, 2002.

[2] J. Webster, *Reliability Issues of Power Devices*, Wily Encyclopedia of Electrical and Electronics Engineering, 2007.

[3] M. P. J. Mergens, W. Wilkening, S. Mettler, H.wolf, A.Stricker, and W. Fichtner, "Analysis of lateral DMOS power devices under ESD stress condition," *IEEE Trans. on Electron Devices*, vol. 47, no.11, pp. 2128-2137, Nov. 2000.

[4] W.-Y. Chen and M.-D. Ker, "Improving safe operating area of an nLDMOS array with an embedded silicon controlled rectifier for ESD protection in a 24-V BCD process," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2944-2951, Sep. 2011.

[5] W.-Y. Chen and M.-D. Ker, "Characterization of SOA in time domain and the improvement techniques for using in high-voltage integrated circuits," *IEEE Trans. Device and Mater. Reliab.*, vol. 12, no. 2, pp. 382-390, Jun. 2011.

[6] S. Voldman, "Smart power, LDMOS, and BCD technology," in *ESD: Failure Mechanisms and Models*. Hoboken, NJ: Wiley, 2009.

[7] C.-T. Dai, P.-Y. Chiu, M.-D. Ker, F.-Y. Tsai, Y.-H. Peng, and C.-K. Tsai, "Failure analysis on gate-driven ESD clamp circuit after TLP stresses of different voltage steps in a 16V CMOS process," in *Proc. of International Symp. on Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2012.

[8] A. W. Ludikhuize, "A review of RESURF technology," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs*, 2000, pp. 11-18.

[9] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, "A double RESURF LDMOS with drain profile engineering for improved ESD robustness," *IEEE Trans. Electron Device Lett.,* vol. 23, no.4, pp. 212-214, Apr. 2002.