Resistor-Less Power-Rail ESD Clamp Circuit with Ultra-Low Leakage Current in 65nm CMOS Process

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***Abstract*—A resistor-less power-rail ESD clamp circuit realized with only thin gate oxide devices, and with SCR as main ESD clamp device, has been proposed and verified in a 65nm 1V CMOS process. Skillfully utilizing the gate leakage currents to realize the equivalent resistors in the ESD-transient detection circuit, the *RC*-based ESD-transient detection mechanism can be achieved without using an actual resistor to reduce the layout area in I/O cells. From the measured results, the proposed power-rail ESD clamp circuit with SCR width of 45μm can achieve 5kV HBM and 400V MM ESD levels under the ESD stress event, while consuming only a standby leakage current of 1.43nA at 25°C under the normal circuit operating condition with 1V bias.**

Keywords-Electrostatic discharge (ESD), gate leakage, power-rail ESD clamp circuit, silicon-controlled rectifier (SCR).

I. INTRODUCTION

In nanoscale CMOS technology, the gate oxide thickness has been scaled down to several nanometers and it causes the gate-tunneling issue more serious [1], [2]. For on-chip electrostatic discharge (ESD) protection, the ESD clamp device drawn in the layout style of big field-effect transistor (BigFET) had demonstrated excellent ESD protection performance [3]-[8]. However, the BigFET layout style is not adequate for low power consumption anymore in the nanoscale CMOS process because the BigFET of large device dimension with thin gate oxide would lead to intolerable gate leakage current. Therefore, the consideration of gate leakage issue has to be involved in the design of the ESD-transient detection circuit.

Recently, the low-leakage power-rail ESD clamp circuit in nanometer CMOS processes had been revealed [9]-[11]. In [9], the gate current was utilized to bias the ESD-transient detection circuit and to reduce the voltage drop across the MOS capacitors. In [10], the *RC*-based ESD-transient detection circuit with the feedback control inverter was used to avoid the direct leakage path through the MOS capacitor. In [11], the ESD-transient detection circuit consisted of the *RC* timer, inverters, and feedback pMOS, where the feedback pMOS used to lower the voltage drop across the *RC* timer and therefore to reduce the gate leakage current of the MOS capacitor. However, those previous circuits were more complicated with large layout area to implement the ESD-transient detection circuits.

In this work, a new resistor-less design of ESD-transient detection circuit is proposed and successfully verified in a 65nm 1V CMOS technology. The proposed ESD-transient detection circuit realized with core devices can be accurately activated to generate the trigger current to the ESD clamp device. According to the experimentally measured results, the standby leakage current of the proposed power-rail ESD clamp circuit can be significantly reduced to a few nano-ampere under the normal circuit operating condition with 1V bias.

II. GATE LEAKAGE CURRENT IN CONVENTIONAL DESIGNS

The *RC*-based power-rail ESD clamp circuit was typically used to protect the core circuits [12], as shown in Fig. 1(a). Under the normal circuit operating condition, the MOS capacitor Mc with a large poly-gate area would induce a large gate leakage current from node A to VSS in nanometer CMOS technology. A voltage drop across the resistor R is generated, and therefore the Mp cannot be completely turned off. The voltage of node B would be raised to a level higher than VSS due to the non-turned-off Mp. Finally, the main ESD clamp device M_{ESD} drawn with large device dimension operated in the sub-threshold region will further generate a huge leakage current from VDD to VSS.

The capacitor-less power-rail ESD clamp circuit was also proposed to protect the core circuits [13], as shown in Fig. 1(b). Under the normal circuit operating condition, the main ESD clamp device M_{ESD} drawn with large device dimension will induce a large gate current from drain to node B and the sub-threshold channel current in M_{ESD} from drain to source in nanometer CMOS process. The voltage drop across the Rp can be designed smaller to keep the Mn in the off state, and therefore the Mp can be virtually turned off. Consequently, the ESD-transient detection circuit can be almost turned off. However, the M_{ESD} drawn with large device dimension still contributes a large standby leakage current.

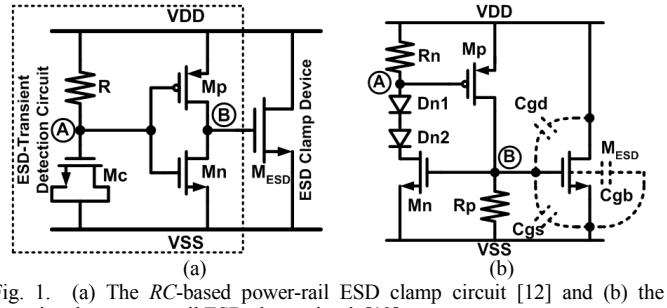
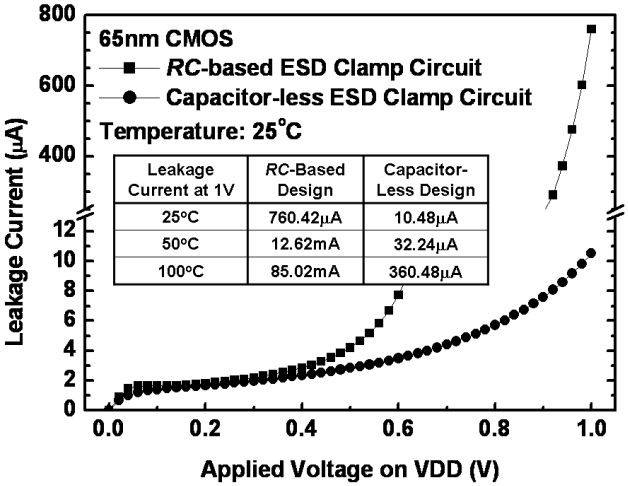


Fig. 1. (a) The *RC*-based power-rail ESD clamp circuit [12] and (b) the capacitor-less power-rail ESD clamp circuit [13].

The device dimensions and the total layout area of the *RC*-based (capacitor-less) power-rail ESD clamp circuit fabricated in a 65nm 1V CMOS process are R=165.3kΩ, Mc=64μm/2μm, Mp=184μm/60nm, Mn=36μm/60nm, M_{ESD}=2000μm/0.1μm, and 82.5×60μm^2 (Rp=20kΩ, Rn=40kΩ, Mp=24μm/60nm, Mn=12μm/60nm, M_{ESD}=2000μm/0.1μm, Dn1=Dn2=0.057μm^2, and 58×60μm^2). The measured standby leakage currents under different temperatures are shown in Fig. 2 and listed in the inset of Fig. 2. We can observe that MOS transistor drawn with large device dimension as the main ESD clamp device would be too

leaky in nanometer CMOS technology, which is not suitable for the portable products requiring low power consumption.



Leakage Current at 1V	*RC*-Based Design	Capacitor-Less Design
25°C	760.42μA	10.48μA
50°C	12.62mA	32.24μA
100°C	85.02mA	360.48μA

Fig. 2. The measured standby leakage currents of the *RC*-based and the capacitor-less power-rail ESD clamp circuits.

III. Proposed Resistor-Less ESD-Transient Detection Circuit

A. Circuit Schematic

The circuit scheme and chip microphotograph of resistor-less power-rail ESD clamp circuit are shown in Fig. 3 with the p-type triggered silicon-controlled rectifier (SCR) as the main ESD clamp device. The layout area of the proposed design is greatly reduced over 65%, as compared with that of prior works [10], [11]. Although the layout area of prior work [9] is almost equal to that of this work, the previous circuit is more complicated to implement the ESD-transient detection circuit. The SCR has no gate leakage current issue due to no poly-gate structure inside the SCR [14]. However, the ESD-transient detection circuit is necessary to enhance the turn-on speed of the SCR under ESD stress condition. The proposed ESD-transient detection circuit is designed with considerations of the gate leakage current and the gate oxide reliability. By inserting the diode in the ESD-transient detection circuit, the voltage differences across the gate oxide of the Mp can be intentionally reduced. By using the gate leakage current of the Mp, the induced equivalent resistors can be a part of ESD-transient detection mechanism. Therefore, the gate leakage current of the Mp can be well utilized to achieve the resistor-less design of ESD-transient detection circuit.

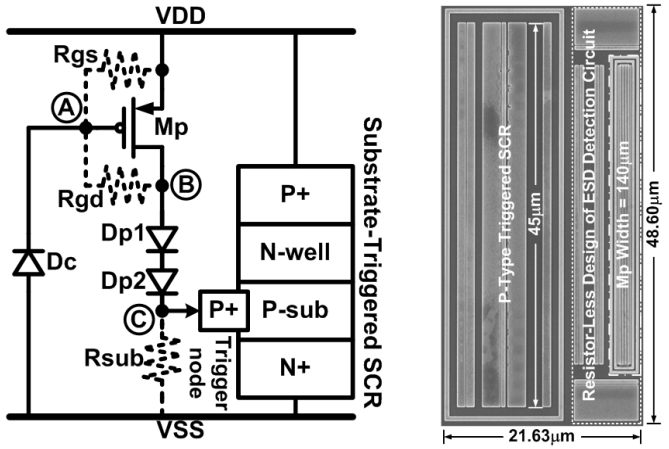


Fig. 3. The proposed resistor-less ESD detection circuit with the p-type substrate-triggered SCR as the ESD clamp device and its chip microphotograph.

B. Operation under Normal Power-On Transition

Under the normal circuit operating condition, the voltage of node A is biased at VDD through the resistors Rgs and Rgd induced by the gate leakage current of Mp. The voltage of node C is simultaneously biased at VSS through the parasitic p-substrate resistor Rsub in the p-type triggered SCR. Because Mp is kept off, no trigger current is generated into the trigger node of SCR. Inserting two diodes, Dp1 and Dp2, in the ESD-transient detection circuit can rise up the voltage of node B to the voltage level near VDD of 1V. All terminals of Mp are almost at the same voltage level to reduce its gate leakage. Therefore, the total leakage current and gate oxide reliability of Mp can be safely relieved.

With the SPICE parameters provided from foundry and the device sizes listed in Table I (adopting Mp width of 140μm), the simulated voltage waveforms and the leakage current of the proposed ESD-transient detection circuit are shown in Fig. 4. In Fig. 4, the voltage of node A is successfully charged to the voltage level of VDD due to the gate leakage current of Mp. Therefore, the Mp is completely turned off and the simulated standby leakage current of the proposed ESD-transient detection circuit is only 1.53nA when VDD is raised up to 1V.

TABLE I
Device Sizes of the Resistor-Less Power-Rail ESD Clamp Circuit

Device	Size								
Dp1 and Dp2 (μm^2)	14								
Dc (μm^2)	52.13			54.79			60.13		
Mp Width (μm)	35			70			140		
SCR Width (μm)	25	35	45	25	35	45	25	35	45

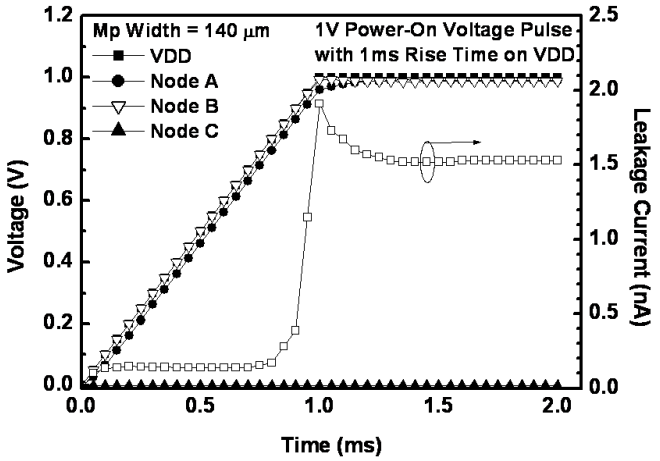


Fig. 4. Simulated voltage waveforms on the nodes and the leakage current of the proposed ESD-transient detection circuit under normal power-on transition.

C. Operation under ESD Transition

The *RC* time delay is consisted by the equivalent resistors, which are induced by gate leakage currents of Mp, and the junction capacitance of the reverse-biased diode Dc to achieve the resistor-less ESD-transient detection circuit. When a positive fast-transient ESD-like voltage is applied to VDD with VSS grounded, the *RC* time delay keeps the node A at a relatively low voltage level as compared with that at VDD. Consequently, Mp can be quickly turned on to generate the trigger current into the trigger node (node C) of SCR.

In order to simulate the fast-transient edge of the human-body-model (HBM) ESD event before the breakdown on the internal devices, a 4V voltage pulse with a rise time of 10ns is applied to VDD. The simulated transient voltage and the trigger current of the ESD-transient detection circuit are illustrated in Fig. 5. Mp is successfully turned on to generate the trigger current of ~41mA into SCR. Therefore, SCR can be fully triggered on to discharge the ESD current from VDD to VSS.

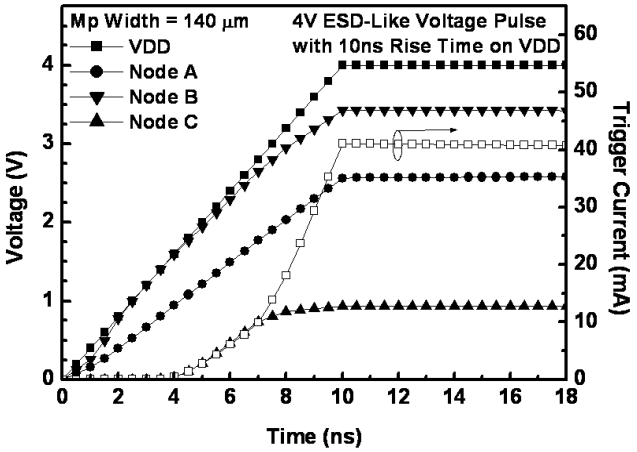


Fig. 5. Simulated voltage waveforms on the nodes and the trigger current of the proposed ESD-transient detection circuit under the ESD-like transition.

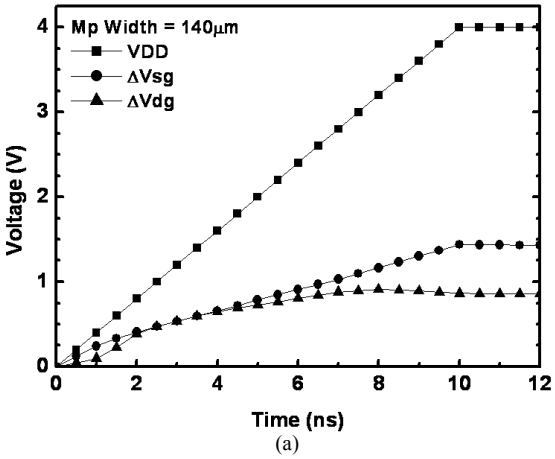
According to the simulated results in Fig. 5, the voltages across the source-to-gate and drain-to-gate (ΔVsg and ΔVdg) in time domain are plotted in Fig. 6(a). The corresponding gate leakage currents of source-to-gate and drain-to-gate (Isg and Idg) in time domain are drawn in Fig. 6(b). The gate leakage currents are in the order of nano-ampere. By using the Ohm's Law, the equivalent resistances (Rgs=ΔVsg/Isg and Rgd=ΔVdg/Idg) can be extracted from the voltage differences and the corresponding gate leakage currents, as shown in Fig. 6(c). During the period of ESD-like transition, the minimum values of Rgs and Rgd are 2.35MΩ and 6.43MΩ, respectively. With these large intrinsic equivalent resistors induced by the gate leakage current of Mp, the *RC* time delay can be achieved by adopting small-size reverse-biased diode Dc to reduce the layout area of the proposed ESD-transient detection circuit.

IV. Experimental Results

The resistor-less power-rail ESD clamp circuits have been fabricated in a 65nm 1V CMOS process. All devices in the proposed design are 1V fully-silicided devices, including the SCR device. The total layout area of the proposed design is $21.63\times48.60\mu m^2$, where the SCR width is 45μm. The widths of SCR devices are split with 25, 35, and 45μm to verify the corresponding ESD robustness. The gate widths of Mp are split with 35, 70, 140μm to investigate the trigger voltage of the proposed design. The resistor-less power-rail ESD clamp circuits are prepared for the measurements by transmission line pulsing (TLP), ESD test, DC I-V curve, and transient behavior.

A. TLP Measurement and ESD Robustness

The TLP generator with a pulse width of 100ns and a rise time of ~2ns is used in this measurement [15]. The TLP measured I-V curves of the proposed power-rail ESD clamp circuits with different SCR widths are shown in Fig. 7, where the device dimension of Mp is kept at 140μm/0.12μm. The power-rail ESD clamp circuit with SCR widths of 25μm, 35μm, and 45μm can achieve the It2 values of 1.48A, 2.14A, and 2.74A, respectively. The It2 and the trigger voltage of the power-rail ESD clamp circuit with different SCR widths and different Mp widths are listed in Table II. As seen in Table II, the It2 of the proposed design is proportional to the width of SCR. The trigger voltage can be obviously reduced by increasing the Mp width to generate larger trigger current. In addition, the SCR device with small width also has lower trigger voltage due to larger parasitic p-substrate resistor Rsub. Therefore, the turn-on speed of the SCR can be properly adjusted by the dimension of Mp. In Fig 7, the holding voltages of the SCR are ~2V, which is higher than the normal circuit operating voltage VDD of 1V. Therefore, the proposed designs are free to latchup issue for 1V applications [16], [17].



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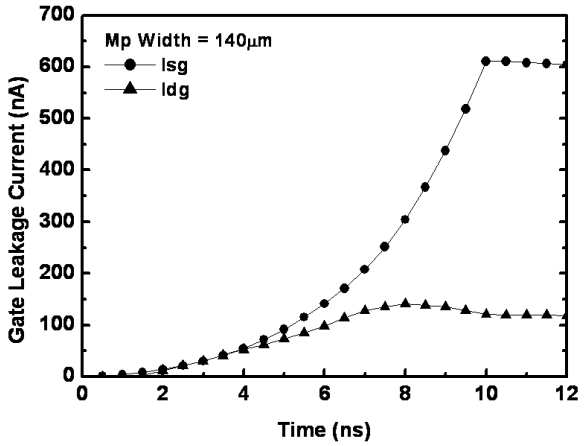

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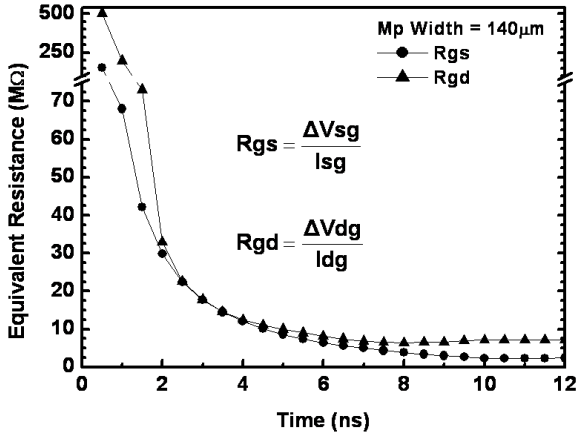


(c)

Fig. 6. Simulated values of (a) ΔVsg, ΔVdg, (b) Isg, Idg, and (c) the extracted equivalent resistances of Rgs and Rgd under the ESD-like transition.

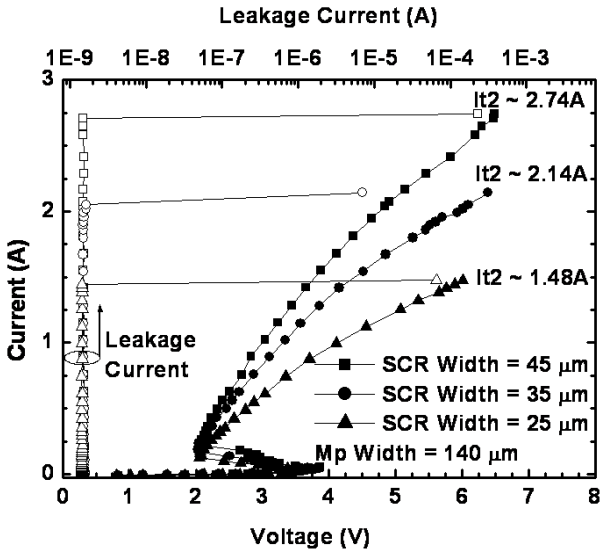


Fig. 7. TLP measured I-V curves of the resistor-less design of power-rail ESD clamp circuits.

TABLE II
MEASURED RESULTS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUITS

Mp Width (μm)		35			70			140		
SCR Width (μm)		25	35	45	25	35	45	25	35	45
It2		1.48A	2.17A	2.74A	1.48A	2.11A	2.71A	1.48A	2.14A	2.74A
Trigger Voltage		4.26V	4.71V	5.17V	3.79V	4.02V	4.26V	3.60V	3.75V	3.86V
HBM ESD Level		3kV	4kV	5kV	3kV	4kV	5kV	3kV	4kV	5kV
MM ESD Level		200V	300V	400V	200V	300V	400V	200V	300V	400V
Leakage Current (@ 1V)	25°C	1.12nA	1.12nA	1.13nA	1.31nA	1.31nA	1.32nA	1.43nA	1.43nA	1.43nA
	50°C	6.69nA	6.80nA	6.84nA	8.18nA	8.48nA	8.65nA	12.13nA	12.55nA	12.62nA
	100°C	0.19μA	0.19μA	0.19μA	0.26μA	0.26μA	0.26μA	0.33μA	0.33μA	0.33μA

The measured HBM and machine-model (MM) ESD levels of the proposed design itself measured by ZapMaster tester under positive VDD-to-VSS ESD stress are also listed in Table II. The measured HBM (MM) ESD levels of the SCR with the widths of 25, 35, and 45μm are 3, 4, and 5kV (200, 300, and 400V), respectively. The measured HBM and MM ESD levels of the proposed power-rail ESD clamp circuits are also proportional to the width of SCR.

Charged-device model (CDM) is also an important ESD testing standard for ICs. In order to investigate the turn-on behavior of the proposed designs under CDM-like fast-transient condition, the very fast TLP (VF-TLP) with a pulse width of 10ns and a rise time of 200ps is used to measure the proposed power-rail ESD clamp circuits. The measured VF-TLP I-V curves of the resistor-less power-rail ESD clamp circuits with different SCR widths are shown in Fig. 8, where the width of Mp is kept at 140μm. In Fig. 8, the proposed power-rail ESD clamp circuits can be successfully activated to achieve higher It2 than those measured by TLP measurement due to the shorter pulse width of VF-TLP. In addition, the measured It2 from VF-TLP are also well proportional to the width of SCR.

The breakdown voltage of gate oxide under HBM timescale is about ~5V in 65nm CMOS process. The trigger voltage of the proposed design can be obviously reduced by increasing the Mp width to generate larger trigger current. In addition, the on-resistance can be reduced by directly enlarging the width of SCR. In practice, the circuit designer would place the power-rail ESD clamp circuits in every specific distance to protect their internal circuit. Therefore, those power-rail ESD clamp circuits are in parallel and the on-resistance can be further lowered to adequately protect the gate oxide when all power-rail ESD clamp circuits are turned on.

B. Standby Leakage Measurement

The DC I-V curves of the fabricated power-rail ESD clamp circuits are measured by HP4155 at 25°C, as shown in Fig. 9 and listed in Table II. In Fig. 9, the largest standby leakage current is only 1.43nA under 1V bias when the Mp width is 140μm. In Table II, the standby leakage currents of the power-rail ESD clamp circuits are almost unrelated on SCR widths, because the leakage current in the SCR device is quite small. The measured standby leakage currents of the fabricated power-rail ESD clamp circuits under 1V bias at 50°C and 100°C are also listed in Table II. The standby leakage currents of the fabricated power-rail ESD clamp circuits are reduced to the order of nano-ampere because the gate oxide reliability of Mp is significantly relieved by inserting the reverse-biased diode Dc and the diodes, Dp1 and Dp2, in the ESD-transient detection circuit. Although increasing the width of Mp causes a slightly increased standby leakage current, it can increase the trigger current to improve the turn-on speed of the SCR with a reduced trigger voltage (as shown in Table II).

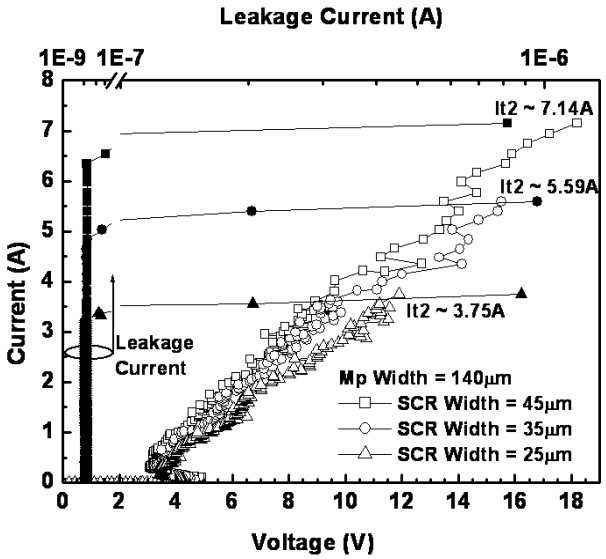


Fig. 8. VF-TLP measured I-V curves of the resistor-less power-rail ESD clamp circuits with Mpd width of 140μm under positive VDD-to-VSS ESD stress.

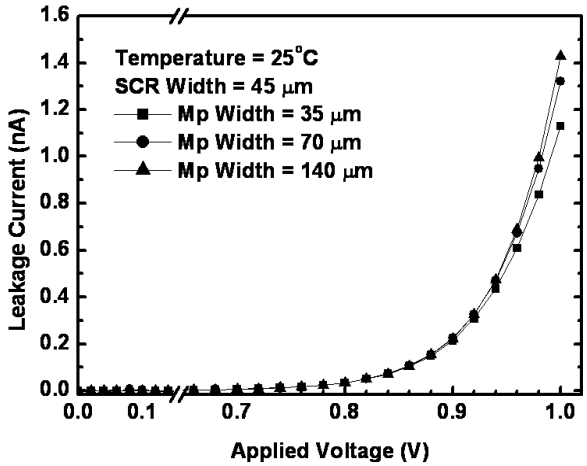
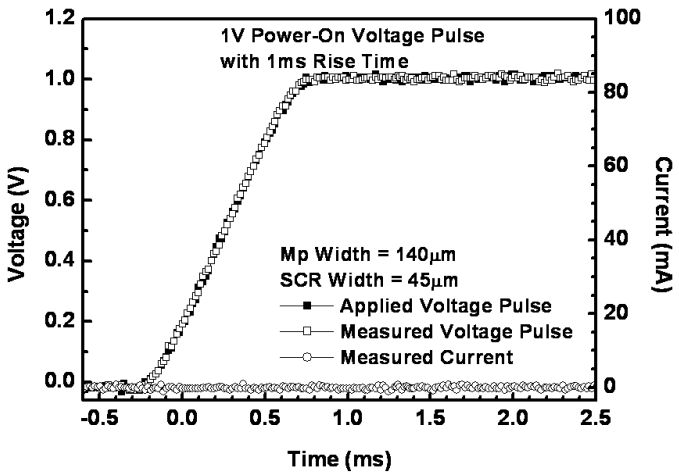


Fig. 9. The measured DC I-V curves of the fabricated power-rail ESD clamp circuits with different widths of Mp at room temperature.

C. Turn-On Verification

For normal power-on condition, the voltage pulse usually has a rise time in the order of milliseconds. As shown in Fig. 10(a), the measured voltage on VDD power line rises up to 1V and the measured current is near zero. However, some previous studies [6], [18] have demonstrated that the power-rail ESD clamp circuits with *RC*-based ESD-transient detection circuits were easily mis-triggered or into the latch-on state under the fast power-on condition. The proposed power-rail ESD clamp circuits have been applied with 1V voltage pulse with 20ns rise time to investigate the immunity against mis-trigger, as shown in Fig. 10(b). The measured voltage on VDD power line is not degraded and the measured current is also at the level near zero. The inserted diodes, Dp1 and Dp2, in ESD-transient detection circuit can ensure that there would not be any on-current flowing through themselves from VDD to VSS. Therefore, the resistor-less design of ESD-transient detection circuit is free from the transient-induced latch-on or mis-trigger issues.



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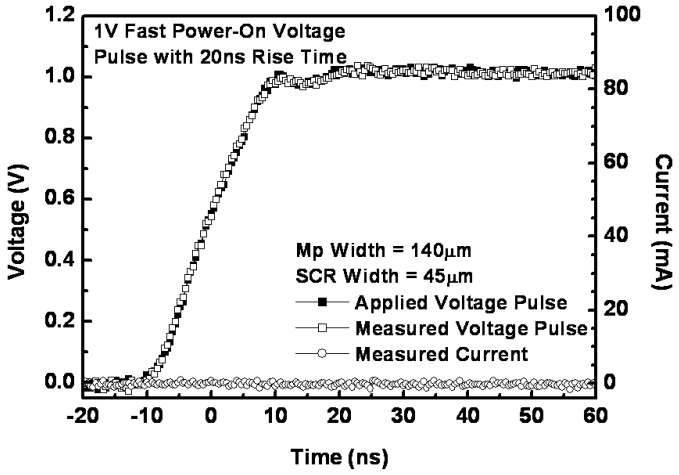


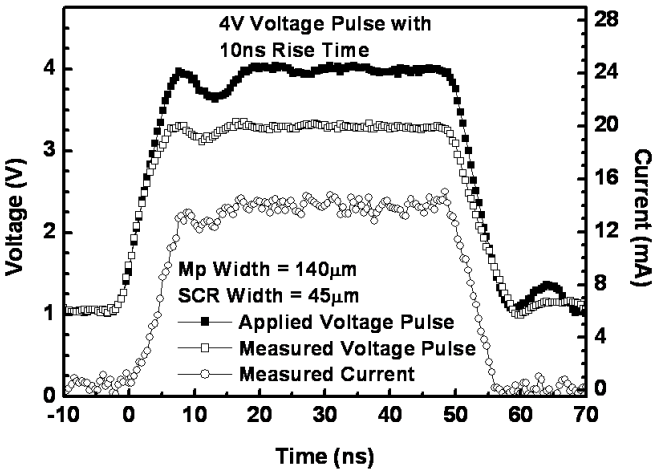
(b)

Fig. 10. The measured transient voltage and current waveforms of the proposed power-rail ESD clamp circuit under the 1V power-on transitions with the rise time of (a) 1ms and (b) 20ns.

The transient voltage with a pulse height of 4V and a rise time of 10ns is applied to the VDD power line with 1V operation voltage to verify any latch-on issue. As shown in Fig. 11(a), the transient voltage will activate the ESD-transient detection circuit to generate the trigger current of ~14mA. The applied 4V transient voltage is clamped down to a lower voltage level of ~3.3V by the proposed power-rail ESD clamp circuit. After the transient, the voltage on VDD power line is back to 1V operation voltage and the current is almost zero.

In order to observe the transient behavior of the proposed ESD-transient detection circuit, a TLP 4V voltage pulse with a rise time of 2ns is applied to the VDD power line with the VSS grounded. The TLP voltage pulse can initiate the ESD-transient detection circuit to generate the trigger current to trigger on the SCR. The measured voltage and current waveforms in time domain on VDD power line are shown in Fig. 11(b). The applied 4V voltage pulse can be quickly clamped down to a lower voltage level of ~3.0V by the proposed ESD-transient detection circuit with the trigger current of ~20mA. When the TLP voltage pulse height is increased, the proposed ESD-transient detection circuit can generate more trigger current into the SCR. The triggered-on SCR can provide a low impedance path from VDD to VSS to discharge ESD current and clamp down the voltage level. Overall, the proposed ESD-transient

detection circuit can be successfully activated by the voltage pulse with fast transient edge to trigger on the SCR.



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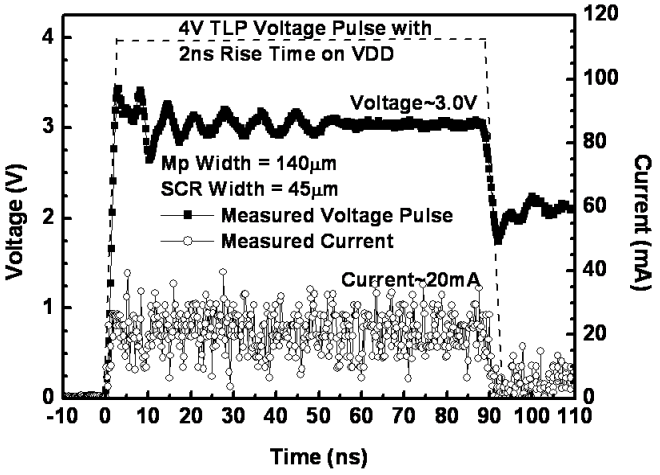

(b)

Fig. 11. Measured voltage and current waveforms of the proposed power-rail ESD clamp circuit under (a) transient noise and (b) TLP transition conditions.

V. CONCLUSION

Resistor-less ESD-transient detection circuit to achieve ultra-low standby leakage current and small layout area has been proposed and successfully verified in a 65nm 1V fully-silicided CMOS technology. The proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate leakage and gate oxide reliability issues. According to the measured results, the standby leakage current of the proposed power-rail ESD clamp circuit is only 1.43nA under 1V bias at room temperature. Moreover, the proposed power-rail ESD clamp circuit has excellent immunity against the transient-induced latch-on or mis-trigger issues. The resistor-less power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS process.

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REFERENCES

[1] M. Luisier and A. Schenk, "Two-dimensional tunneling effects on the leakage current of MOSFETs with single dielectric and high-k gate stacks," *IEEE Trans. on Electron Devices*, vol. 55, no. 6, pp. 1494-1501, Jun. 2008.

[2] P. J. Wright and K. C. Saraswat, "Thickness limitations of SiO_2 gate dielectrics for MOS ULSI," *IEEE Trans. on Electron Devices*, vol. 37, no. 8, pp. 1884-1892, Aug. 1990.

[3] M. Stockinger, J. Miller, M. Khazhinsky, C. Torres, J. Weldon, B. Preble, M. Bayer, M. Akers, and V. Kamat, "Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symposium*, 2003, pp. 17-26.

[4] J. Li, R. Gauthier, and E. Rosenbaum, "A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symposium*, 2004, pp. 273-279.

[5] J. Li, R. Gauthier, S. Mitra, C. Putnam, K. Chatty, R. Halbach, and C. Seguin, "Design and characterization of a multi-RC-triggered MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symposium*, 2006, pp. 179-185.

[6] S.-H. Chen and M.-D. Ker, "Area-efficient ESD-transient detection circuit with smaller capacitance for on-chip power-rail ESD protection in CMOS ICs," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 56, no. 5, pp. 359-363, May 2009.

[7] J. C. Smith and G. Boselli, "A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symposium*, 2003, pp. 8-16.

[8] J. C. Smith, R. A. Cline, and G. Boselli, "A low leakage low cost-PMOS based power supply clamp with active feedback for ESD protection in 65nm CMOS technologies," in *Proc. EOS/ESD Symposium*, 2005, pp. 298-306.

[9] C.-T. Wang and M.-D. Ker, "Design of power-rail ESD clamp circuit with ultra-low standby leakage current in nanoscale CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3, pp. 956-964, Mar. 2009.

[10] M.-D. Ker and P.-Y. Chiu, "New low-leakage power-rail ESD clamp circuit in a 65-nm low-voltage CMOS process" *IEEE Trans. on Device and Materials Reliability*, vol. 11, no. 3, pp. 474-483, Sep. 2011.

[11] M.-D. Ker and C.-Y. Lin, "High-voltage-tolerant ESD clamp circuit with low standby leakage in nanoscale CMOS process," *IEEE Trans. on Electron Devices*, vol. 57, no. 7, pp. 1636-1641, Jul. 2010.

[12] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, no. 1, pp. 173-183, Jan. 1999.

[13] C.-T. Yeh and M.-D. Ker, "Capacitor-less design of power-rail ESD clamp circuit with adjustable holding voltage for on-chip ESD protection," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2476-2486, Nov. 2010.

[14] M.-D. Ker and K.-C. Hsu, "Latchup-free ESD protection design with complementary substrate-triggered SCR devices," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1380-1392, Aug. 2003.

[15] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. of EOS/ESD Symp.*, 1985, pp. 49-54.

[16] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits,* John Wiley & Sons, 2009.

[17] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. on Electron Devices*, vol. 52, no. 8, pp. 1821-1831, Aug. 2005.

[18] C.-C. Yen and M.-D. Ker, "The effect of IEC-like fast transients on *RC*-triggered ESD power clamps," *IEEE Trans. on Electron Devices*, vol. 56, no. 6, pp. 1204-1210, Jun. 2009.