Low-Leakage Power-Rail ESD Clamp Circuit With Gated Current Mirror in a 65-nm CMOS Technology

Federico A. Altolaguirre* and Ming-Dou Ker*†
*Insitute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
†Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan.

***Abstract*—A new power-rail ESD clamp circuit is proposed and verified with consideration of the gate leakage issue in 65-nm CMOS technology. The proposed circuit can reduce the total leakage current of the traditional power-rail ESD clamp circuit in two orders of magnitude. Moreover, the proposed circuit reduces the required silicon area by boosting the capacitor with a current mirror. The measured leakage current of the proposed power-rail ESD clamp circuit is 220nA ($V_{DD} = 1V$, T=25 °C), much lower than the 20.55μA of the traditional design. In addition, the required area for the proposed design is $50\mu\text{m} \times 30\mu\text{m}$, which is a 40% reduction in silicon area to the traditional one, that can sustain the HBM (MM) ESD stress of 3.5kV (250V).**

I. Introduction

Electrostatic discharge (ESD) is a major reliability issue in the IC industry. The ESD phenomenon happens when, for example, a body charged with electrostatic charge is touching an IC. The potential difference between body and chip will cause a current flow to balance the charges. The peak ESD currents of human body can be up to several amperes, with ESD voltages of thousands volts. Such discharges can cause serious damage to the internal components of the ICs. Therefore, to protect the ICs from ESD damage, special components for ESD protection are placed around the I/O and power-supply (V_{DD} and V_{SS}) pads. The typical whole-chip ESD protection design is shown in Fig. 1. In such a scheme, the power-rail ESD clamp circuit plays an important role to improve the ESD robustness of IC chips [1].

With the continuous shrinking in CMOS technologies, the transistor gate oxide has been scaled down to less than 2nm. With such an ultra-thin oxide, the gate tunneling current becomes noticeable and cannot be neglected. This leakage current has been previously studied and characterized [2], and it has been included in the BSIM4 SPICE model [3]. The gate leakage impacts seriously in the traditional power-rail ESD clamp circuit. The big capacitor used for ESD transient detection, which is traditionally realized with a MOSFET, suffers from a very large leakage current. Moreover, the voltage drop across the resistor caused by this leakage current slightly turns on the driver transistor, adding another leakage current. The resulting total leakage current of the traditional power-rail ESD clamp circuit in nanoscale CMOS technologies becomes too large; therefore a re-design of the power-rail ESD clamp circuit with gate leakage consideration is required.

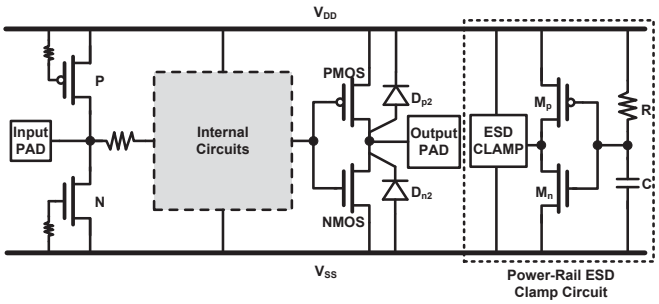

Fig. 1. Typical whole-chip ESD protection scheme designed with the power-rail ESD clamp circuit.

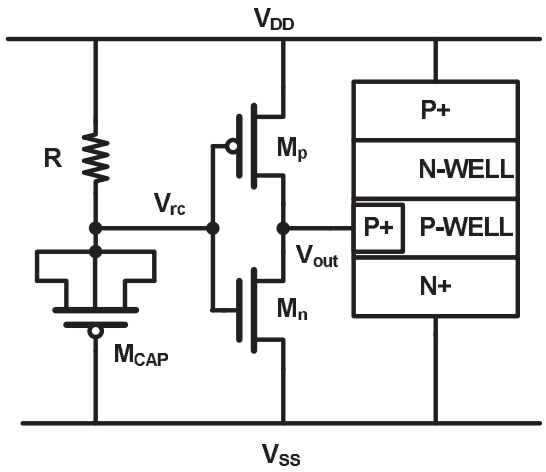

Fig. 2. Traditional power-rail ESD clamp circuit realized with the RC-based ESD transient detection and the substrate-triggered SCR device.

II. Impact of the Gate Leakage in the Power-Rail ESD Clamp Circuit

Fig. 2 shows the traditional power-rail ESD clamp circuit using a silicon-control-rectifier (SCR) as main ESD clamp. The SCR is a better choice than the BIGFET, which can provide better ESD robustness with smaller area [4]. Another reason is that with the gate leakage issue, the BIGFET will have a huge leakage current from drain to gate during the stand-by mode. Because the SCR is current triggered, the transistor M_p has to be enlarged in size to provide an adequate trigger current. The size of M_p is often determined by experience from previous

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TABLE I
DEVICE DIMENSIONS OF THE FABRICATED POWER-RAIL ESD CLAMP CIRCUITS

	R	M_{CAP}	M_p	M_n	M_1	M_2	M_3	SCR
Traditional Design	50kΩ	$20\mu\text{m} \times 20\mu\text{m}$	100μm/150nm	1μm/150nm	—	—	—	40 μm
Proposed Design	50kΩ	$3\mu\text{m} \times 1.5\mu\text{m}$	100μm/150nm	1μm/150nm	1μm/150nm	19μm/150nm	10μm/150nm	40 μm

runs. The chosen size for M_p is $W/L = 100\mu\text{m}/150\text{nm}$ in this work. The capacitor for the RC delay is realized with a PMOS to reduce the required area, though some previous work used MOM capacitor without too much area overhead [5]. The device dimensions of all components for the traditional power-rail ESD clamp circuit implemented in a 65-nm CMOS process are shown in Table I.

When an ESD is zapping at V_{DD} (with V_{SS} grounded), the RC delay cannot follows up the fast rising transient of V_{DD}. So V_{rc} is initially ∼0V and then starts increasing exponentially with the RC time constant (the RC time constant is designed ∼100ns, which is slow enough for typical ESD stresses). As V_{rc} is kept at a lower potential than V_{DD}, the transistor M_p is turned on and triggers the SCR to discharge the ESD current.

Under normal circuit operation, when V_{DD} is stable at the operating voltage, there is ideally no current through the RC circuit, so V_{rc} is tied to V_{DD} and M_p is turned off. The transistor M_n is then turned on to avoid mistriggering the SCR due to noise in V_{DD}. The assumption that there is no current flowing through the RC delay circuit is true for the older CMOS technologies, but not for the 65-nm CMOS process with thinner gate oxide. Due to the gate leakage issue, there is a large current flowing through M_{CAP}, and so $V_{rc} < V_{DD}$. Therefore, M_p is slightly turned on to cause another leakage path from V_{DD} to ground. Simulations verified that the current through the capacitor is larger than 10μA for $V_{DD} = 1V$. The total leakage current in the traditional power-rail ESD clamp circuit is 29.3μA, with $V_{DD} = 1V$ and T = 25 °C.

III. PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

From the viewpoint of efficiency, the traditional power-rail ESD clamp circuit has two major issues: high leakage current and large area implementation. The high leakage current will make the traditional design not adequate for low-power applications. On the other side, the large area required to implement the power-rail ESD clamp circuit will lend to higher fabrication cost. Some previous works have reported an improvement in the reduction of the leakage current [5], [6], but the area of these designs is, at best, the same as that of the traditional design.

A technique to reduce the area of a capacitor in high-voltage CMOS technologies was previously reported [7]. This technique is the basis of the proposed design in this work. Consider the circuit shown in Fig. 3(a). The transistors M_1 and M_2 are connected as a current mirror, so the current flowing through the capacitor is amplified by the current mirror ratio.

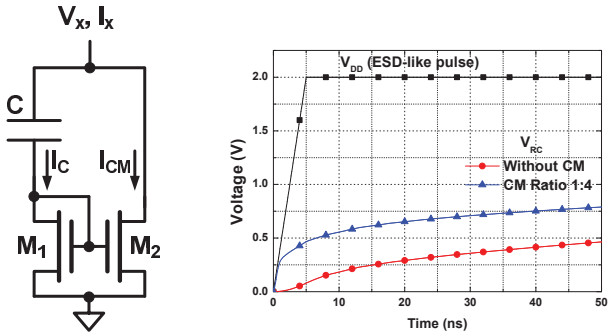


Fig. 3. (a) Simplified schematic for the boosted capacitor, and (b) simulation results for the RC delay circuit in a 65-nm CMOS process. Notice that the capacitor was implemented with a PMOS to provide a more accurate simulation. The capacitor size is modified with the selected current mirror ratio to provide the same effective capacitance.

This can be written as

$$I_{CM} = A \cdot I_C, \tag{1}$$

where

$$A = \frac{W_2/L_2}{W_1/L_1}. \tag{2}$$

If the gate-source voltage drop at M_1 is neglected, then

$$I_C = \frac{d}{dt} V_x, \tag{3}$$

and the total current I_x is given by

$$I_x = I_C \cdot (A+1), \tag{4}$$

$$I_x = C \cdot (A+1) \cdot \frac{d}{dt} V_x. \tag{5}$$

Equation (5) shows that the impedance seen at the node V_x is a capacitance of $A + 1$ times the value of C. Therefore, the capacitance value is effectively boosted by the current mirror. Fig. 3(b) shows a simulation of an RC delay using the boosted capacitance. The node V_{rc} raises exponentially as the traditional RC circuit, but with an offset caused by the V_{GS} voltage of M_1. Nonetheless, the difference between V_{DD} and V_{rc} is large enough to guarantee a correct detection of ESD events.

If the capacitor is implemented with the leaky PMOS, the leakage current of this transistor is also amplified by the current mirror. To avoid the leakage amplification during normal circuit operation, an additional switch (M_3) is added to the amplifying branch of the current mirror, as shown in Fig. 4. This switch is "open" during normal circuit operation,

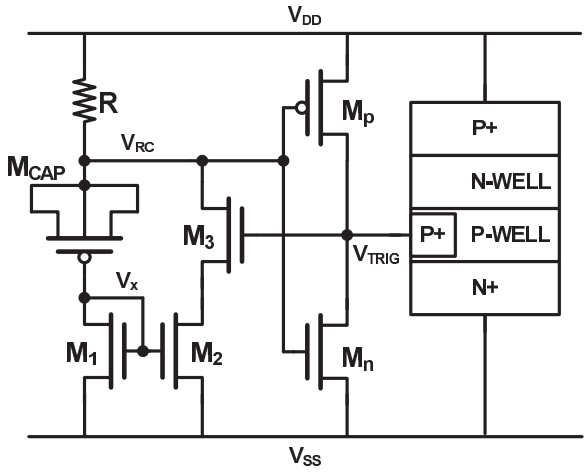


Fig. 4. Proposed power-rail ESD clamp circuit with the gated current mirror.

so the leakage current is only the one of the small capacitor. The switch control is done by using feedback. During normal circuit operation, V_{rc} is tied at V_{DD} by the resistor, so the node V_{TRIG} is tied to V_{SS} by M_n. Therefore, the transistor M_3 is turned off. Under a positive ESD stress between V_{DD} and V_{SS}, the node V_{rc} is initially kept at ∼0V and starts charging with the smaller time constant until M_p is turned on to drive V_{TRIG} high, therefore M_3 is turned on. After M_3 is turned on, V_{rc} starts charging with the longer time constant, therefore the SCR is kept triggered during all the ESD event. As smaller the capacitor is, V_{rc} will raise to a higher voltage during the transient. This will cause a shorter period for the transistor M_p to be turned on, thus reducing the apparent time constant. Therefore, there is a limit on how small the capacitor can be used. According to the simulations, the smaller capacitor obtained is $W/L = 3\mu\text{m}/1.5\mu\text{m}$. With this capacitor of smaller dimension, the current mirror ratio is set to 19 to create an equivalent capacitance similar to that used in the traditional power-rail ESD clamp circuit. The final device dimensions of the proposed power-rail ESD clamp circuit are also shown in Table I.

IV. Experimental Results

A test chip has been fabricated in a 65-nm CMOS general purpose (GP) fully-silicide process, including the traditional and the proposed power-rail ESD clamp circuits with the device dimensions as specified in Table I. The SCR used in the power-rail ESD clamp circuits is shown in Fig. 5. The width of the SCR is 40μm. The layouts of the fabricated power-rail ESD clamp circuits are shown in Fig. 6(a) and Fig. 6(b). The chip microphotography with different designs of power-rail ESD clamp circuits is shown in Fig. 6(c).

To measure the leakage current, the circuits are probed on-die at the controlled temperatures of 25 °C and 125 °C, under 1V bias. The traditional power-rail ESD clamp circuit shows a leakage current of 20.55μA and 103μA at T = 25 °C and T = 125 °C, respectively. For the proposed power-rail ESD clamp circuit, the leakage current is only 220nA

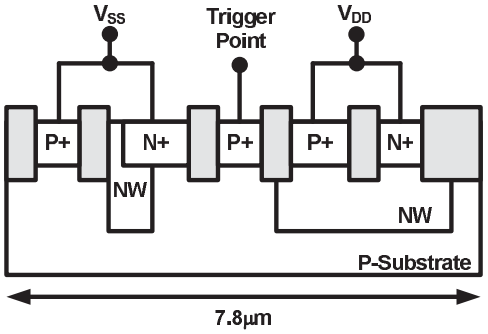
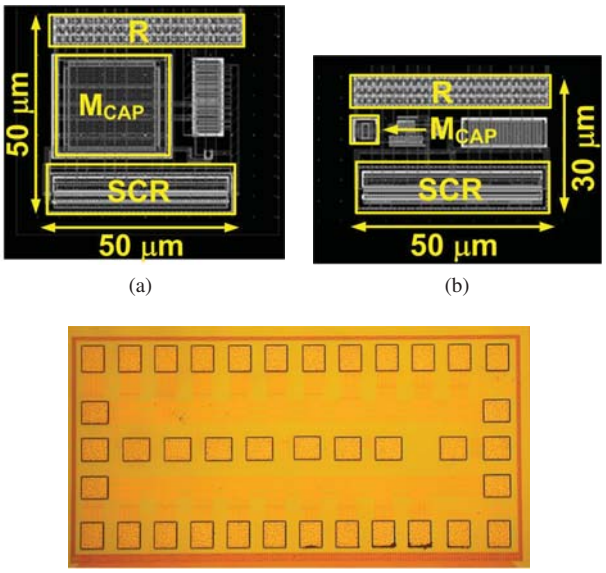


Fig. 5. Cross-section view of the SCR used in this work.



(a) (b)

(c)

Fig. 6. Layout of (a) the traditional power-rail ESD clamp circuit, (b) the proposed power-rail ESD clamp circuit, and (c) chip microphotography.

and 1.42μA at T = 25 °C and T = 125 °C, respectively. The leakage currents under different biases and temperature conditions can be observed in Fig. 7.

Another important verification is the turn-on speed of the ESD clamp circuit [8]. A 5V square pulse with 5ns rise time and 100ns pulse width is applied to the V_{DD} pad of the device under test (DUT) with V_{SS} grounded. The voltage at the pad is monitored by an oscilloscope to verify whether the pad voltage is clamped by the SCR. Fig. 8 shows the measurement results. The clamping voltage of the proposed design (∼2.8V) is a little higher than than of the traditional design (∼2.6V), because V_{RC} is at a higher voltage and therefore the SCR trigger current is smaller. But, they are all below the gate oxide breakdown voltage (∼5V).

The final measurement is to test the ESD levels with the HBM and MM ESD models. Both circuits failed after 4kV HBM stress and 300V MM stress. FA analysis is shown in Fig. 9. Notice that the HBM damage is due to the guard ring too close to the SCR. If this guard ring is moved further, the HBM level should be increased.

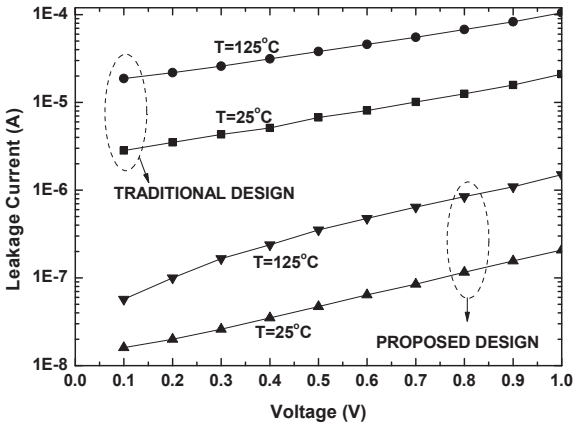


Fig. 7. Leakage current for the traditional and proposed power-rail ESD clamp circuits under different bias and temperature conditions.

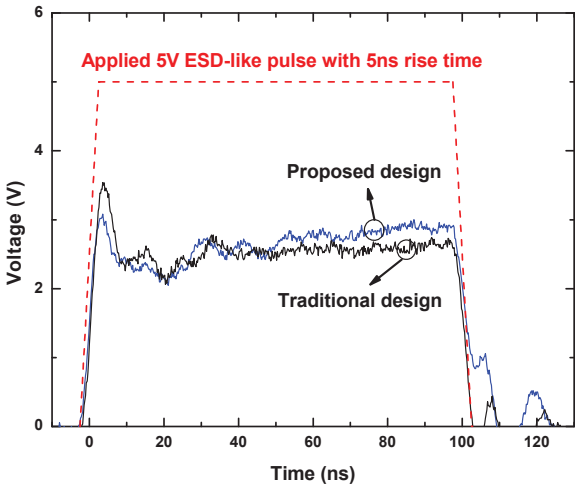


Fig. 8. Turn-on verification on the proposed and the traditional power-rail ESD clamp circuits.

V. Conclusions

The proposed power-rail ESD clamp circuit has been verified successfully, showing an increased performance compared to the traditional power-rail ESD clamp circuit. A comparison between the traditional power-rail ESD clamp circuit and the proposed circuit is shown in Table II. By using the boosted capacitor with gated current mirror, the required area for the power-rail ESD clamp circuit can be reduced 40%. The leakage current of the proposed circuit shows a reduction of 2 orders in the magnitude from that of the traditional power-rail ESD clamp circuit. In addition, the SCR holding voltage (∼2.8V) in the 65-nm CMOS process is higher than the operating supply voltage (1V), so there is no latch-up issue.

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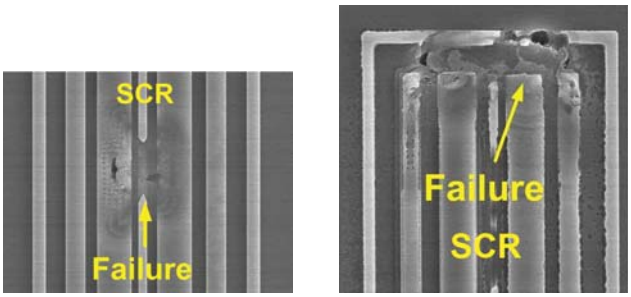
TABLE II
Comparison of Experimental Results

Circuit	Traditional	This work
Leakage current (T=25 °C)	20.55μA	220nA
Leakage current (T=125 °C)	103μA	1.42μA
HMB Level	3.5kV	3.5kV
MM Level	250V	250V
Area	$50\mu m \times 50\mu m$	$50\mu m \times 30\mu m$

The bias voltage for leakage measurement is 1V.



(a) (b)

Fig. 9. SEM images showing the failure location after ESD test by (a) 300V MM stress and (b) 4kV HBM stress.

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