Self-Protected LDMOS Output Device with Embedded SCR to Improve ESD Robustness in 0.25-μm 60-V BCD Process

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Abstract **— For high-voltage output driver, the lateral DMOS (LDMOS) is often used for both output function operation and self-protection against electrostatic discharge (ESD) events. In this work, a new structure of LDMOS output device with embedded SCR has been proposed and verified in a 0.25-μm 60-V BCD process. This new structure, with additional p+ and n+ implantation regions added between the drain contact and poly-gate of LDMOS, can keep it stably in the high-current holding region after snapback. By using this structure, the LDMOS can provide high enough self-protected ESD robustness for applications in the high-voltage output drivers.**

Index Terms **— Electrostatic discharges (ESD), lateral diffused MOS (LDMOS), silicon-controlled rectifier (SCR).**

I. INTRODUCTION

High-voltage operations are often used in the industrial applications, such as automotive electronics, green energy, power management ICs, and industrial control. One of the most popular structures in high-voltage process is the Lateral Diffused MOS (LDMOS) which is widely used as an output device. Therefore, LDMOS was expected to have self-protected capability against electrostatic discharge (ESD).

Some previous studies showed that the reduced surface field (RESURF) technique can advance those high voltage LDMOS transistors by having lower ON-state resistance and higher breakdown voltage [1], [2]. The higher breakdown voltage means larger safe operation area (SOA) which prevents noise mis-trigger the parasitic structure. Also, the lower ON-state resistance can increase the driving current during the normal operation. Some high doping layer added to enhance the driving efficiency is not good for the device against electrostatic discharge, because the lower resistance would cause difficulty for the parasitic BJT to be turned on. If the parasitic BJT does not turn on before the device get some unrecoverable damage from the ESD-generated heat, the device may fail in low stress level. Therefore, the stand-alone LDMOS which following the foundry rule with SOA consideration in high voltage process is not a good self-protection ESD device.

There are several solutions proposed to increase the ESD robustness of nLDMOS. The most popular way to improve ESD robustness is inserting silicon controlled rectifier (SCR) into the LDMOS [3]-[5]. SCR is known as an area-efficient method to improve ESD robustness, but it may have higher trigger voltage than that of stand-alone LDMOS. Under ESD stress, the stand-alone LDMOS may fail before the embedded SCR is triggered on to discharge ESD current.

The embedded SCR can work for ESD protection if it can get into snapback region stably. So, the critical issue is how to let the parasitic BJT inside the LDMOS turn on during ESD stress. Two solutions have been realized in some previous works [6]-[10]. One kind of design is to provide some trigger current which can turn on the parasitic BJT [6], [7]. Another way is to optimize the structure of LDMOS by changing the layout style [8]-[10]. One of the previous works reported that increasing the space between the poly-gate and the active region in drain side with shallow trench isolation (STI) may help to trigger the parasitic npn device inside the LDMOS [10]. However, some devices still failed before it got into the snapback region, especially when the operating voltage is greater than 40V.

This work combines the concepts of changing the layout space and embedded SCR inside LDMOS to develop a new structure of self-protected LDMOS (which is named as LDMOS-SCR). The new proposed LDMOS-SCR has additional p+ and n+ implantation regions between its drain and poly-gate to make sure that it can keep stably in the high-current holding region after snapback for improving ESD robustness.

II. DEVICE STRUCTURE

In 0.25-μm 60-V BCD process, the cross-section view of stand-alone LDMOS is shown in Fig. 1. Different space of the STI between gate and drain, which is marked as the parameter S in Fig. 1, will not help the LDMOS snapback. The transmission-line-pulsing (TLP) measurement results on the stand-alone LDMOS in Fig. 2 can indicate that those devices of three different S (which is 3.8μm, 5.8μm, and 7.8μm, respectively) all failed before it get into the snapback region, where the d is hold at 5μm. As the result shown in Fig. 2, the ESD levels of these three devices are not improved apparently. Similarly, changing the space between active region and the contact of the drain side, which is marked as the parameter d in Fig. 1, has no significant improvement on ESD robustness of LDMOS. The measurement results of LDMOS with different parameter d are shown in Fig. 3, where the S is kept at 3.8μm. According to previous

study, extending the STI space (which is the parameter S in Fig. 1) can increase ESD level of the device when the device snapback successfully under ESD stress. So, the following devices, which are investigated in this work, almost follow the foundry's design rules except for the space of STI at the drain which have been extended to 5.8μm and keep the same value for these devices.

The second device is modified from LDMOS by inserting p+ implantation region in drain active region to create the parasitic SCR. This device is named as embedded SCR LDMOS and shown in Fig. 4. Embedded SCR inside LDMOS is the simplest way to improve ESD level, which provided that the parasitic device can be triggered on before it failed. The third device shown in Fig. 5, which is named as new proposed LDMOS-SCR, is similar to the embedded SCR LDMOS but with additional p+ and n+ implantation regions between gate and drain. There is STI between those additional implantation regions. In the third structure, there is a dummy gate between two p+ regions for reducing the total space and increasing the gain of the parasitic BJT. To make sure that the parasitic pMOS being kept off, the dummy gate is connected to the drain. The new proposed LDMOS-SCR is fully process compatible to high voltage process without additional mask layer or process step. Those devices are drawn with 800μm/1μm (width/length) in the test chip for performance comparison and have been verified in a 0.25-μm 60-V BCD process.

III. Experimental Results

To verify the proposed new structure of LDMOS-SCR, a transmission-line-pulsing (TLP) system is used to measurement the breakdown voltage, trigger voltage (V_{t1}), holding voltage, and the maximum current-handling ability (the secondary breakdown current, I_{t2}) of the fabricated devices. The failure criterion is defined 1-μA leakage current under the bias of maximum 60V supply voltage after each test on the devices.

The TLP measurement results of stand-alone LDMOS and embedded SCR LDMOS are shown in Fig. 6 and Fig. 7, respectively. Both stand-alone LDMOS and embedded SCR structure failed before their snapback, so the current-handling ability of those two devices are weak (I_{t2} ~400mA). There is no obvious ESD improvement as comparing those two figures. Besides, the breakdown voltage of the embedded SCR LDMOS is down to 59V, which is lower than the maximum supply voltage of 60V. Fig. 8 shows the TLP measurement results of the new proposed LDMOS-SCR. The I-V curve indicates that the new proposed LDMOS-SCR structure can be triggered on at 86V and successfully get into the snapback region. Consequently, it has a higher I_{t2} (> 2A) than others. The breakdown voltage of the new proposed LDMOS-SCR is 75V which maintains the same breakdown voltage as that of the stand-alone LDMOS.

The human-body-model (HBM) ESD robustness of the fabricated devices is characterized by the ESD tester. The measurement result of the stand-alone LDMOS is 1.5kV. The embedded SCR structure only passes 1kV during the HBM test. The new proposed LDMOS-SCR can pass more than 2kV level which is the best one among these three devices investigated in this work. All the experimental results are summarized in Table I. The new proposed LDMOS-SCR can have better ESD level.

The SEM pictures of the embedded SCR LDMOS and the new proposed LDMOS-SCR structure after HBM test are shown in Fig. 9 and Fig.10, respectively. In Fig. 9, the damage appears in the middle finger only. Non-uniform silicon melting damage is the sign of filamentation. Conversely, the distribution of failure locations after HBM stress on the new proposed LDMOS-SCR become uniform. Every finger has shown with ESD damage in Fig. 10. The uniform ESD dissipation current causes the increase of the self-protection ability of the new proposed LDMOS-SCR during the ESD test.

IV. Conclusions

The new structure of LDMOS not only increases its I_{t2} level to more than 2A but also improves the HBM level to over 2kV, which can meet the typical ESD specification of commercial IC products. Besides, the new structure of LDMOS keeps the same electrical safe operation area due to the breakdown voltage unchanged. The new proposed LDMOS-SCR structure will be the useful self-protection solution against ESD events in high-voltage applications.

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References

[1] M. Imam, M. Quddus, J. Adams, and Z. Hossain, "Efficacy of charge sharing in reshaping the surface electric field in high-voltage lateral RESURF devices," *IEEE Trans. Electron Devices*, vol. 51, pp. 141-148, 2004.

[2] M. Imam, Z. Hossain, M. Quddus, J. Adams, C. Hoggatt, T. Ishiguro, and R. Nair, "Design and optimization of double-RESURF high-voltage lateral devices for a manufacturable process," *IEEE Trans. Electron Devices,* vol. 50, no. 7, pp. 1697-1700, July 2003.

[3] P. Zhang, Y. Wang, S. Jia, and X. Zhang, "Analysis of LDMOS-SCR ESD protection device for 60V SOI BCD technology," in *Proc. IEEE Int. Conf. of Electron Devices and Solid-State Circuits*, 2010.

[4] T. H. Lai, M. D. Ker, W. J. Chang, T. H. Tang, and K. C. Su, "High-robust ESD protection structure with embedded SCR in high-voltage CMOS process," in *Proc. IEEE Int. Reliability Physics Symposium,* 2008, pp. 627-628.

[5] K. Nakamura, T. Naka, K. Matsushita, T. Matsudai, N. Yasuhara, and A. Nakagawa, "ESD protection structure with novel trigger technique for LDMOS based on BCD process," in *Proc. IEEE Int. Symp. on Power Semiconductor Devices and ICs*, 2009, pp. 227-230.

[6] C. T. Wang and M. D. Ker, "ESD protection design with lateral DMOS transistor in 40-V BCD technology," *IEEE Trans. Electron Devices,* vol. 57, no. 12, pp. 3395-3404, Dec. 2010.

[7] W. Y. Chen and M. D. Ker, "Improving safe operating area of nLDMOS array with embedded silicon controlled rectifier for ESD protection in a 24-V BCD process," *IEEE Trans. Electron Devices,* vol. 58, no. 9, pp. 2944-2951, Sep. 2011.

[8] J. Lee, H. Su, C. Chan, D. Yang, J. Chen, and K. Wu, "The influence of the layout on the ESD performance of HV-LDMOS," in *Proc. IEEE Int. Symp. on Power Semiconductor Devices and ICs*, 2010, pp. 303-306.

[9] S. Chen, Y. Tsai, D. Lee, F. Chen, W. Liu, C. Chung, S. Hsu, J. Shih, A. Liang, and K. Wu, "The influence of NBL layout and LOCOS space on component ESD and system level ESD for HV-LDMOS," in *Proc. IEEE Int. Symp. on Power Semiconductor Devices and ICs*, 2007, pp. 137-176.

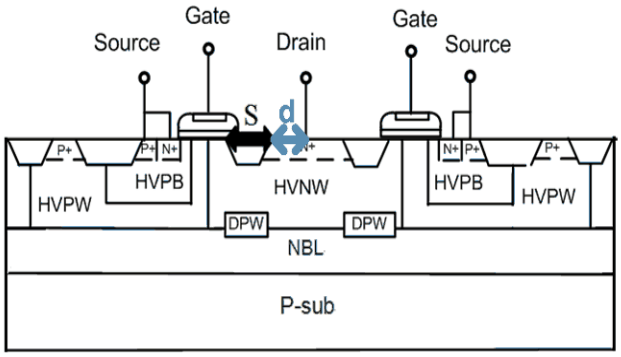

Fig.1. The cross-section view of stand-alone LDMOS device. Parameter S means the space of STI, and the parameter d means the space between contact and diffusion region.

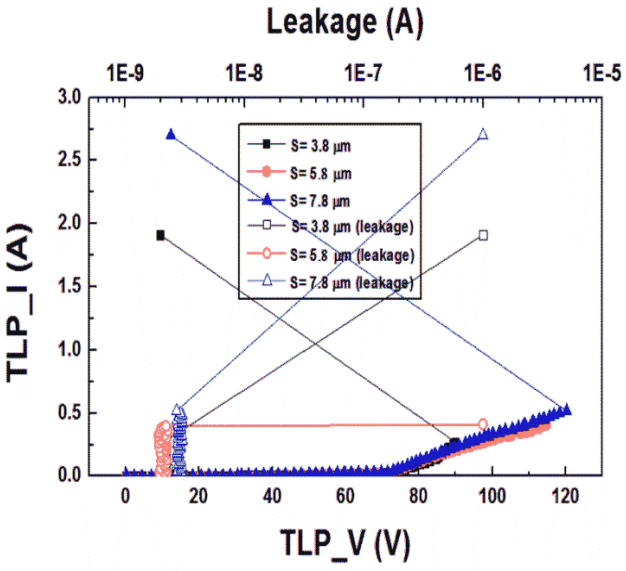

Fig.2. TLP-measurement results of the stand-alone LDMOS with different STI space (the parameter S in Fig. 1), under d=5μm.

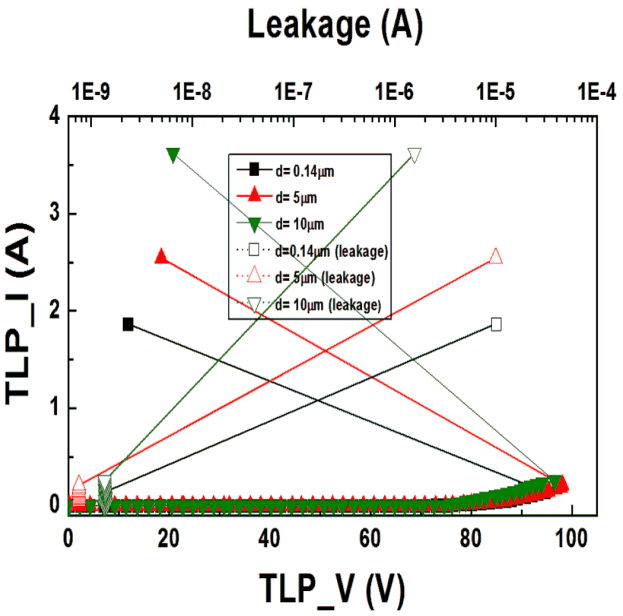

Fig.3. TLP-measurement results of the LDMOS with different space between contact and active region (the parameter d) in the drain side, under S=3.8μm.

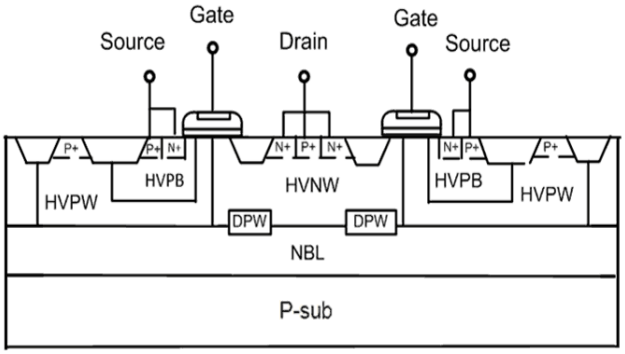

Fig.4. The cross-section view of embedded SCR LDMOS device. The space of STI (S) between gate and drain is kept at 5.8μm.

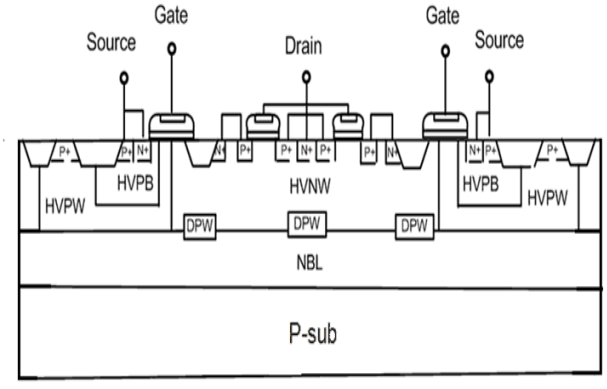

Fig. 5. The cross-section view of new proposed LDMOS-SCR device. The space of STI (S) between gate and drain is kept at 5.8μm.

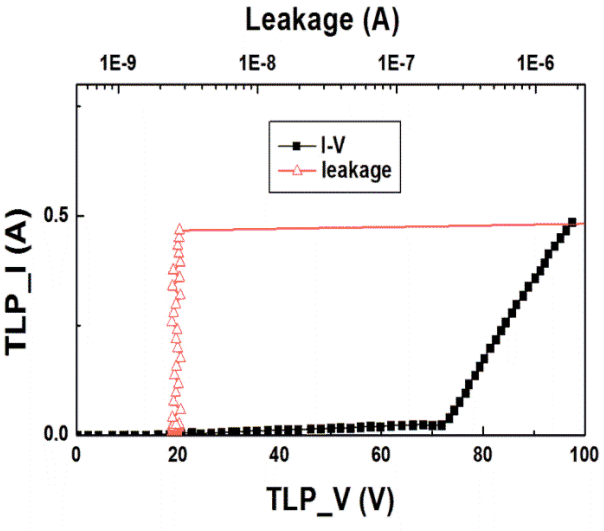

Fig. 6. TLP-measurement results of stand-alone LDMOS.

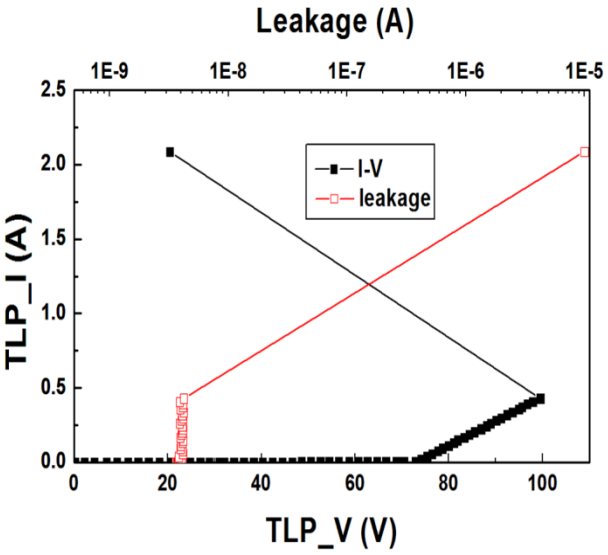

Fig. 7. TLP-measurement results of embedded SCR LDMOS device.

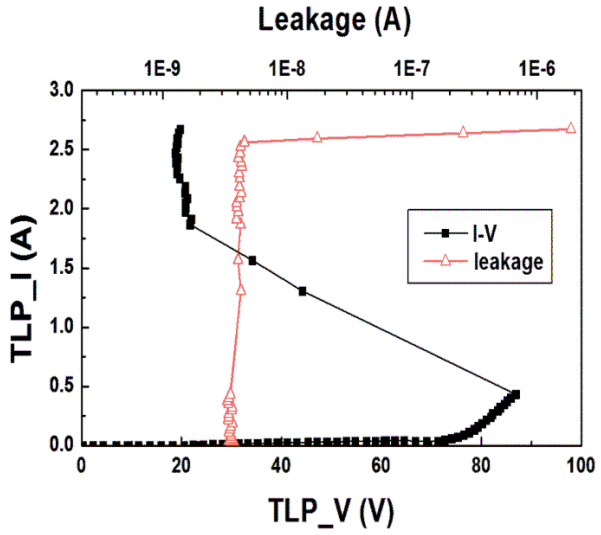

Fig. 8. TLP-measurement results of the new proposed LDMOS-SCR.

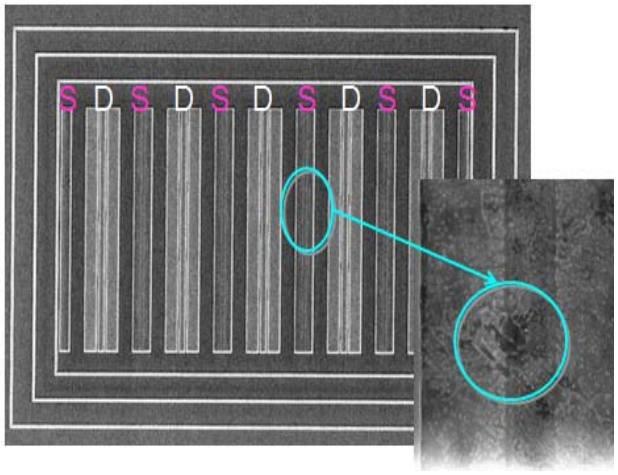

Fig. 9. The SEM image of embedded SCR LDMOS device after 1.5kV HBM test.

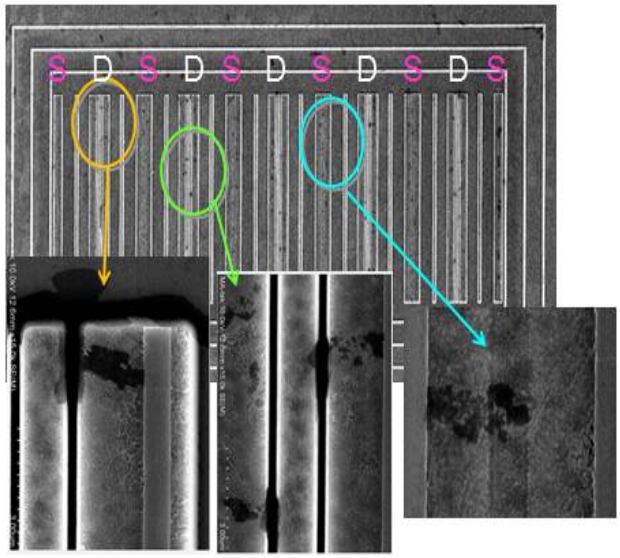

Fig. 10. The SEM image of new proposed LDMOS-SCR after 2.5 kV HBM test.

Table I
SUMMARY OF DEVICE CHARACTERISTICS AND ESD LEVELS AMONG THE FABRICATED THREE HIGH-VOLTAGE DEVICES.

	Stand-Alone LDMOS	Embedded SCR LDMOS	Proposed LDMOS-SCR
Breakdown Voltage	75V	59V	75V
Trigger Voltage	88V	96V	86V
Secondary Breakdown Current (I_{t2})	378mA	430mA	2.5 A
Holding Voltage	N/A	N/A	19V
HBM ESD level	1.5kV	1kV	2kV

∗ W/L=800μm/1μm for all devices in this table.