16.1 A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic SoC for Real-Time Epileptic Seizure Control

Wei-Ming Chen[1], Herming Chiueh[1], Tsan-Jieh Chen[1], Chia-Lun Ho[1], Chi Jeng[1], Shun-Ting Chang[1], Ming-Dou Ker[1], Chun-Yu Lin[1], Ya-Chun Huang[1], Chia-Wei Chou[1], Tsun-Yuan Fan[1], Ming-Seng Cheng[1], Sheng-Fu Liang[2], Tzu-Chieh Chien[2], Sih-Yen Wu[2], Yu-Lin Wang[2], Fu-Zen Shaw[2], Yu-Hsing Huang[2], Chia-Hsiang Yang[1], Jin-Chern Chiou[1], Chih-Wei Chang[1], Lei-Chun Chou[1], Chung-Yu Wu[1]

[1]National Chiao Tung University, Hsinchu, Taiwan,
[2]National Cheng Kung University, Tainan, Taiwan

Epilepsy is one of the most common neurological disorders. Around 1% of the world's population is affected, and nearly 25% of the patients cannot be treated by available therapies. Recently, seizure-triggered feedback electrical stimulation has been proved to effectively suppress pathological brain activities [1], but devices with accurate detection and effective stimulation for real-time seizure control are still unavailable. In this paper, a fully integrated 8-channel closed-loop seizure-control SoC with entropy-and-spectrum-aided seizure detection and adaptive neural stimulation is presented. This chip is powered wirelessly, aiming for implantable devices. The functionality of the fabricated chip is verified in animal tests.

Figure 16.1.1 shows the architecture of the seizure-control SoC, where a signal-acquisition unit (SAQ), a bio-signal processor (BSP), an electrical stimulator, a wireless transceiver, and a wireless power supply are integrated. The SAQ and BSP are used to record and recognize seizures. Once a seizure is detected, the BSP sends a command to activate the adaptive stimulator to suppress the aberrant brain activities. Recorded neural signals are transmitted over the MedRadio band (401 to 406MHz) for system monitoring. Required power is transmitted through inductive coils over the ISM band (13.56MHz). Data transmission is encoded through a reliable cyclic redundancy check (CRC).

The 8-channel acquisition unit consists of auto-reset capacitive-coupled instrumentation amplifiers (AR-CCIA), configurable band-pass filters (BPF), V-to-I power-gating PGAs, a multiplexer, a shared transimpedance amplifier (TIA), and a 10b delta-modulated SAR ADC (DMSAR-ADC), as shown in Fig. 16.1.2. A T-connected pseudo-resistor (TPR) is used to suppress charge accumulation. An auto-reset unit (ARU) senses the drift of output voltage, providing a fast-settling path to reset the impendence of the TPR. The NEF of the AR-CCIA is 1.77. The AFE provides 3-step gains (41, 50, and 61dB) for adaptive signal scaling. By configuring BPF parameters, the high- and low-pass cutoff frequencies can be adjusted from 0.1 to 10Hz and from 0.8 to 7kHz, respectively. The circuit achieves better filtering performance with lower resistance (1TΩ) than [2] for 0.1Hz high-pass cutoff frequency. Power gating is embedded, reducing power consumption by 40%. The 10b DMSAR ADC is composed of a switched-capacitor array, a time-shared comparator, a memory, an adder, and an asynchronous clock generator. Only the voltage difference between two successive samples is resolved to reduce the number of conversion steps, reducing the power/channel by up to 66%. The measured SNDR is 56.12dB at an input frequency of 7kHz.

Figure 16.1.3 shows the architecture of the wireless data transceiver and power-supply system. The transmitter (TX) is composed of a ring-oscillator VCO with OOK modulation. The receiver (RX) has a single-to-differential amplifier (SDA), 4 cascaded fully differential amplifiers (FDA), and a demodulator. A T/R switch is used to increase isolation between TX and RX ports. A current-mode envelope detector is used to recover the amplified signal from the gain stage with data frequency of up to 4MHz. The 4-input demodulator eliminates the offset voltage caused by the previous stage and performs full-wave rectification with a succeeding LPF for envelope recovery. Energy consumption of the TX and the RX are 0.16 and 0.07nJ/b, respectively.

The power-supply system includes a coil pair, which resonate at 13.56MHz, an active rectifier [3], and 3 LDOs. In the active rectifier, a delay comparator compensates the gate delay of the power MOS devices, achieving 84.8% conversion efficiency. A multi-LDO topology is adopted to mitigate the interferences across different power domains. ALDO and RLDO are deployed for analog and reference circuits. DLDO is used for digital and stimulation circuits. Replica-based design and flipped voltage follower (FVF) cells enhance the load regulation and achieve high loop-gain bandwidth. Adaptively biased voltage-controlled current sources (ABVCCS) and voltage-controlled current sources (VCCS) are used to stabilize the voltage under various load conditions. Fast transient recovery is achieved using slew-rate enhancement (SRE) circuits.

Figure 16.1.4 shows the seizure-detection algorithm and signal-processing flow of the BSP [4]. Both signal entropy and frequency spectrum are extracted as epileptic features. They are then fed into a linear least-square (LLS) classifier for seizure classification. In the off-line training stage, continuous neural signals of seizures and non-seizures are recorded for feature extraction. Once the seizure parameters are determined, the parameters are loaded for real-time operation. Operated at 3.2kHz for each channel, the computation of entropy, FFT, and LLS classification is finished within 23.5ms. Through an efficient pipelined architecture, epileptic seizures can be detected within 32 samples (160ms). The processor detects more than 92% of seizures within 0.8s, outperforming the support vector machine (SVD)-based EEG acquisition processor in [5], which achieves 84.4% detection accuracy within 2s.

The stimulator delivers biphasic stimulation currents with adaptive supply voltage, as shown in Fig. 16.1.5. It consists of a pair of high-voltage-tolerant output drivers [6] with H-bridge topology, a pair of current controllers, and a high-voltage generator. With enable signals (V_{ST} and V_{STB}) generated from BSP, the biphasic stimulation current (I_{stim}) is modulated. To adapt to a wide range of load impedances of the electrode-tissue interface, a high-voltage generator is designed to supply a variable voltage (V_{CC}, up to 10V) for output driver. The high-voltage generator consists of a 5-stage charge pump, a comparator, a clock controller, and buffers. The clock controller is used to generate the clock signals (clk and clkb) and to activate the charge pump during the stimulation period. A constant 30μA stimulation current I_{stim} is delivered through a feedback control loop.

The closed-loop neural-prosthetic SoC is tested on Long-Evan rats to verify its functionality. Four rats are subjected to absence seizures. Abnormal neural spike-and-wave episodes are detected and syndromes are suppressed within 0.8s. Figure 16.1.6 shows the recorded intracranial EEG signals with and without stimulation. The seizure syndrome is well detected and suppressed by the stimulation. Figure 16.1.7 shows the chip micrograph and the performance summary of the SoC. The chip occupies 13.47mm^2 in 0.18μm CMOS and it dissipates 2.798mW. A wirelessly powered neural-prosthetic SoC with analog frontend, ADC, bio-signal processor, adaptive stimulator, and wireless transceiver is demonstrated to be a promising solution for treating epilepsy.

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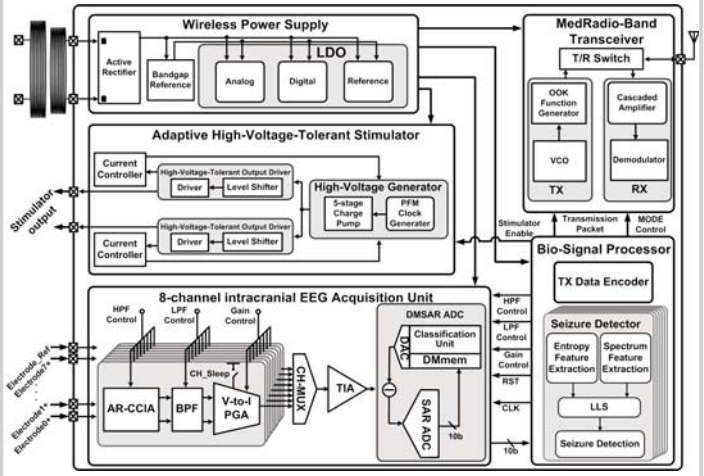


Figure 16.1.1: Architecture of the epileptic seizure-control SoC.

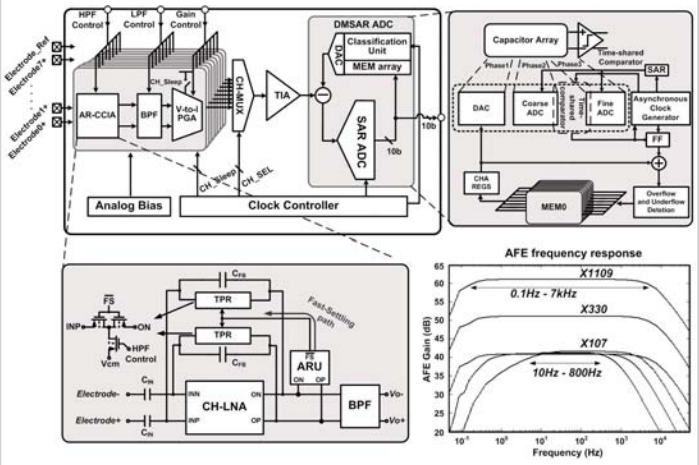


Figure 16.1.2: Configurable neural-signal acquisition unit.

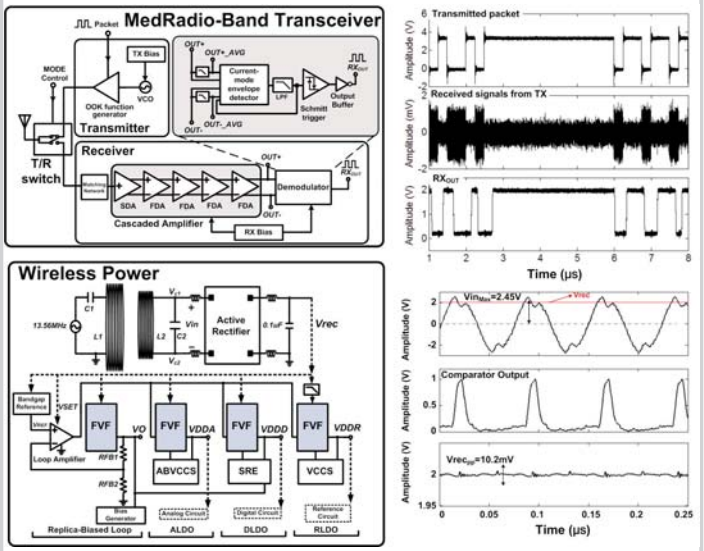


Figure 16.1.3: Wireless transceiver and power-supply system.

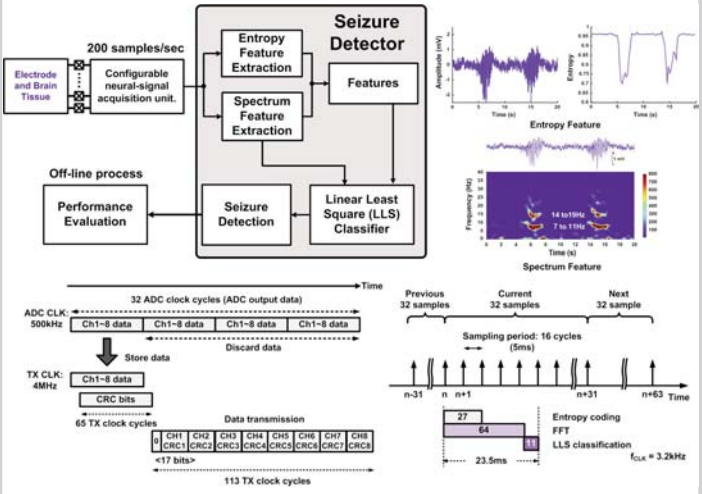


Figure 16.1.4: Algorithm and timing diagram of the seizure detector.

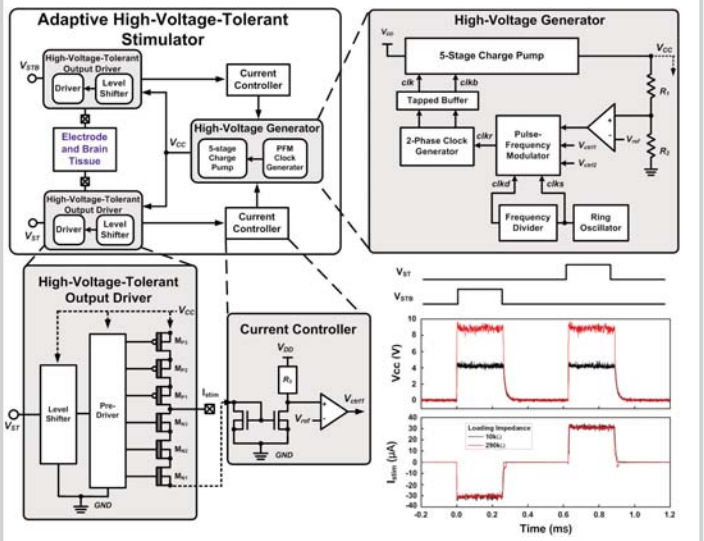


Figure 16.1.5: Adaptive high-voltage-tolerant stimulator.

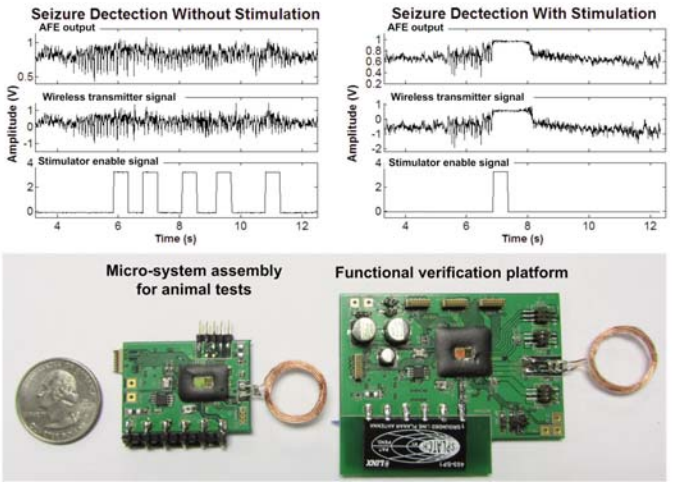
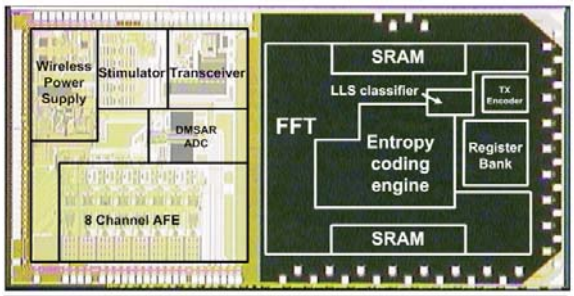


Figure 16.1.6: Seizure detection and closed-loop conditional stimulations with prototype PCBs.



Process			TSMC 0.18μm 1P6M CMOS		
Area			2.76mm x 4.88mm		
AFE	Gain	41-61dB	Rectifier	Power efficiency	84.82%
	High-pass f_{3dB}	0.1-10Hz	ALDO	Current efficiency	95.93%
	Low-pass f_{3dB}	0.8k-7kHz		Load regulation	0.21V/A
	NEF	1.77 (ARCCIA)	BSP	Accuracy	92%
DMSAR ADC	ENOB	9.57b @ 500kS/s		Latency	0.8s
	INL/DNL	0.32/0.08 LSB		Energy per detection	77.91μJ
Transceiver	Energy per bit	0.16nJ/bit (TX)	Stimulator	Stimulator	Bipolar
		0.07nJ/bit (RX)		Stimulation Current	30μA

Figure 16.1.7: Chip micrograph and summary.

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