

ESD Protection Design for Radio-Frequency Integrated Circuits in Nanoscale CMOS Technology

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Abstract—Nanoscale CMOS technologies have been used to implement the radio-frequency integrated circuits. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of IC products. Therefore, on-chip ESD protection designs must be added at all input/output pads in CMOS chip. To minimize the impacts from ESD protection on circuit performances, ESD protection at input/output pads must be carefully designed. In this work, a new proposed ESD protection design has been realized in a nanoscale CMOS process. Experimental results of the test circuits have been successfully verified, including RF performances, I-V characteristics, and ESD robustness.

I. INTRODUCTION

Nanoscale CMOS technologies have been used to implement the radio-frequency (RF) integrated circuits; however, the device realized in CMOS technology is susceptible to an electrostatic discharge (ESD) event which may damage the IC products [1]. Therefore, on-chip ESD protection circuits must be added at the RF circuits that may be stressed by ESD, including the input pads of low-noise amplifier (LNA) and the output pads of power amplifier (PA) [2], [3]. A typical specification for a gigahertz RF circuit on human-body-model (HBM) / machine-model (MM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV / 200 V and 200 fF, respectively [4]-[6]. To mitigate the performance degradation caused by ESD protection, some design techniques had been developed to reduce the parasitic capacitance of ESD protection devices. The ESD protection circuit with reduced parasitic capacitance can be easily combined or co-designed with RF circuits [7].

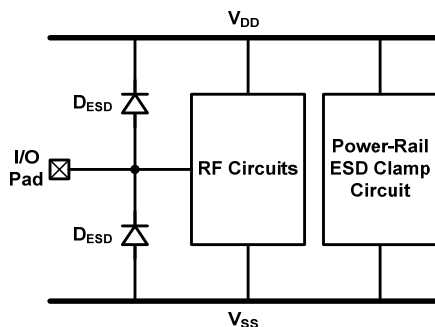


Fig. 1. Conventional double-diode ESD protection scheme for RF circuits in nanoscale CMOS technologies.

The conventional double-diode ESD protection scheme has been generally used for gigahertz RF circuits, since it can meet the typical specification on ESD robustness and the maximum parasitic capacitance. Fig. 1 shows the double-diode ESD protection scheme with diodes (D_{ESD}) at I/O pad and the power-rail ESD clamp circuit between V_{DD} and V_{SS} [8]. Under positive-to- V_{DD} (PD) or negative-to- V_{SS} (NS) ESD stresses, ESD current is discharged through the forward-biased D_{ESD} . During positive-to- V_{SS} (PS) ESD stress, ESD current is discharged from the I/O pad through the forward-biased D_{ESD} to V_{DD} , and discharged to the grounded V_{SS} through the power-rail ESD clamp circuit. Similarly, during negative-to- V_{DD} (ND) ESD stress, ESD current is discharged from the V_{DD} through the power-rail ESD clamp circuit and the forward-biased D_{ESD} to the I/O pad.

For some RF circuits, such as power amplifier, the signal swing at output pad may be as high as two to three times the supply voltage (V_{DD}). The conventional double-diode ESD protection design limits the maximum signal swing at RF output. Therefore, the PA needs large-swing-tolerant ESD protection circuit at its output pad. In this work, a novel large-swing-tolerant ESD protection circuit is proposed for effective ESD protection on gigahertz PA in nanoscale CMOS technology. This design can achieve low parasitic capacitance, large swing tolerance, high ESD robustness, and good latchup immunity.

II. PROPOSED DESIGN AND REALIZATION

The proposed ESD protection circuit utilizes diode and silicon-controlled rectifier (SCR) [9] as main ESD-current-discharging paths. The equivalent circuit of the SCR consists of the cross-coupled PNP BJT (Q_{PNP}) and NPN BJT (Q_{NPN}), as shown in Fig. 2. As ESD stresses from anode (RF_{OUT}) to cathode (V_{SS}) of the SCR are applied, the positive-feedback regenerative mechanism of PNP and NPN BJTs results in the SCR device becoming highly conductive to make the SCR very robust against ESD stresses. To enhance the turn-on speed of SCR, the trigger signal should be sent into the base terminal of the NPN BJT of SCR device. The proposed ESD protection circuit is shown in Fig. 3, which consists of a P-type diode (D_P), a high-voltage node (V_H), an N-type diode (D_N), an SCR, a trigger diode (D_T), and a trigger resistor (R_T). The D_N and SCR provide the ESD paths between RF_{OUT} and V_{SS} . Once ESD stresses from anode to cathode of

the SCR, the D_P and D_T will turn on first, and then the R_T will generate a high voltage to trigger the SCR. The power-rail ESD clamp circuit is used to provide the ESD paths between V_{DD} and V_{SS} .

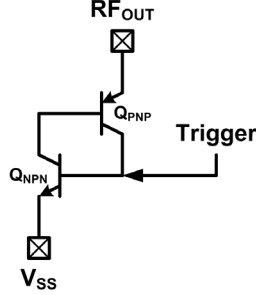


Fig. 2. Equivalent circuit of SCR device.

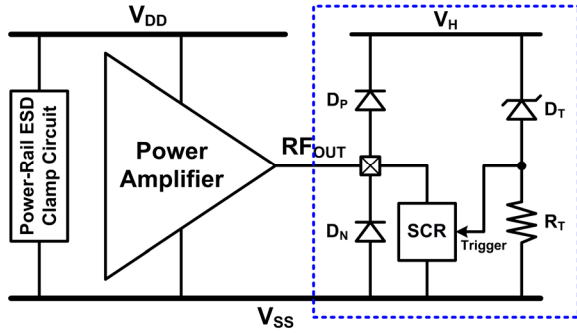


Fig. 3. Proposed ESD protection design for RF power amplifier.

While positive ESD charges stress to RF_{OUT} with grounded V_{SS} (PS mode), the trigger signal is sent through the forward-biased D_P , reverse-breakdown D_T , and R_T to enhance the turn-on efficiency of SCR, and the ESD currents can be discharged through the SCR. As positive ESD charges stress to RF_{OUT} with grounded V_{DD} (PD mode), the ESD currents can be discharged through the SCR to the floating V_{SS} , and then through the power-rail ESD clamp circuit to V_{DD} . While negative ESD charges stress to RF_{OUT} with grounded V_{SS} (NS mode), the ESD currents can be discharged through the forward-biased D_N . As negative ESD charges stress to RF_{OUT} with grounded V_{DD} (ND mode), the ESD currents can be discharged through the forward-biased D_N to the floating V_{SS} , and then through the power-rail ESD clamp circuit to V_{DD} .

Under normal RF circuit operating conditions, the V_H node is charged and kept at a high voltage by the output swing of the power amplifier; therefore, the D_P is kept off. Besides, the D_N and SCR are also kept off to prevent from the signal loss.

To realize the proposed design in silicon chip, a cross-sectional view of test circuit is shown in Fig. 4. All the components used in the proposed design are embedded in this structure. The D_P and D_N are realized by P+/N-well and N+/P-well junctions, respectively. The SCR path consists of P+, N-well, P-well, and N+. The D_T is realized by N+/P-ESD junction, where the P-ESD denotes the p-type ESD implantation [10]. The R_T is realized by the P-well resistor.

The dimensions of the test circuits are labeled as S_1 , S_2 , S_3 , S_4 , S_5 , S_6 , and S_7 . The P+/N-well and N+/P-well junctions in the main ESD-current-discharging paths of D_N and SCR

should be wide enough, so the S_1 is selected to $0.8 \mu m$. The turn on voltage of SCR is mainly determined by the breakdown voltage of D_T . The test circuits with different dimensions are split to investigate the characteristics of the proposed ESD protection circuit, including the parasitic capacitance, ESD robustness, turn on voltage, and holding voltage. In the test circuit A, the dimensions are arranged as $S_1=0.8 \mu m$, $S_2=0.3 \mu m$, $S_3=0.3 \mu m$, $S_4=0.2 \mu m$, $S_5=0.3 \mu m$, $S_6=0.4 \mu m$, and $S_7=1 \mu m$. In the test circuits B, C, D, E, F, and G, the dimensions are changed to $S_2=1 \mu m$, $S_3=1 \mu m$, $S_4=1 \mu m$, $S_5=1 \mu m$, $S_6=1 \mu m$, and $S_7=0.5 \mu m$, respectively. The device width (W) of the test circuits are kept at $40 \mu m$, which is estimated to pass 2-kV HBM and 200-V MM ESD tests. All these dimensions of test circuits are listed in Table I.

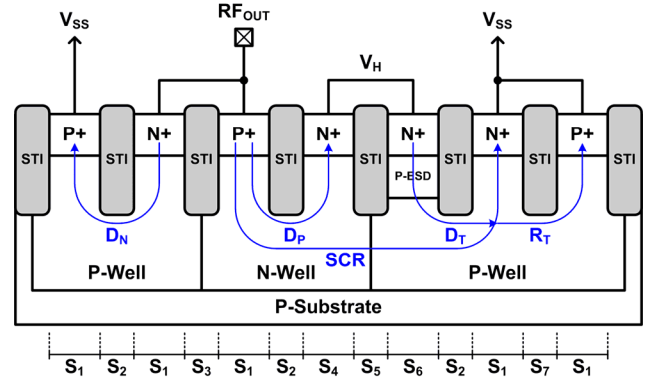


Fig. 4. Cross-sectional view of test circuit.

I. EXPERIMENTAL RESULTS

The test circuits have been fabricated in a 65-nm salicided CMOS process. Fig. 5 shows the chip photograph of one test circuit. The test circuits are implemented with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port RF measurement. The parasitic effects of the G-S-G pads have been removed by using the de-embedding technique. Fig. 6 shows the parasitic capacitance of the test circuits from 0 to 20 GHz, which are extracted from the two-port S-parameters. The intrinsic parasitic capacitances of the test circuits are about 75 fF at 2.4 GHz.

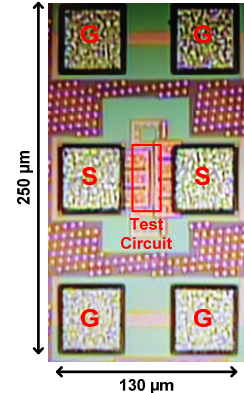


Fig. 5. Chip photograph of one test circuit.

The HBM and MM ESD robustness of the test circuits are evaluated by the ESD tester. The failure criterion is defined as

TABLE I
DESIGN PARAMETERS AND MEASUREMENT RESULTS OF TEST CIRCUITS

| | | Test Circuits | | | | | | |
|-------------|---------------------------------------|---------------|------|------|------|------|------|------|
| | | A | B | C | D | E | F | G |
| Design | S_1 (μm) | 0.8 | | | | | | |
| | S_2 (μm) | 0.3 | 1 | 0.3 | | | | |
| | S_3 (μm) | 0.3 | | 1 | 0.3 | | | |
| | S_4 (μm) | 0.2 | | | 1 | 0.2 | | |
| | S_5 (μm) | 0.3 | | | | 1 | 0.3 | |
| | S_6 (μm) | 0.4 | | | | | 1 | 0.4 |
| | S_7 (μm) | 1 | | | | | | 0.5 |
| | W (μm) | 40 | | | | | | |
| Measurement | Parasitic Capacitance at 2.4 GHz (fF) | 75.7 | 74.6 | 73.4 | 75.3 | 74.8 | 77.6 | 75.3 |
| | HBM ESD Robustness (kV) | 3.25 | 3.25 | 3.25 | 3 | 3.25 | 3 | 3 |
| | MM ESD Robustness (V) | 200 | 200 | 225 | 175 | 200 | 200 | 175 |
| | TLP V_{t1} (V) | 8.04 | 8.65 | 8.08 | 8.25 | 7.99 | 7.97 | 8.18 |
| | TLP I_{t2} (A) | 1.76 | 1.82 | 1.76 | 1.66 | 1.73 | 1.69 | 1.64 |
| | DC V_{hold} (V) | 2.52 | 3.11 | 2.37 | 3.61 | 3.1 | 3.07 | 2.79 |

the I-V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. In other words, the leakage current under V_{DD} bias (2.5 V, in this work) will not increase over 30 % if the test circuit is not failed after ESD stresses. The test circuits A, B, C, D, E, F, and G have about 3-kV HBM and about 200-V MM ESD robustness.

under dc measurement are lower than those under TLP measurement due to the self-heating effect. The test circuits B, D, E, F, and G exhibit dc V_{hold} larger than V_{DD} (2.5 V) with at least 10% margin, which are very safe from latchup event. All these measured data are summarized in Table I.

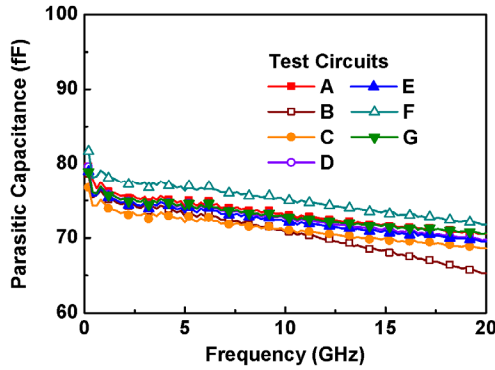


Fig. 6. Measured parasitic capacitances of test circuits.

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the ESD protection circuits, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used. The TLP-measured I-V characteristics are shown in Fig. 7. The trigger voltages (V_{t1}) of the test circuits are about 8 V, which means the ESD protection circuit can sustain up to 8-V signal swing. The secondary breakdown current (I_{t2}) of ESD protection circuit, which indicated the current-handling ability, can also be obtained from the TLP-measured I-V curve. All test circuits can achieve the I_{t2} of about 1.7-A.

The dc I-V curves of the test circuits are shown in Fig. 8. The holding voltages (V_{hold}) of the ESD protection circuits

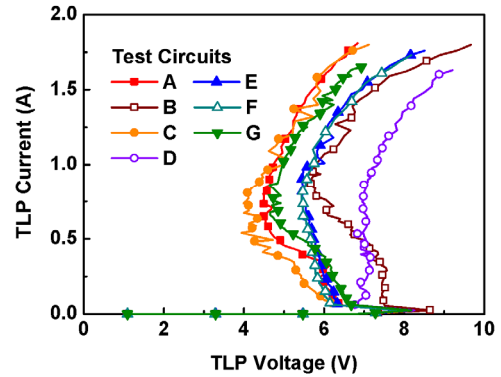


Fig. 7. TLP-measured I-V curves of test circuits.

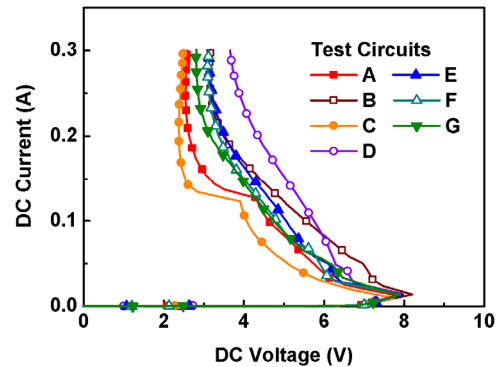


Fig. 8. DC I-V curves of test circuits.

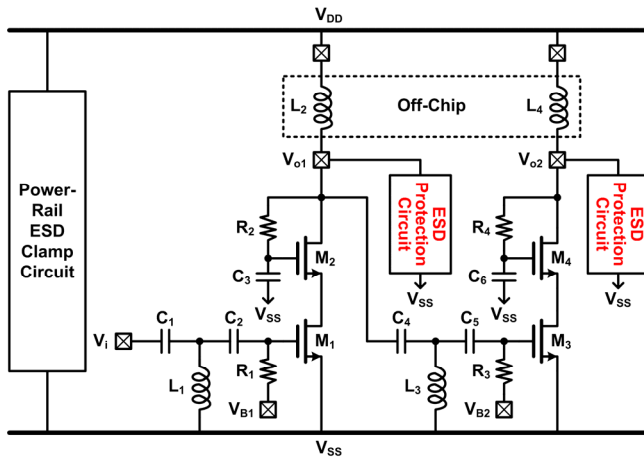


Fig. 9. Power amplifier with ESD protection design.

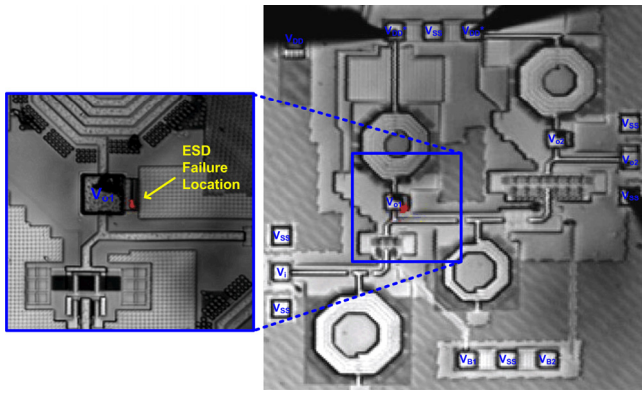


Fig. 10. EMMI photograph to show ESD failure location.

II. ESD PROTECTION FOR PA USING PROPOSED DESIGN

According to the experimental results, most of the test circuits achieve the targets of 2-kV HBM / 200-V MM ESD robustness and 8-V signal swing tolerance with only ~ 75 -fF parasitic capacitance. Among the test circuits, the test circuit E with 74.8-fF parasitic capacitance, 3.25-kV HBM / 200-V MM ESD robustness, 7.99-V TLP V_{tl} , 1.73-A TLP I_{t2} , and 3.1-V dc V_{hold} is much suitable for ESD protection on the PA.

The proposed ESD protection circuit has been further applied to the PA, as shown in Fig. 9. The PA is designed to operate at 2.4 GHz with V_{DD} supply of 2.5 V. To sustain large signal swing, the PA utilizes the self-biased cascode topology. The PA with and without ESD protection circuits have been fabricated in 65-nm CMOS process.

The RF characteristics are measured on wafer through G-S-G microwave probes. The input and output of PA were matched to 50 Ω . Each PA circuit operates with the 2.5-V V_{DD} supply and draws a total current of 420 mA. The used bias voltages V_{B1} and V_{B2} are all 0.9 V. The small-signal gains are about 23 dB for two PAs. The input return losses for both PAs are about 20 dB. The maximum output power of both PAs are about 22 dBm with power gain of 21 dB and PAE of 28%. The proposed ESD protection circuit does not degrade the RF performances of the PA.

The ESD-protected PA after 4-kV HBM ESD test has failed. Fig. 10 shows the emission microscope (EMMI)

analysis of the PA with new proposed ESD protection circuits after 4-kV HBM ESD tests, where failure location is found in the ESD protection circuit beside V_{o1} pad. The proposed ESD protection circuit has been verified to protect the PA from ESD damage with 3-kV HBM ESD robustness.

III. CONCLUSION

The new ESD protection design with low parasitic capacitance, large swing tolerance, high ESD robustness, and good latchup immunity has been developed for the RF circuits in nanoscale CMOS technologies. The test circuits have been designed, realized, fabricated, and characterized in a 65-nm CMOS process. The proposed ESD protection design provides 3-kV HBM ESD robustness without degrading the RF performances. The on-chip ESD protection designs for RF circuits will continuously be an important design task in nanoscale CMOS technologies.

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