

ESD and EOS Impacts during Module Assembly Processes for Display Panels

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Abstract

In the manufacturing process of the display module assembly, from the integration of PCB and LCD glass to each module to be assembled, there will be a lot of transferred moving and contacted behavior by equipment or personnel, inevitably. Therefore, the ESD and EOS phenomenon occurring in those production processes will impact the reliability of finished or semi-finished products owing to the damage of ESD/EOS sensitive semiconductor elements. The failure processes and root causes have been addressed to improve the production yield of LCM for display panels.

1. Introduction

In the liquid crystal display (LCD) module production processes, so called as LCM(Liquid Crystal Module) processes, from the LCD glass material feeding to start, followed by the preparation of the inner/outer load bonding (ILB/OLB) jobs, the driver integrated circuits (IC) and the printed circuit board (PCB) will be combined with LCD glass. The driver IC was usually used as the form of TCP (Tape Carrier Package), COF (Chip On Film), or COG (Chip On Glass) with FPC (Flexible Printed Circuit) to connect with LCD glass and PCB, which included data-control board (X-Board) and scan-control board (Y-Board).

The bonding technology with welding operation of TCP, COF, or FPC can solder the driver IC and PCB to the LCD glass through the anisotropic conductive film (ACF) adhesive lamination. The completed process with PCB and integrated LCD glass by film, so called as PCBI, forms as the bare LCD panel. To check the function of bare LCD panel, functional probe card with toggle pins was sometimes used to probe the test holes of PCB, so called as PCBI-Check.

After the PCBI process, most of the followed assembly procedures are manual operations and finished in lower-class level clean room. In this stage, the LCD panel module after PCBI will be integrated with the backlight (BL) module. To avoid foreign particles to enter the module gap between panel and BL module, the bare LCD panel was lighted to check the particles before the assembly process. An extra BL box, which was designed by LCM factory, will be used to check the defects or particles of lit bare LCD panel with or without tearing polarizer protective film. This kind of check was mostly called as A-Check. Most of PCBI-Check and A-check were sometimes merged together to reduce the process schedule. In A-Check station, two protection films of polarizer on the two sides of bare LCD panel will be teared off to assemble with BL module. And then, one or more metal frame of display will be screwed with LCD panel and BL module. Some extra control boards of display were also assembled at the same process. The function test, called as B-Check, will be done again after module assembly.

Finally, the assembly module aging to screen the product reliability with some potential risk should be completed. Followed

C-Check will be done to check any quality issues after aging. Many ESD and EOS events in LCM processes always cause lower production yield[1], [2].

2. The Potential ESD and EOS Risks

During most ILB process, the main materials of driver IC with FPC or COF package of tape reel were fed into cutting machine and bonded to LCD glass material. While, the brush, which was used to clean particles on film as shown in Figure 1, rubs the TCP/COF films of driver IC and induce serious electrostatic discharge (ESD) during friction or when the cutting machine will slice the isolated driver IC.

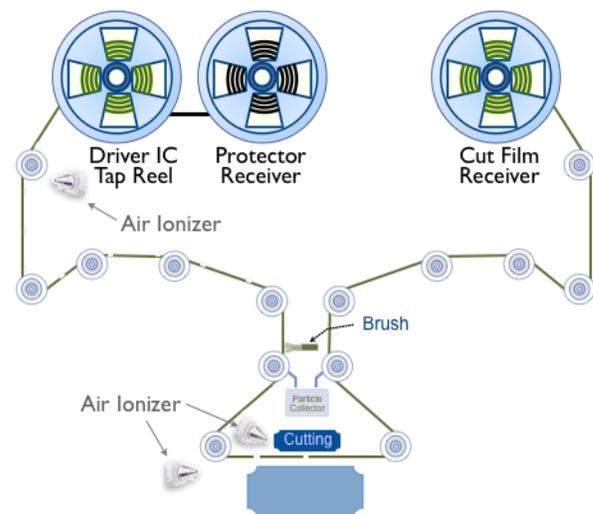


Figure 1. TCP/COF feeder with brush to clean particle for ILB process.

Another ESD problem occurred in that the automation equipment transmission and nip PCB operation in PCBI process. These friction will produce a lot of instantaneous electrostatic charges. When the metal holders nip to some test holes of PCB shown in Figure 2, the stored intrinsic charges of LCD glass and driver IC, of especial occurrence on X-Board, will re-distribute and quickly discharge. This kind of discharge model on the IC is similar to a so-called charged device model (CDM) ESD [3]-[6], and the similar discharge on PCB could also be called as board level charged device model (BLCDM) ESD [7].

In the previous process, BLCDM ESD tolerance should not only pay attention to, but also pay attention to the equal-potential in work bench. Air ionizer has been widely used to reduce environment electrostatic charge and build the equal-potential work environment.

After the PCBI process, the bare LCD panel will be put on one backlight box with insulator or metal materials to do the PCBI or A-Check testing. Some ESD and EOS phenomena inevitably occur owing to the different potential between LCD panel and backlight box during testing. And therefore need to avoid the PCB test hole or backside of driver IC is directly contacted with the metal or insulator backlight box, as shown in Figure 3. Some electrostatic dissipative bumps should be added to avoid this issue.



Figure 2. Relation of PCB holder and test holes of PCB during PCBI process.

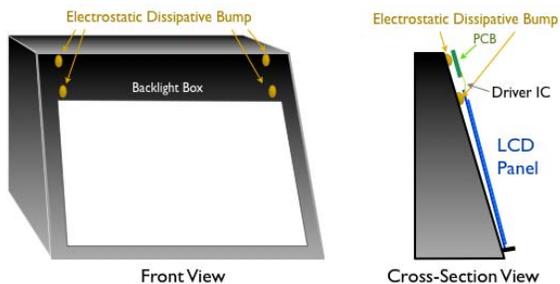


Figure 3. Backlight box with electrostatic dissipative bumps design for A-Check after PCBI process.

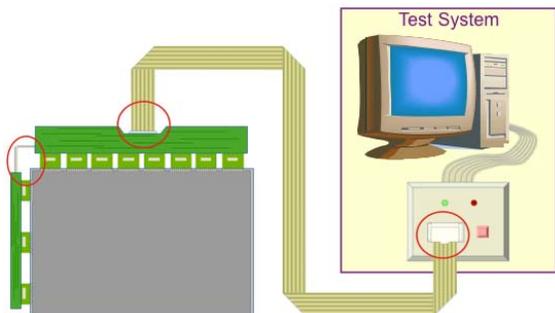


Figure 4. The illustration of testing environment.

While, during checking sequences and aging status, some EOS impacts are always induced by the testing equipment such as switch controller shown in Figure 4, universal connector shown in Figure 5, ground connection, and etc. The switch with on-off function of the test equipment should be design to avoid the hot-plug events. Those universal connectors, in Figure 4, have the usage life-time. Figure 5 shown one degraded case of universal connectors. Most EOS stressed components were the timing-controller (T-con) IC. The auditor of LCM process should define the used times of the universal connector, and operator should check them on a regular time schedule.

Before the bare LCD panel is assembled to the BL module, the polarizer protective films on both sides of the LCD glass must be removed firstly. During this process, as several manual operations in the tear film is particularly important, serious ESD failures were often found in A-Check or B-Check. A lot of tearing methodologies were studied such as speed, vertical direction, and horizontal direction, shown in Figure 6. While, no certain rules could be followed, owing to different characteristics of different

designed LCD-PCB modules. Another distinct ESD impact is due to the connected position and material of grounded wire during tearing process.

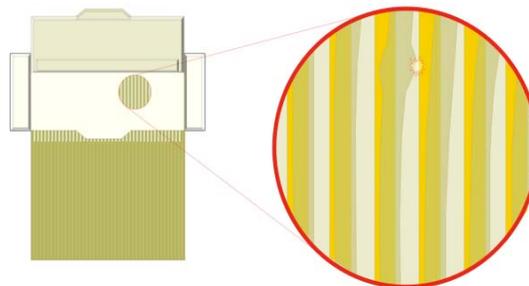


Figure 5. The degradation of universal connector induced pin-shortened EOS event.

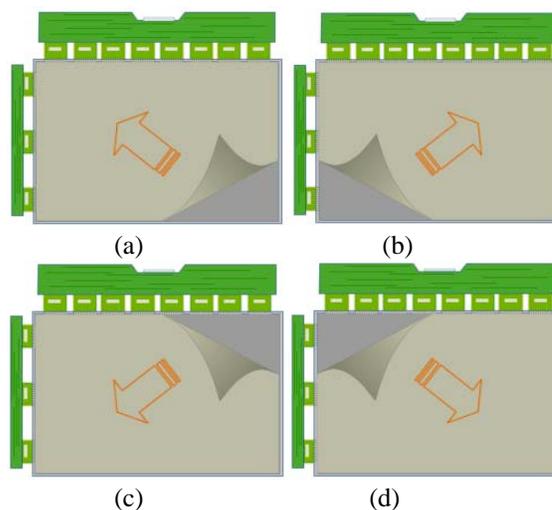


Figure 6. Tearing polarizer protective films with different horizontal directions.

Experientially, most ESD events of LCM process happened to the assembly process to combine bare LCD panel with BL, as shown in Figure 7. In Figure 7(a), the backside or test hole of COF driver IC with face-down design was sometime found to touch with the metal frame of BL during assembly. In Figure 7(b), the backside of TCP driver IC with face-up design was sometime touched by the external metal frame. Even in the COG driver IC design, the backside of driver IC and the test hole of FPC was sometime found to touch with BL frame and external metal frame, individually, as shown in Figure 7(c) and 7(d). In the process, many kinds of failure modes were found on the driver ICs or the cells in LCD glass. One weak line issue, which is the damage of glass gate control line (g-line), was normally found in those ESD events, but not the driver IC failure.

After the combination of bare LCD panel, control module, and BL module, the assembly one LCD set is finished. Some potential reliability problem, included in the previously mentioned component storage charge induced ESD events, with tiny destruction will be enhanced during or after the aging process, but was not found in B-Check. After the aging process, the LCD set were moved out from aging furnace room to do C-Check. From the aging temperature to room temperature, the storage charges will re-distribute among each components of the LCD set. It will

once again suffer these ESD and EOS problems, and thus be eliminated.

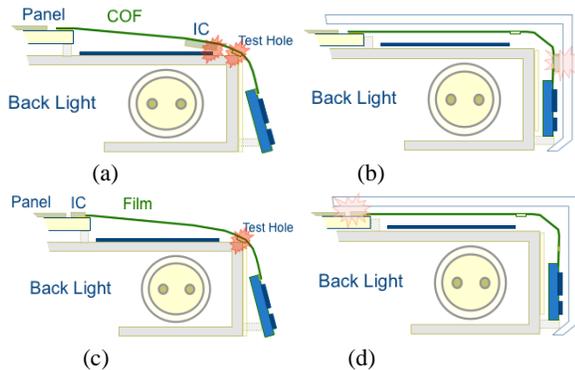


Figure 7. Four different ESD events can be found during panel assembly.

3. Failure Analysis and Experiment Design

To understand what ESD events happen in LCM process, the structure of LCD and the relation circuits among PCB, driver ICs, and LCD cell are shown in Figure 8 and Figure 9, individually. Owing to those driver ICs with full chip ESD protection design [8], those protection circuits among powers and I/O pins of all ICs will contribute a complex network in the LCD panel system as shown in Figure 9. The gate driver IC of Y-Board will control the storage charge in the LCD cell capacitance, but the gate signal was not always under open status to discharge the storage charges from source driver output line of X-Board.

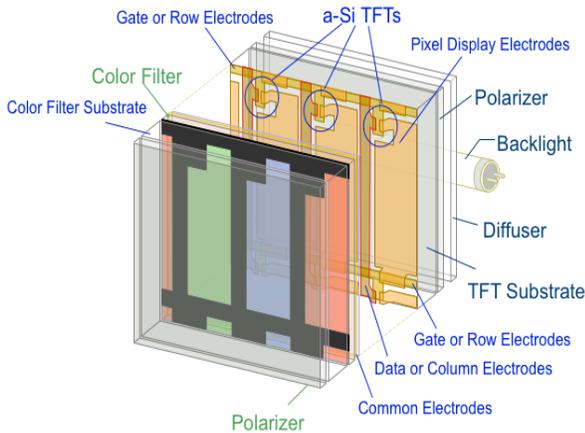


Figure 8. TFT LCD structure with RGB three cells.

To verify the ESD path and energy during tearing process, a tearing-film experiment, which was designed by connecting the ground of PCB to ground by a wire and using Tek-CT1 current probe with 500MHz oscillator, can actually calculate the ESD energy as shown in Figure 10. A 20-A pick-current could be found but not always happen in this repeated experiments. This imply the hundred or thousand ppm (piece per million set) failure ratio during this process.

During testing process, connector degradation induced EOS event will be most easily found in the IO pins of T-con IC. The physical failure analysis (PFA) was shown in Figure 11. It could clearly shown that the connected metal of IO was melted with

power or ground metal traces. Almost, we can trace feedback to certain testing station and find the degraded universal connector when we found the similar PFA photos.

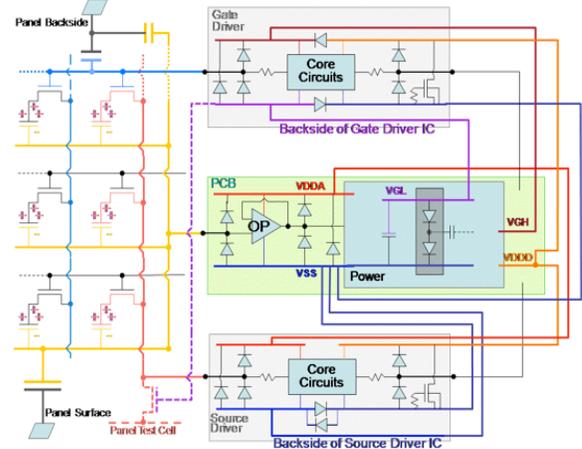


Figure 9. The relationship schematic circuits among PCB, driver ICs, and LCD cell.

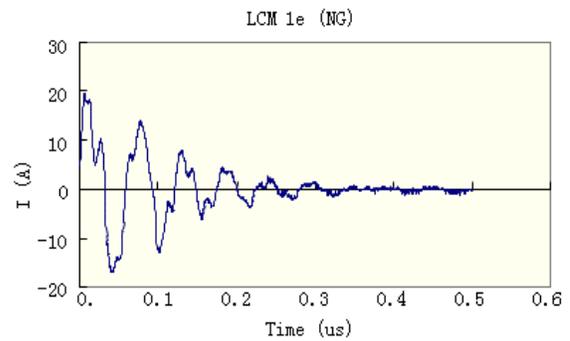


Figure 10. Measured current waveform of grounded PCB during polarizer protective films removed.

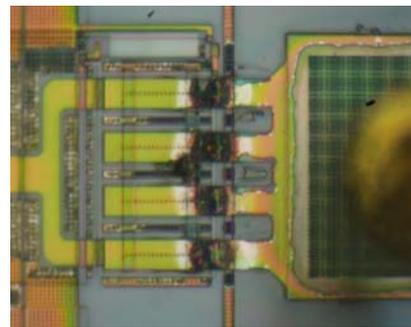


Figure 11. Failure analysis picture for the T-con input pin with EOS stress.

Why the ESD or EOS events will impact on the backside of driver IC or test hole of film? To verify the supposition, the system ESD gun was used to directly stress on those points of driver IC with power-on LCD panel as shown in Figure 12. The ESD gun was used to stress on the backside edge of drive IC die in 12(a), and on the test hole of film in 12(b). We could find the similar PFA results for the LCM failure return samples and

experimental samples. The CDM-like ESD failure, shown in Figure 13(a), could be found in the edge device of driver IC due to the backside ESD stress as shown in Figure 12(a). The output burn PFA result in Figure 13(b) could be found due to ESD stress on the test hole as shown in Figure 12(b).

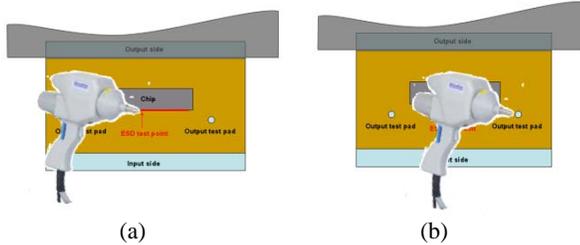


Figure 12. ESD stress experiment to verify the ESD impact on (a) the backside of driver IC, and on (b) the test hole of film.

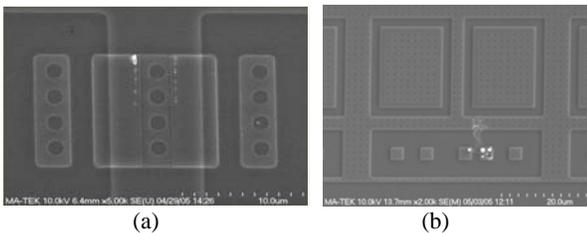


Figure 13. PFA samples of driver IC after the ESD stresses on (a) the backside edge of driver IC and (b) the test hole of film.

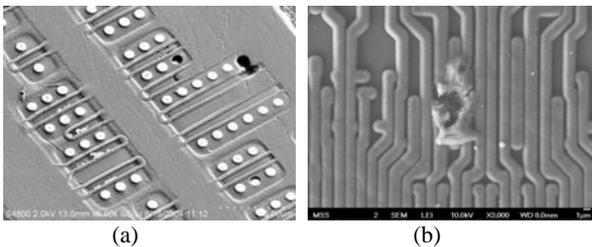


Figure 14. ESD-like and EOS-like events were found in the internal circuits of driver IC.

While, the accumulation charges were not only storage in the panel cell, but also in the driver ICs. The unstable energy potential among LCD cell, driver IC, PCB, and assembly environment will

induce the potential EOS events during testing operation. Some internal circuits with ESD-like or EOS-like damages could be found in the PFA pictures, as shown in Figure 14, of those samples from LCM failure return.

4. Conclusion

A lot of LCM processes with ESD and EOS potential risks have been studied. The backside of driver IC, test holes on film or PCB, and universal connectors are major intermediaries between LCD components and environment ground. To deal with the highest guiding principle of ESD prevention, the target is to keep the various objects in the working environment at the same potential level. Safe discharge with lower current paths are designed among potential ground connected points.

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6. References

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