DESIGN OF 2×V_{DD} LOGIC GATES WITH ONLY 1×V_{DD} DEVICES IN NANOSCALE CMOS TECHNOLOGY

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ABSTRACT

The novel 2xV_{DD} NOT, NAND, and NOR logic gates have been designed and implemented in a nanoscale CMOS process with only 1xV_{DD} devices. With the proposed dynamic source bias technique, the logic gates can be designed to have 2xV_{DD} tolerant capability. Thus, the new 2xV_{DD} logic gates can be operated under 2xV_{DD} voltage environment without suffering the gate-oxide reliability issue.

I. INTRODUCTION

In CMOS technology, a single type of MOSFET device can be only operated within a regular V_{DD} voltage region to meet reliability specification. When the operation voltage exceeds V_{DD}, the device will suffer the gate-oxide overstress issues [1], [2]. However, by using circuit design technique with good arrangement of device combination, the circuits can be operated in the higher supply voltage. In the interface circuits those communicate with other chips of different operating voltages, some I/O interface circuits have been successfully developed with high voltage tolerant capability by using only 1xV_{DD} (thin-oxide) devices [3]-[5].

In CMOS digital circuit applications, the basic circuit units are the complementary logic gates. In this work, the logic gates are developed to be safely operated under 2xV_{DD} voltage signal by using only 1xV_{DD} (thin-oxide) devices.

II. DESIGN OF 2xV_{DD} LOGIC GATES

Figs. 1(a) and 1(b) show the design concepts of the dynamic source bias technique when the logic output (OUT) driving to logic high and logic low. With the M_P and M_N gate voltage biased at V_{DD}, the M_P and M_N can be turned on or turned off by changing device's source voltage. For transmitting a logic high signal (0V-2xV_{DD}) as shown in Fig. 1(a), by applying a 0V-V_{DD} signal at M_N's source and a V_{DD}-2xV_{DD} signal at M_P's source, the OUT can successfully transmit a digital signal of 0V-2xV_{DD}. On the other hand, for transmitting a logic low signal (2xV_{DD}-0V) as shown in Fig. 1(b), the V_{DD}-0V and 2xV_{DD}-V_{DD} signals are needed for source terminals of M_N and M_P, respectively. Therefore, with such source voltage bias arrangements, the logic gates implemented by only 1xV_{DD} devices can be successfully operated under 2xV_{DD} voltage without suffering the aforementioned reliability issues.

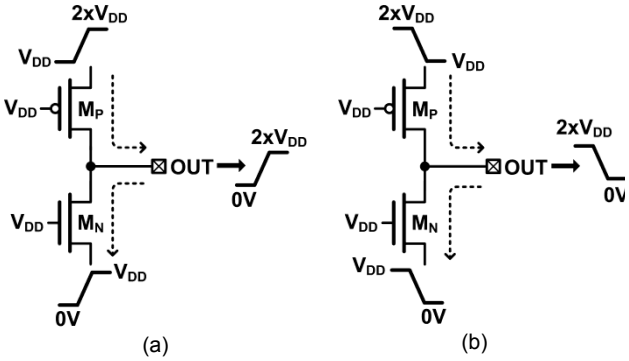


Figure 1: Dynamic source bias technique when driving the signals to (a) logic high and (b) logic low.

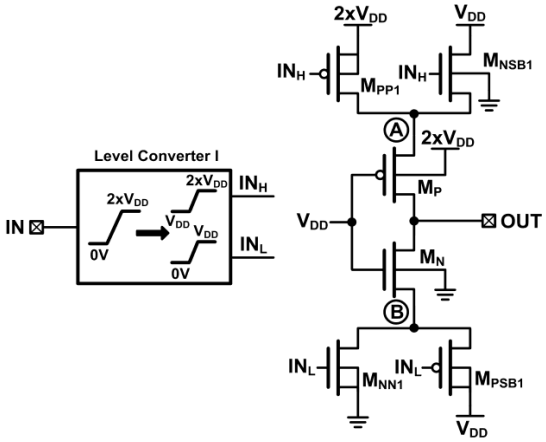


Figure 2: Circuit schematic of NOT gate with 2xV_{DD} tolerant capability.

By implementing the dynamic source bias technique into the circuit, complementary logic gates can be modified to have 2xV_{DD} tolerant capability. Fig. 2 shows the 2xV_{DD} NOT gate. M_P and M_N with gate voltages of V_{DD} are used to conduct logic level to output and avoid gate-oxide overstress issue during operation. M_{PP} and M_{NN} are

used to decide the function of logic gate. M_{NSB1} (M_{PSB1}) is used to bias the source voltage of M_P (M_N) at V_{DD} when M_{PP} (M_{NN}) is turned off during operation. Since the device operation voltage is not allowed to exceed $1xV_{DD}$ range, the 0V-$2xV_{DD}$ input signal needs to be separated to a 0V-V_{DD} and a V_{DD}-$2xV_{DD}$ control signal for pull-low path and pull-high path, respectively.

Fig. 3 illustrates the proposed level converter I, which converts the 0V-$2xV_{DD}$ voltage signal to the required voltage signals. As shown in Fig. 3, when the input signal IN is from 0V to V_{DD}-Vth, where V_{th} is MOSFET's threshold voltage, M_{N1} and M_{P2} are turned on. IN_L is conducting the voltage signal from 0V to V_{DD}-Vth, and IN_H is biased at V_{DD}. When IN signal is from V_{DD}+V_{th} to $2xV_{DD}$, M_{N2} and M_{P1} are turned on. IN_H is conducting the voltage from V_{DD} to $2xV_{DD}$ and IN_L is biased at V_{DD}. By the proposed level converter I, the 0V-$2xV_{DD}$ voltage signal can successfully be separated to a 0V-V_{DD} voltage signal IN_L and a V_{DD}-$2xV_{DD}$ voltage signal IN_H. Then, the IN_L signal is connected to the M_{NN} and M_{PSB1} at pull-low path, while the IN_H signal is connected to the M_{PP} and M_{NSB1} at pull-high path (as shown in Fig. 2). With those circuit arrangements, the voltage across each MOSFET does not exceed $1xV_{DD}$ voltage range. Moreover, the output voltage signal can be driven to the required $2xV_{DD}$ magnitude.

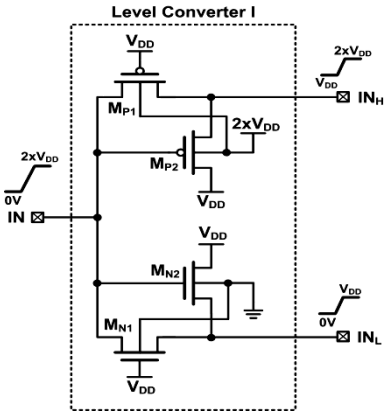
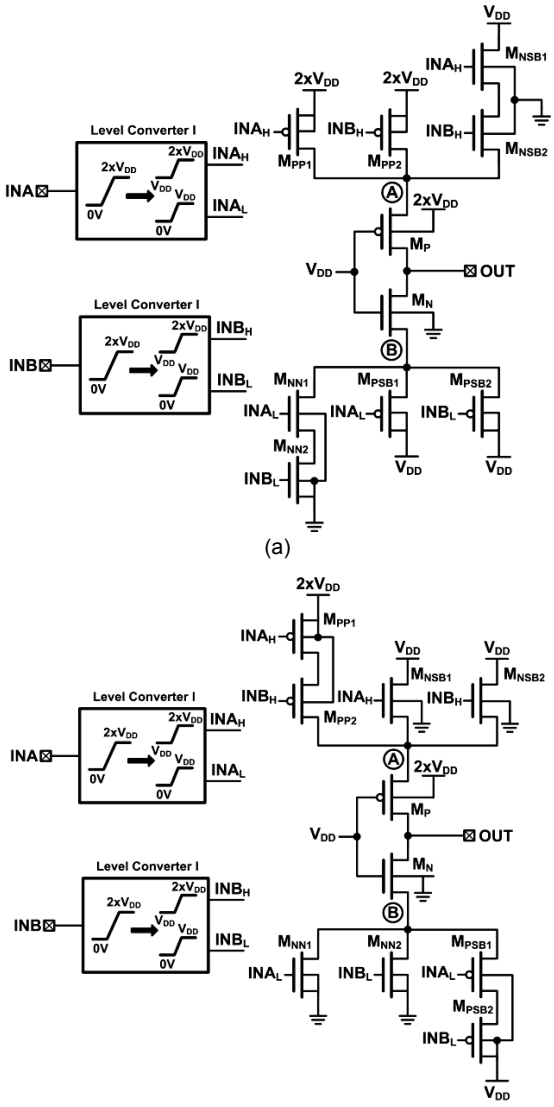


Figure 3: Circuit implementation of level converter I.

For example, when the $2xV_{DD}$ NOT gate input signal IN is 0V, the IN_L signal is also 0V to turn off the M_{NN} and turn on M_{PSB1}. At the same time, the IN_H signal is driven to V_{DD} to turn on M_{PP} because the source voltage is $2xV_{DD}$. Therefore, the output voltage of the $2xV_{DD}$ NOT gate is driven to $2xV_{DD}$ and the voltage at node B is biased to V_{DD}. On the other hand, when input signal IN is $2xV_{DD}$, the IN_L signal is V_{DD} to turn on the M_{NN} and turn off M_{PSB1}. At the same time, the IN_H signal is driven to $2xV_{DD}$ to turn off M_{PP} and turn on M_{NSB1}. Therefore, the output voltage of the $2xV_{DD}$ NOT gate is driven to 0V and the voltage of node A is biased to V_{DD}. Whether the output voltage is pulled high to $2xV_{DD}$ or pulled low to 0V, each two terminals of all MOSFETs do not exceed a $1xV_{DD}$. Thus, gate-oxide overstress issue can be completely avoided in the proposed $2xV_{DD}$ NOT gate.



(a)

(b)

Figure 4: Circuit schematics of (a) NAND and (b) NOR gates with $2xV_{DD}$ tolerant capability.

With the design concepts, the NAND and NOR logic gates can also be modified to have $2xV_{DD}$ tolerant capability. Figs. 4(a) and 4(b) show the $2xV_{DD}$ NAND and $2xV_{DD}$ NOR gate, respectively. M_P and M_N with gate voltage of V_{DD} are also used to conduct logic level to the output and avoid gate-oxide overstress issue. M_{PP1}, M_{PP2}, M_{NN1}, and M_{NN2} are used to define the function of logic gate. M_{PSB1},

M_{PSB2}, M_{NSB1}, and M_{NSB2} are used to bias the source voltage of M_P and M_N at V_{DD} when the pull-low or pull-high path is turned off during operation.

In order to achieve the correct logic operation, the function defining devices and source biasing devices need to have complementary structure when the logic gates have more than one input. For example, with the series connection of NMOS M_{NN1} and M_{NN2} in the $2xV_{DD}$ NAND gate's pull-low path, the source bias PMOS M_{PSB1} and M_{PSB2} should be in parallel connected at the source terminal of M_N, as shown in Fig. 4(a). Even though the pull-low path is turned off when input IN_A and IN_B are with opposite logic signals, node B still can be biased to the safe voltage of V_{DD} by M_{PSB1} or M_{PSB2}. Figs. 5(a), 5(b), and 5(c) show the simulated voltage waveforms of $2xV_{DD}$ NOT, NAND, and NOR gates, respectively. Besides, the corresponding circuit logics and devices' behavior of each $2xV_{DD}$ logic gate are summarized in Tables 1 ~ 3.

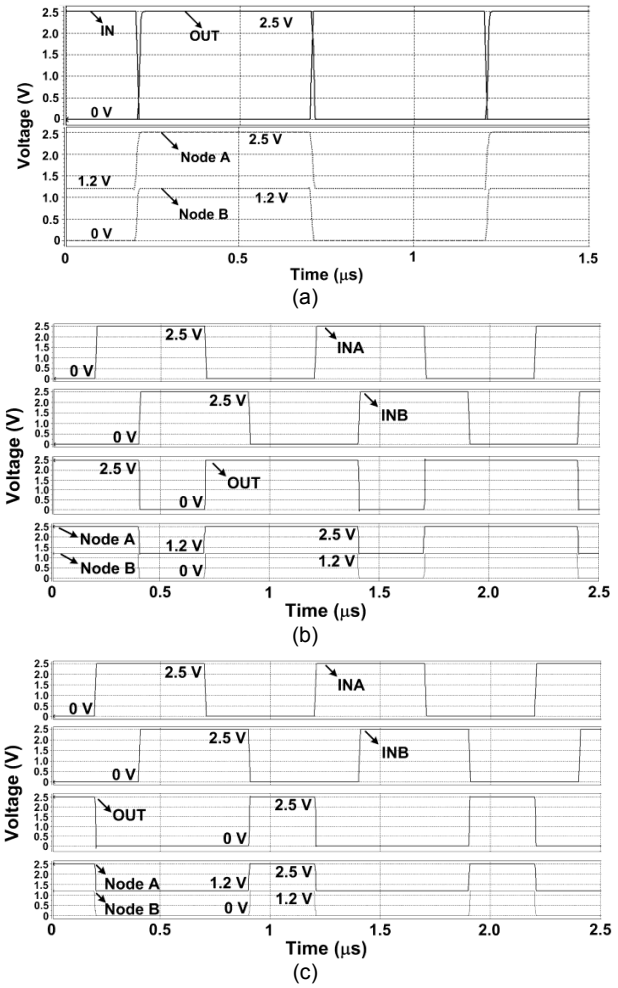


Figure 5: Simulated voltage waveforms of $2xV_{DD}$ (a) NOT gate, (b) NAND gate, and (c) NOR gate, with signal voltage level of 2.5 V ($2xV_{DD}$).

To implement in a 90-nm CMOS process, the normal operating voltage ($1xV_{DD}$) for core devices is 1.2 V. In the simulated results, each $2xV_{DD}$ logic gate performs the correct logic operation, and no gate-oxide overstress issue was encountered in all MOSFETs.

Table 1: Corresponding circuit logics and devices' behavior in proposed $2xV_{DD}$ NOT gate.

Circuit Logic	Pull-High	Pull-Low
IN	0	$2xV_{DD}$
IN_L	0	V_{DD}
IN_H	V_{DD}	$2xV_{DD}$
Node A	$2xV_{DD}$	V_{DD}
Node B	V_{DD}	0
OUT	$2xV_{DD}$	0
M_{PP}	ON	OFF
M_{PSB1}	ON	OFF
M_P	ON	OFF
M_{NN}	OFF	ON
M_{NSB1}	OFF	ON
M_N	OFF	ON

Table 2: Corresponding circuit logics and devices' behavior in proposed $2xV_{DD}$ NAND gate.

Circuit Logic	Pull-High	Pull-High	Pull-High	Pull-Low
(INA, INB)	(0, 0)	(0, $2xV_{DD}$)	($2xV_{DD}$, 0)	($2xV_{DD}$, $2xV_{DD}$)
(INA_L, INB_L)	(0, 0)	(0, V_{DD})	(V_{DD}, 0)	(V_{DD}, V_{DD})
(INA_H, INB_H)	(V_{DD}, V_{DD})	(V_{DD}, $2xV_{DD}$)	($2xV_{DD}$, V_{DD})	($2xV_{DD}$, $2xV_{DD}$)
Node A	$2xV_{DD}$	$2xV_{DD}$	$2xV_{DD}$	V_{DD}
Node B	V_{DD}	V_{DD}	V_{DD}	0
OUT	$2xV_{DD}$	$2xV_{DD}$	$2xV_{DD}$	0
M_{PP1}	ON	ON	OFF	OFF
M_{PP2}	ON	OFF	ON	OFF
M_{PSB1}	ON	ON	OFF	OFF
M_{PSB2}	ON	OFF	ON	OFF
M_P	ON	ON	ON	OFF
M_{NN1}	OFF	OFF	OFF	ON
M_{NN2}	OFF	ON	OFF	ON
M_{NSB1}	OFF	OFF	ON	ON
M_{NSB2}	OFF	OFF	OFF	ON
M_N	OFF	OFF	OFF	ON

Table 3: Corresponding circuit logics and devices' behavior in proposed $2xV_{DD}$ NOR gate.

Circuit Logic	Pull-High	Pull-Low	Pull-Low	Pull-Low
(INA, INB)	(0, 0)	(0, $2xV_{DD}$)	($2xV_{DD}$, 0)	($2xV_{DD}$, $2xV_{DD}$)
(INA_L, INB_L)	(0, 0)	(0, V_{DD})	(V_{DD}, 0)	(V_{DD}, V_{DD})
(INA_H, INB_H)	(V_{DD}, V_{DD})	(V_{DD}, $2xV_{DD}$)	($2xV_{DD}$, V_{DD})	($2xV_{DD}$, $2xV_{DD}$)
Node A	$2xV_{DD}$	V_{DD}	V_{DD}	V_{DD}
Node B	V_{DD}	0	0	0
OUT	$2xV_{DD}$	0	0	0
M_{PP1}	ON	ON	OFF	OFF
M_{PP2}	ON	OFF	OFF	OFF
M_{PSB1}	ON	OFF	OFF	OFF
M_{PSB2}	ON	OFF	ON	OFF
M_P	ON	OFF	OFF	OFF
M_{NN1}	OFF	OFF	ON	ON
M_{NN2}	OFF	ON	OFF	ON
M_{NSB1}	OFF	OFF	ON	ON
M_{NSB2}	OFF	ON	OFF	ON
M_N	OFF	ON	ON	ON

III. EXPERIMENTAL RESULTS

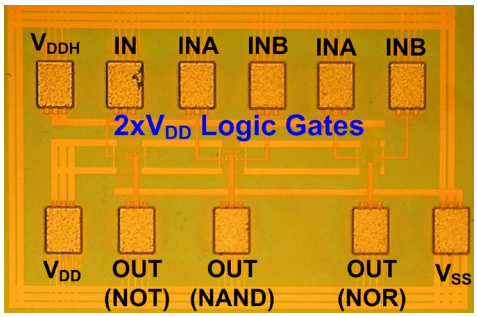


Figure 6: Chip micrograph of the 2xV_{DD} logic gates fabricated in a 90-nm CMOS process with 1.2-V devices.

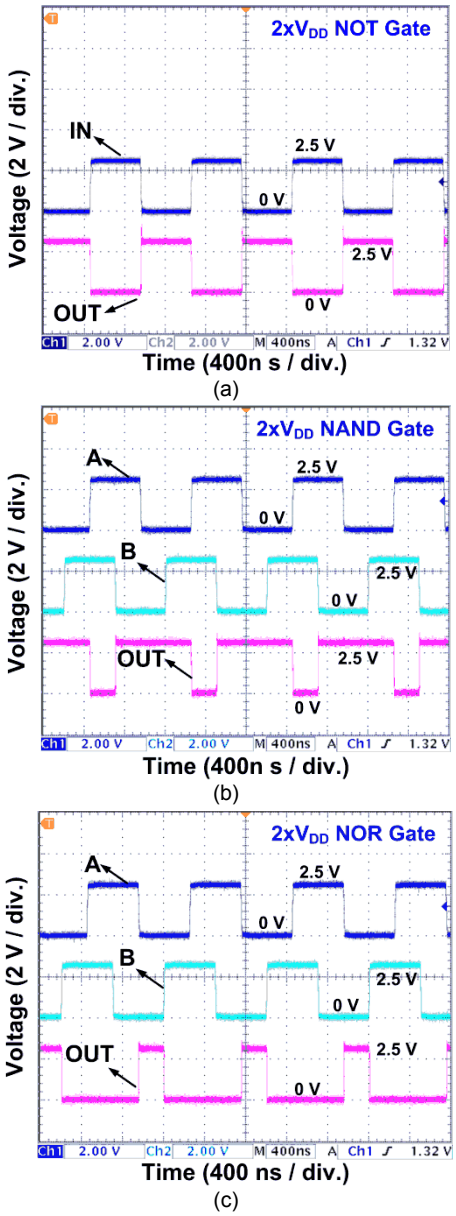


Figure 7: Measured voltage waveforms of 2xV_{DD} (a) NOT gate, (b) NAND gate, and (c) NOR gate, with 2xV_{DD} of 2.5V.

The new proposed 2xV_{DD} logic gates have been fabricated in a 90-nm CMOS process with 1.2-V devices. The micrograph of test chip is shown in Fig. 6. The measured voltage waveforms of 2xV_{DD} NOT, NAND, and NOR gates are shown in Figs. 7(a), 7(b) and 7(c), respectively. The input data rate verified in those figures is 1 MHz. The measured results have demonstrated that the proposed 2xV_{DD} logic gates can be safely operated with the voltage signals of 2.5 V to provide the correct logic functions.

IV. CONCLUSION

Novel 2xV_{DD} logic gates have been proposed and verified in a 90-nm CMOS process with only 1.2-V (1xV_{DD}) devices. By using the dynamic source bias technique, the CMOS logic gates are realized to have 2xV_{DD} tolerant capability without suffering gate-oxide reliability issue. The proposed 2xV_{DD} logic gates can be used in the applications of microelectronic systems facing the mixed-voltage environments. The circuit solution proposed in this work can be generally applied to all CMOS processes to realize 2xV_{DD} logic gates with only 1xV_{DD} devices.

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