Analysis and Solution to Overcome EOS Failure Induced by Latchup Test in A High-Voltage Integrated Circuits

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Abstract—**Proper layout and additional circuit solution have been proposed to solve the practical EOS failure induced by latchup test in an industry case of high-voltage integrated circuits (IC). The modified design has been implemented in 0.6-um 40-V BCD (Bipolar-CMOS-DMOS) process to successfully pass the 500-mA negative trigger current test. By eliminating overstress damages as happened in the prior work with only guard ring protection, the proposed solution can be adopted to implement high-voltage-applicable IC products which meet the requirement of industry applications with sufficient latchup immunity.**

Keywords- Latchup, electrical overstress (EOS), high-voltage IC, regulator.

I. INTRODUCTION

In the design of HV IC's, an interface as a high-voltage-tolerated pre-regulator is usually required between HV and LV blocks. By preventing high voltage paths to the inner low-voltage circuits and providing the necessary low supply voltage to maintain normal operation with high-voltage-tolerated pre-regulator, most main functions in circuits can be implemented by LV devices and make the chip area more compressive. However, high-voltage drift Nwell (HVNW) junctions in the HV devices used in HV blocks as the HV pre-regulator are more sensitive to the sink current brought by the parasitic bipolar transistor. Moreover, certain node voltages in pre-regulator may be abnormal affected by the induced current and lead to EOS problems due to mis-conduction from low voltage to high voltage paths.

A common failure, latchup, is generally examined in IC industry for qualified product manufacture with specification and methodology specified in the JEDEC latchup test standard [1]. The mechanism for latchup is triggered by overshooting/undershooting voltage or current perturbation to the parasitic PNPN structure and causes the occurrence of low impedance path between the supply and ground. For the trigger source comes from other place in the chip or the terminal of the PNPN structure, it can be distinguished to external or internal latchup, respectively [2]-[4].

To examine the latch-up immunity, positive or negative current perturbation is given to the pin of ICs during positive or negative current test (I-test). However, when large sink current is applied in the negative current test, the above mentioned unexpected mis-conduction may happen due to the improper layout placement related with circuit structure. Thus,

permanent damages [5]-[6] at the metal connections or junctions of LV devices may also be brought by such overstress damages and make ICs fail to normal operation.

To enhance the latch-up immunity of the chips, guard ring protection is often used to reduce the substrate current which flows in the inner circuit blocks [7]-[8]. However, wider width of guard rings as well as wider distance between the trigger source at I/O pin and the inner circuit increase the chip area or the fabrication cost [9].

In this work, a practical industry high-voltage integrated circuits suffers EOS damages induced by the latchup negative I-test was presented. The modifications including layout and circuit aspects are also illustrated with experimental results to verify the improvement.

II. A PRACTICAL INDUSTRY DESIGN SUFFERS NEGATIVE I-TEST INDUCED EOS FAILURE

Figure 1 shows a simplified structure for practical high-voltage-tolerable IC. The necessary low supply voltage such as ~3.3 V (at VAP node) or ~2 V (at VPD node) to the analog or digital LV inner circuit is generated by the high-voltage-tolerable pre-regulator, respectively. The schematic of the pre-regulator in the practical design is shown as Figure 2. It contains 5-V LV devices (MN1, MN2, and MP1), HV NMOS transistors (MHN1 to MHN4) with 40-V tolerance of drain-to-source voltage difference ($|Vds|$) and HV PMOS transistors
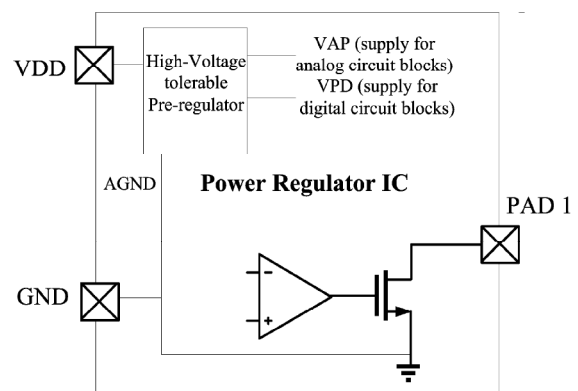

Figure 1. Simplified structure for a practical high-voltage tolerable power regulator IC.

(MHP1 to MHP7) with up to 40-V tolerance of source-to-drain voltage difference (|Vsd|) in a 40-V HV process. The main structure of the high-voltage-tolerable pre-regulator is a typical LDO circuit composed of a two-stage amplifier [10]. The IC can operate normally under the desired HV supply such as 40 V but still suffers damages after applying negative I-test as 100-mA sink current at some I/O PAD (as the PAD1 shown in Figure 1) with the high supply voltage (such as 30 V at VDD). The damaged chip photo is shown in Figure 3 with apparent burns located at the drain terminals of MHP6 and MHP7 that shows the short-through conduction happens from the supply voltage VDD to ground GND at the interfaces of high-voltage-tolerable pre-regulator to the LV digital blocks. From the failure result, it seems that even with the guard ring protection between the HV I/O PAD to the internal circuit blocks, the transistor MHP6 and MHP7 are still mis-conducted and cause the above short-through paths.

To analysis the failures, the simplified cross-section graph from I/O PAD to the HV input pair (MHN1, MHN2) and the related parasitic NPN structure from the p-type substrate to the internal HVNW junctions of the guard ring as well as

HV NMOS transistors are shown in Figure 4(a) and (b). HV NMOS input pairs MHN1 and MHN2 are placed as MHN1-MHN2-MHN2-MHN1 in the layout with shared drain region of the two multipliers of MHN2 for compressing the die area. The parasitic NPN structure attributed by the guard ring is expected to provide the most current to the I/O PAD when the negative current is applied at the I/O PAD (as the PAD1 depicted in Figure 3). However, the parasitic NPN structures to the HV NMOS (MHN1,2,4) are still triggered to induce some current with amount related to the junction area of the parasitic devices and also the distance from the current source to the affected victims. Moreover, the double area of the HVNW junction connected to the drain terminal of MHN2 than that connected to the drain terminal of MHN1 as shown in Figure 4(a) brings more current sunk at the drain terminal of MHN1. Therefore, the voltage of gate terminal for MHP6 and MHP7 is pulled low leads to the conduction of MHP6 and MHP7 to cause the overstress failures in the practical work as shown in Figure 3.
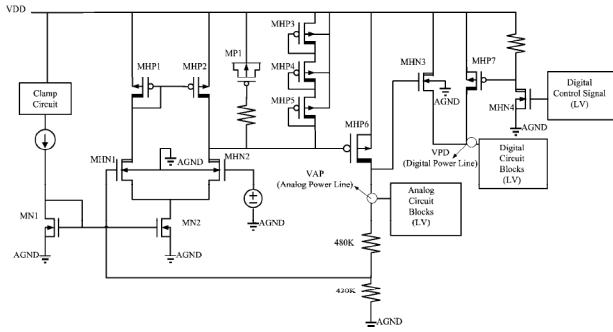

Figure 2.   The high-voltage-tolerable pre-regulator in this practical work.
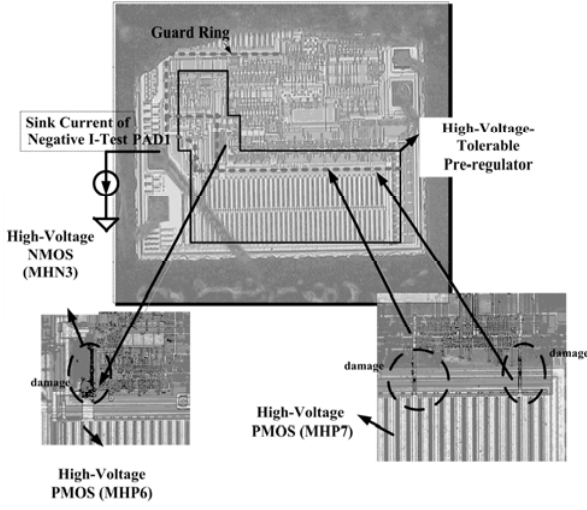

Figure 3.   Chip photo of the practical IC with negative I-test induced EOS damages fabricated in 0.6-um 40-V BCD process. The guard ring connected to VDD is presented by the dotted line in the photo.
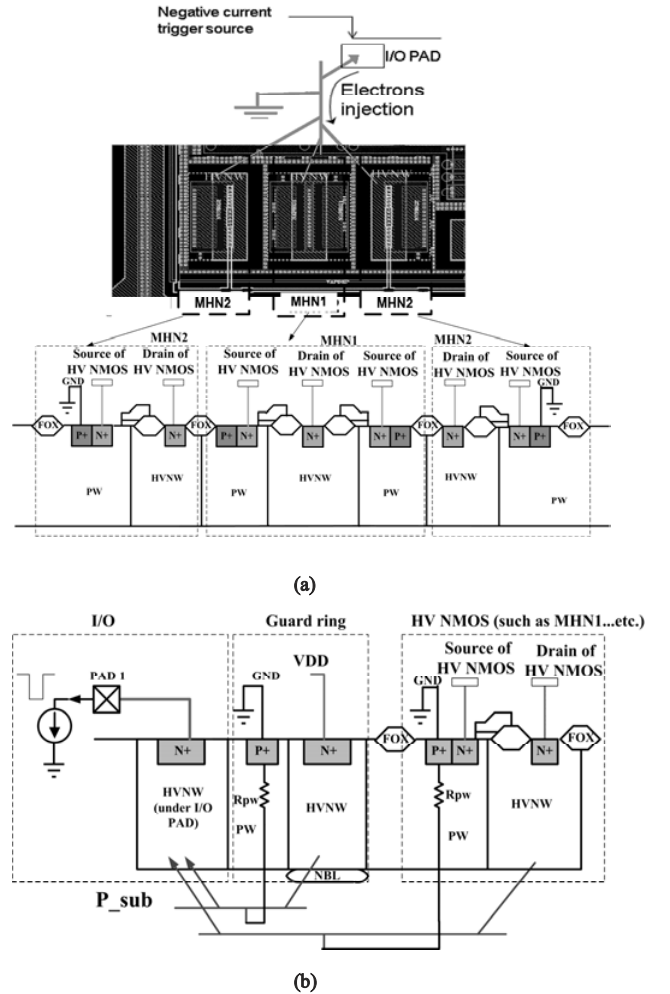

(a)

(b)

Figure 4.   (a) The simplified cross-section graph from I/O PAD to the HV input pair (MHN1, MHN2) and (b) the related parasitic NPN structures from the p-type substrate to the internal HVNW junctions of the guard ring and HV NMOS tranistors.

III. NEW REVISED DESIGN TO PREVENT LATCH-UP TEST INDUCED EOS FAILURE

A. Redesign for layout

The simplified improper layout placement for the input pair MHN1 and MHN2 of the original work is shown in Figure 5(a) and the proper modification is shown in Figure 5(b) respectively. With exchanged locations of the input pair (MHN1 and MHN2), more current can be sunk at the node connected to the drain terminal of MHN1 than that of MHN2. Thus, the compensated current is enough from the current mirror structure to pull high the voltage at the gate terminal of MHP6 to disturb the conduction from external supply VDD to inner supply VAP and VPD through MHP6.

B. Redesign with additional circuit

Figure 6 shows the proposed modification with additional sensing and compensation circuits [11] to reduce the overstress effect bringing by the induced sink current. Under normal operation, the HV NMOS MHN5 and HV PMOS MHP8~10 are all turned off but offer the sink current corresponding to the sensed large negative current at PAD 1 through the parasitic NPN structure. By connecting the drain terminals of the HV PMOS transistors as MHP9 and MHP10 to the nodes as the gate terminals of MHP6 and MHP7, the latchup-test-induced sink current can be compensated. Thus, the gate voltages of MHP6 and MHP7 were prevented from pulled low to trigger low impedance paths from external HV supply to inner LV supply. Such sensing technique can also be adapted to provide a digital enable signal to prevent the effect by mis-trigger of certain logic circuit under negative-current-triggered latch-up test.

Figure 6. The schematic of the revised design with new proposed sensing and compensation circuit.

IV. EXPERIMENTAL RESULTS

The proposed layout replacement and additional circuit solution have been verified with 0.6-um 40-V BCD process in the revised version of the HV IC. Figure 7 shows the measured inner supply voltage (VAP) with 6-V external voltage VDD. When a 30-mA sink current is applied at the PAD 1, the inner supply voltage VAP is pulled up from the normal value (~3.3 V) to the voltage near VDD and thus is damaged directly when the applied voltage VDD is higher than the breakdown voltage of LV junctions. Figure 8 shows the revised design with the exchange of layout locations and is verified by 500-mA sink current test that the inner supply voltage VAP will be pulled

Figure 7. Measured inner supply voltage when a 30-mA sink current is applied at the PAD 1 of the original IC without modification.

Figure 8. Measured inner supply voltage with a 500-mA sink current at the PAD 1 of the revised design with proper layout at input pair of the pre-regulator.
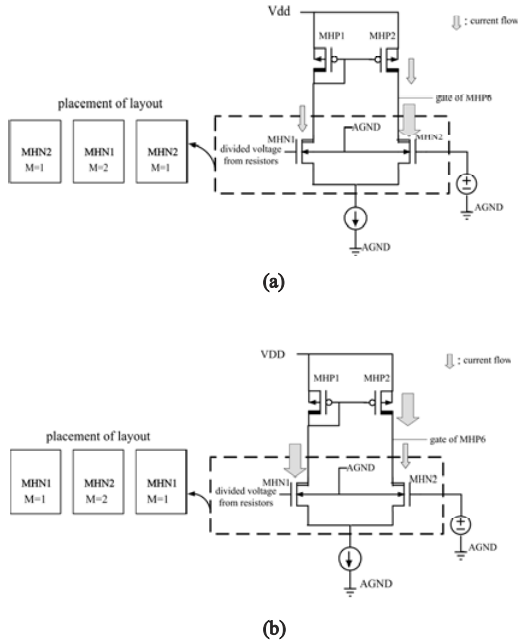

(a)

(b)

Figure 5. (a) Improper layout placement for the input pair composed of MHN1 and MHN2 in the original work. (b) The proper modification of the revised design with replacement in layout by metal re-connection.
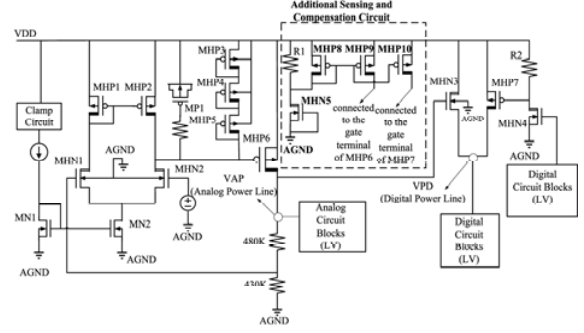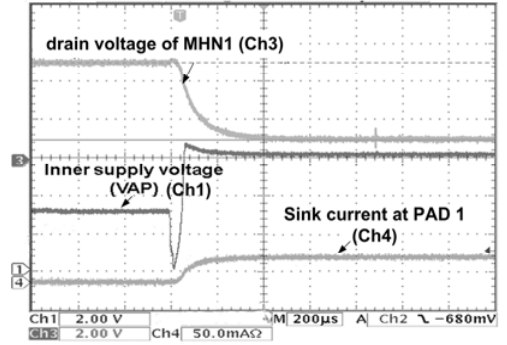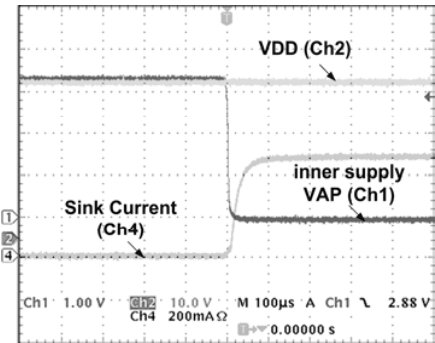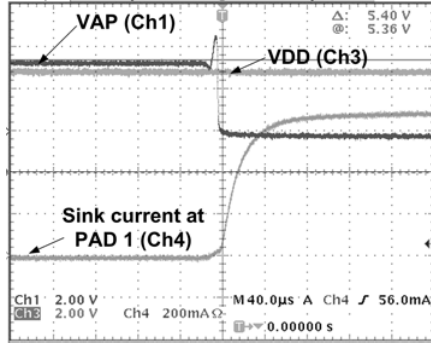
Figure 9. Measured inner supply voltage with a 700-mA sink current at the PAD 1 of the revised design with proper layout at input pair of the pre-regulator.
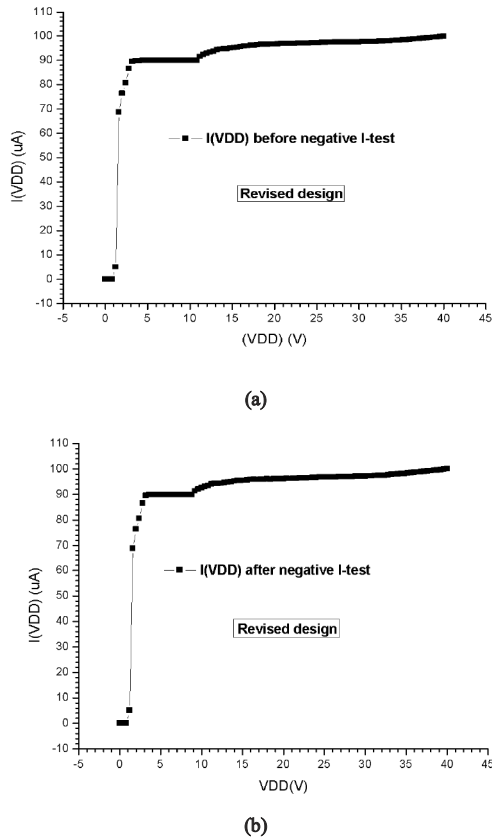

(a)

(b)

Figure 10. Measured external supply current I(VDD) to the related supply voltage (VDD) for the revised design with the modifications (a) before, and (b) after, the negative I-test with 100-mA sink current at PAD1.

low directly to avoid the electrical overstress. The measured inner supply voltage with a 700-mA sink current for the revised design with circuit modifications is shown in Figure 9. It also shows a pulled-down reaction for VAP to prevent the overstress to the LV blocks. Figure 10(a) and (b) present the measured external supply current I(VDD) corresponding to the

related supply voltage (VDD) for the revised design with both modifications before and after 100-mA negative I-test. Without additional large leakage current, the modification is verified to prevent the damages of prior design successfully.

V. CONCLUSION

The proposed layout arrangement and circuit modifications to solve the EOS problem induced by the negative I-test have been verified successfully in silicon and pass at least 500-mA latch-up test. By eliminating the unexpected conduction from HV external supply to inner power of LV blocks, the revised design has improved robustness for HV environment while remains qualified latch-up immunity to meet the requirement for Industry applications.

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