Ultra-Low-Leakage Power-Rail ESD Clamp Circuit in a 65-nm CMOS Technology

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***Abstract*—The gate tunneling current impacts seriously on the power-rail ESD clamp circuit, causing a large leakage current through the MOS capacitor used in ESD detection. In this work, a novel technique is implemented to eliminate the gate leakage current through the MOS capacitor by using a couple of transistors to control the voltage drop across the RC delay in the ESD detection circuit. This circuit has been verified in a 65-nm CMOS technology, with a total leakage current of 165nA under 1V bias, at 25°C, and a ESD robustness of 3kV HBM and 200V MM.**

I. Introduction

Electrostatic discharge (ESD) is one of the most important reliability issues in ICs, and it must be taken into consideration during the design phase [1]. Since ESD specification is not scaled down with the CMOS technology, efficient ESD protection design for the nanoscale CMOS devices with thinner gate oxide becomes more challenging. In the whole-chip ESD protection scheme (shown in Fig. 1), the power-rail ESD clamp circuit plays an important role because it determines the overall ESD robustness of the IC [2]. The power-rail ESD clamp circuits are designed to provide the ESD current path between V_{DD} and V_{SS} during ESD stresses, and to be kept off under normal power-on conditions. The traditional power-rail ESD clamp circuit was realized with RC-based ESD-detection circuit and an ESD clamp device. With the consideration on the area efficiency, the capacitor in the ESD-detection circuit was often realized with the MOS capacitor (MOS capacitors have the largest capacitance per unit area in generic CMOS processes). However, the gate leakage current in the MOS capacitor becomes serious in nanoscale CMOS processes [3], [4], and impacts drastically on the leakage current of the power-rail ESD clamp circuits. With the large gate leakage through the MOS capacitor, the power-rail ESD protection circuit with the traditional RC structure cannot be used anymore. A new design to further reduce the leakage current in the power-rail ESD clamp circuit is necessary.

In this work, a new circuit topology is used to eliminate the leakage current of the MOS capacitor by dynamically adjusting the voltage across the capacitor.

II. Traditional Power-Rail ESD Clamp Circuit

The traditional power-rail ESD clamp circuit is shown in Fig. 2. The circuit is comprised of an RC transient detection circuit formed by R and M_{CAP}, a trigger circuit formed by M_p and M_n, and a silicon controlled rectifier (SCR) as ESD clamp device. The SCR is preferred to the MOSFET as it can provide better ESD robustness per silicon area [5].

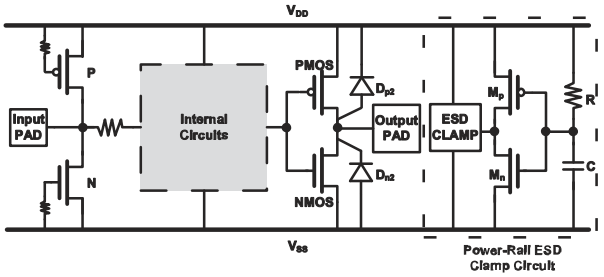

Fig. 1. Typical whole-chip ESD protection scheme designed with the power-rail ESD clamp circuit.

Under a positive ESD pulse zapping the node V_{DD} (V_{SS} grounded), the initial value of V_{rc} is kept to ~0V. The capacitor M_{CAP} then charges up the node V_{rc} with the RC time constant (~100ns). As the node V_{rc} remains low, the transistor M_p is turned on and drives the trigger current to the SCR, causing the SCR to turn on and therefore to protect the internal circuits.

Under normal circuit operation V_{rc} is ideally kept to V_{DD}. Therefore, M_p and M_n are turned off and on, respectively, so the SCR trigger node is tied to V_{SS}, maintaining the SCR in off state. The RC time constant of the capacitor M_{CAP} and resistor R is fast enough so the RC delay stage can follow the V_{DD} transient voltage and there are no misstriggers during the power-on ramp (usually 100μs to 1ms). In advanced CMOS technologies, there is a high leakage current through the capacitor (M_{CAP}) due to gate tunneling, which causes a voltage drop across the resistance R and prevents M_p to be fully turned off. There is, therefore, another source of leakage across the transistors M_p and M_n, which increases the total leakage current of the power-rail ESD clamp circuit.

The traditional power-rail ESD clamp circuit was simulated using the 65-nm SPICE models, with device sizes as specified in Table I. The overall leakage current with 1V bias voltage and T=25°C is 29.2μA. The simulation transient waveforms are shown in Fig. 3.

III. Ultra-Low-Leakage Power-Rail ESD Clamp Circuit

The origin of the leakage current in the traditional power-rail ESD clamp circuit is due to the voltage drop across

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TABLE I
DEVICE SIZES USED IN THE POWER-RAIL ESD CLAMP CIRCUITS IN THIS WORK

Device	R	M_{CAP}	M_p	M_n	M_{pg}	M_{ng}
Size	$50k\Omega$	$20\mu m/20\mu m$	$100\mu m/150nm$	$1\mu m/150nm$	$2\mu m/150nm$	$5\mu m/150nm$

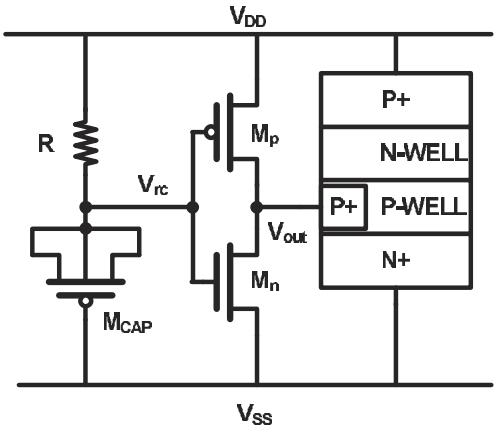


Fig. 2. Traditional power-rail ESD clamp circuit realized with the RC-based ESD transient detection and the substrate-triggered SCR device.

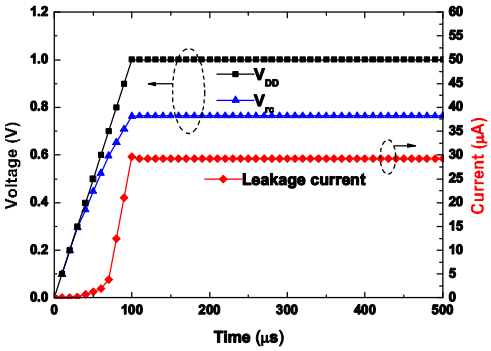


Fig. 3. Simulation results on the traditional ESD clamp circuit in a 65-nm CMOS process under normal V_{DD} power-on transition with a rise time of 0.1ms.

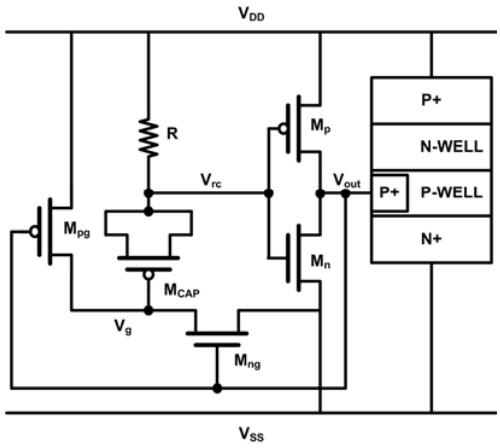


Fig. 4. Proposed power-rail ESD clamp circuit.

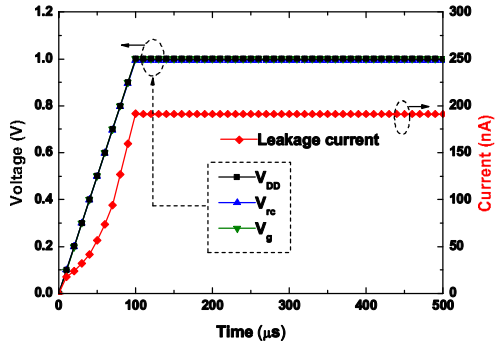


Fig. 5. Simulation results on the proposed ESD clamp circuit in a 65-nm CMOS process under normal V_{DD} power-on transition with a rise time of 0.1ms.

M_{CAP}. Some previous work used circuit techniques to reduce the voltage drop across M_{CAP} to effectively reduce the leakage current [6]. This idea could be extended to reduce the voltage drop across M_{CAP} to 0V to eliminate the leakage current, but under ESD stress the capacitor should have the whole voltage drop in order to function correctly. Therefore, the voltage drop across the capacitor requires two different states, dependeing whether the circuit is under normal circuit operation or under ESD stress. The capacitor voltage drop control can be implemented with a couple of extra transistors. The proposed power-rail ESD clamp circuit is shown in Fig. 4. The transistors M_{pg} and M_{ng} control the capacitor bottom plate voltage.

During power-on transition, V_{DD} raises to its full voltage level with a slow rise time. As the rise time is slower than the RC time constant, the node V_{rc} can follow V_{DD}. Therefore, the transistor M_p is turned off, as its gate-source voltage remains $\sim$0V. Moreover, the transistor M_n is turned on, tying the node V_{out} to V_{SS}, and maintaining the SCR in turn-off state. As the node V_{out} is $\sim$0V, the transistor M_{ng} is turned off and the transistor M_{pg} is turned on, driving V_g to V_{DD}. Therefore, both capacitor nodes, V_{rc} and V_g are biased to V_{DD}, and so the capacitor gate leakage current is eliminated.

When a positive ESD pulse is zapping at V_{DD} (V_{SS} grounded), the fast rise time nature of the discharge keeps the node V_{rc} low, so the transistor M_p is turned on and drives the node V_{out} high. As the node V_{out} is higher than V_{SS}, the transistor M_{ng} is turned on, tying the node V_g to V_{SS}, so the

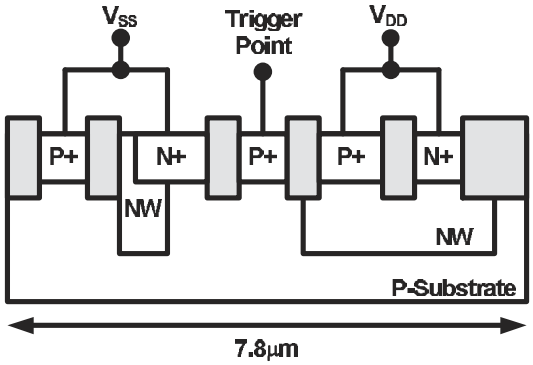


Fig. 6. Cross-sectional view of the SCR with the substrate trigger point. The device width is 40μm.

capacitor bottom node is connected to ground and therefore the node V_{rc} starts charging with the RC time constant. The node V_{rc} remains lower than the inverter (M_p and M_n) logic switch point during the ESD zap (set as a design consideration). Therefore, the node V_{out} remains high and drives the trigger current to the SCR, assuring the SCR turns on and therefore protecting the internal circuits from damage.

The proposed power-rail ESD clamp circuit was simulated using the 65-nm SPICE models, with device sizes as specified in Table I. The overall leakage current with 1V bias voltage and T=25°C is 191nA. There is a significant reduction in the current leakage from the traditional power-rail ESD clamp circuit (29.2μA). The simulation transient waveforms are shown in Fig. 5.

IV. Experimental Results

The traditional power-rail ESD clamp circuit of Fig. 2 together with the proposed power-rail ESD clamp circuit of Fig. 4 were realized in a 65-nm CMOS process using the device dimensions listed in Table I. The SCR is implemented as shown in Fig. 6, with 40μm width. The experimental results are summarized in Table II.

A. Leakage current

The leakage current is measured on-die at the controlled temperature. The circuits are probed at 1V bias voltage at 25°C and 125°C, respectively. The leakage current for the traditional power-rail ESD clamp circuit is 20.55μA and 103μA for T=25°C and T=125°C, respectively. The leakage current for the proposed power-rail ESD clamp circuit is only 165nA and 1.11μA for T=25°C and T=125°C, respectively.

B. TLP measurement

Transmission pulse line (TLP) is an important verification method for ESD protection circuits. The TLP measurement results are shown in Fig. 7. The V_{T1} voltage is ~3V for both circuits, which is lower than the gate oxide breakdown voltage (~5V for the 65-nm CMOS process). The failure current (I_{T2}) for both designs is ~2.3A.

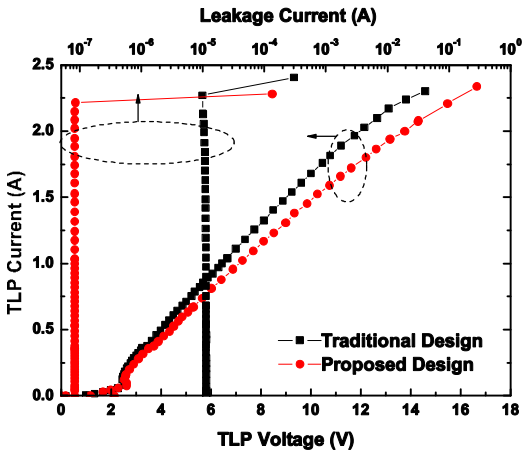


Fig. 7. TLP IV curves between the traditional and proposed power-rail ESD clamp circuits.

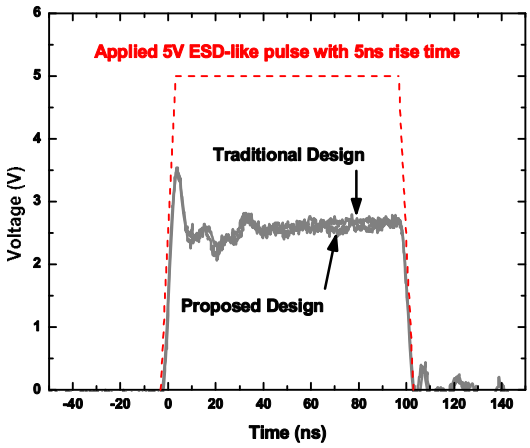


Fig. 8. Turn-on verification for the power-rail ESD clamp circuits implemented in this work.

C. Turn-on verification

The turn-on verification consists of applying a 5V pulse with rise time of 5ns to the device under test (DUT), and observe the voltage at the pad to verify whether the SCR is turned on and the pad voltage is clamped to a lower voltage. The turn-on verification transient waveforms are shown in Fig. 8. The SCR holding voltage for both power-rail ESD clamp circuits is ~2.5V, which is higher than the supply voltage (1V) and therefore is free of the latch-up issue.

D. HBM and MM verification

The ESD stress verification is perfomed by following the human-body-model (HBM) [7] and machine-model (MM) [8] standards. A simple schematic of the test model can be viewed in Fig. 9, whereas R_{ESD} and C_{ESD} are 1.5kΩ and 100pF for the HBM model, and 0Ω and 200pF for the MM model. The high voltage source is stepped with 500V step for HBM and 50V for MM. After each stress, the DUT IV curve is

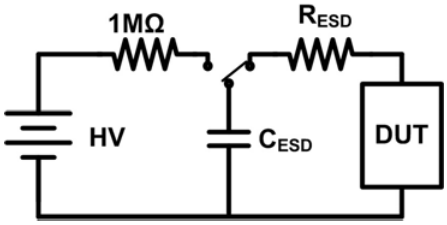
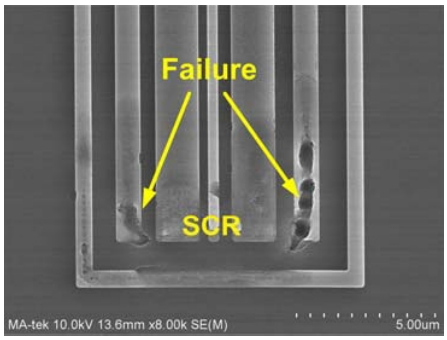
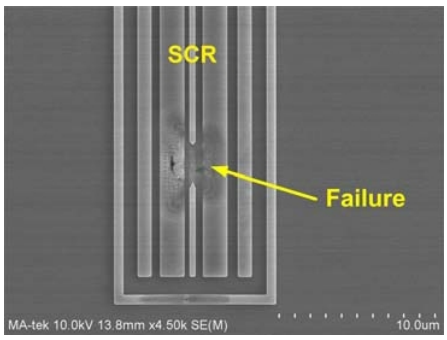


Fig. 9. HBM and MM ESD tests schematic. R_{ESD} and C_{ESD} are 1.5kΩ and 100pF for the HBM model, and 0Ω and 200pF for the MM model.



(a)



(b)

Fig. 10. Failure analysis for the proposed power-rail ESD clamp circuit after ESD stress of (a) 3.5kV HBM, and (b) 300V MM.

measured and compared with the nominal curve. Any deviation higher than 20% is considered as failure. Both traditional and proposed power-rail ESD clamp circuits failed at 3.5kV HBM and 300V MM. SEM analysis was done to find the failure locations. Fig. 10 shows the ESD failure located on the SCR for the proposed power-rail ESD clamp circuit. The ESD failures located on the traditional power-rail ESD clamp circuit are similar to the ones on Fig. 10.

TABLE II
COMPARISON AMONG THE POWER-RAIL ESD CLAMP CIRCUITS

Design	Leakage Current		ESD Performance		Technology
	T=25°C	T=125°C	HBM	MM	
Traditional	20.55μA	103μA	3kV	250V	65-nm
Ref. [9]	358nA	1.91μA	4kV	400V	65-nm
This work	165nA	1.11μA	3kV	250V	65-nm

* The leakage currents were measured under 1V bias.

V. CONCLUSION

A novel power-rail ESD clamp circuit with ultra-low standby leakage current was proposed and verified in a fully-silicided 65-nm CMOS process. The proposed design can effectively eliminate the capacitor gate leakage, resulting in a very low leakage current in the power-rail ESD clamp cicuit, which is ideal for low power applications.

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