Improvement on CDM ESD Robustness of High-Voltage Tolerant nLDMOS SCR Devices by Using Differential Doped Gate

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***Abstract*— Early failure has been observed during CDM ESD stress on high-voltage tolerant nLDMOS-SCR devices in a standard low-voltage CMOS technology due to the gate oxide (GOX) degradation. In this work, we propose a special p+/n+ differential doped gate which boosts the CDM ESD failure current level with a factor of 3 to 9.**

Keywords-Electrostatic Discharge (ESD); laterally diffused nMOS (nLDMOS); high-voltage tolerant (HVT) devices; transmission line pulsing (TLP) system; very fast TLP system (VFTLP); gate oxide reliability

I. INTRODUCTION

In order to develop cost-effective System-on-Chip (SoC) solutions, it is important to implement High-Voltage (HV) tolerant devices using standard CMOS technologies for varied applications, such as display and LED drivers, flash memories, automotive applications etc. However, HV-tolerant devices are usually very sensitive to ESD events [1]-[6]. The Laterally Diffused nMOS (nLDMOS) Silicon Controlled Rectifier (SCR) device is widely considered as one of the more reliable ESD solutions [4]-[6]. Some previous studies indicated that HV-tolerant nLDMOS (or nLDMOS SCR) would easily suffer from gate oxide damage or degradation during CDM ESD stress or constant voltage long-term stress [5]-[7]. The root cause of the oxide degradation has been already related to higher electrostatic potential on Si surface below the gate to n-well overlap region, inducing gate electrons tunneling and further subsequent hot carrier injection degradation of the gate oxide [7]. Reducing the gate to n-well overlap length in nLDMOS structures helps to relieve the oxide deterioration. However, it causes higher voltage overshoot during CDM ESD or VFTLP stress [5]. The higher voltage overshoot could damage the transistors to be protected in functional circuits.

The purpose of this work is to provide a solution which prevents gate oxide degradation under VFTLP stress, without increasing the voltage overshoot of nLDMOS SCR device. The proposed differential doped gate structure is fully compatible to standard CMOS technologies [8], [9]. In addition, TCAD simulations illustrate the different device physics of nLDMOS SCR devices with different gate doped types. This understanding is crucial for the ESD design and the optimization of nLDMOS or nLDMOS SCR devices.

II. DEVICES AND EXPERIMENTS

A. Device Structures

A conventional nLDMOS SCR device has been implemented with grounded gate in a standard 130 nm CMOS technology with ~2 nm SiO_2 gate oxide (GOX), 1 µm channel length (L_{CHAN}), 0.5 µm gate to N-well overlap length (L_{GN}) and 50 µm channel width. The gate of the conventional device is n-type doped, and it is used as a reference in this work. In order to prevent hot carrier generation and subsequent gate oxide degradation, a differentially doped gate is proposed for an improved nLDMOS SCR device, as shown in Fig. 1. At the left side of gate, the gate is n-type doped above the p-well region, forming an n-type channel from n+ source (at cathode) to n-well drift region which is connected to the n+ drain (at anode) during normal transistor operation. At the right side of gate, the gate is p-type doped above the n-well drift region and also extends above the STI structure.

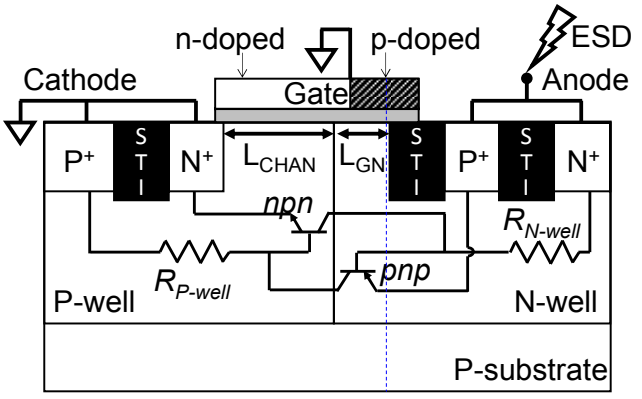

Fig. 1: Schematic cross-section (not to scale) of the proposed nLDMOS-SCR device with p+/n+ differential doped gate. The GOX is ~2 nm SiO_2, the channel length (L_{CHAN}) is 1 µm, the gate to n-well overlap length (L_{GN}) is 0.5 µm, and the channel width is 50 µm.

Figs. 2a and 2b show the band diagrams and e^- density along the depth (y) direction near the STI overlapped with different doped gates, which are n-doped and p-doped respectively, in the nLDMOS SCR devices. With a p-type doped gate in Fig. 2b, very low electron (e^-) density (minority carriers) can significantly suppress the possibility of e^- tunneling from gate to n-well and also the majority carriers (hole; h^+) will not be pulled from the low potential gate to the high potential n-well. Therefore, the proposed solution prevents hot carriers generation and subsequent gate oxide degradation.

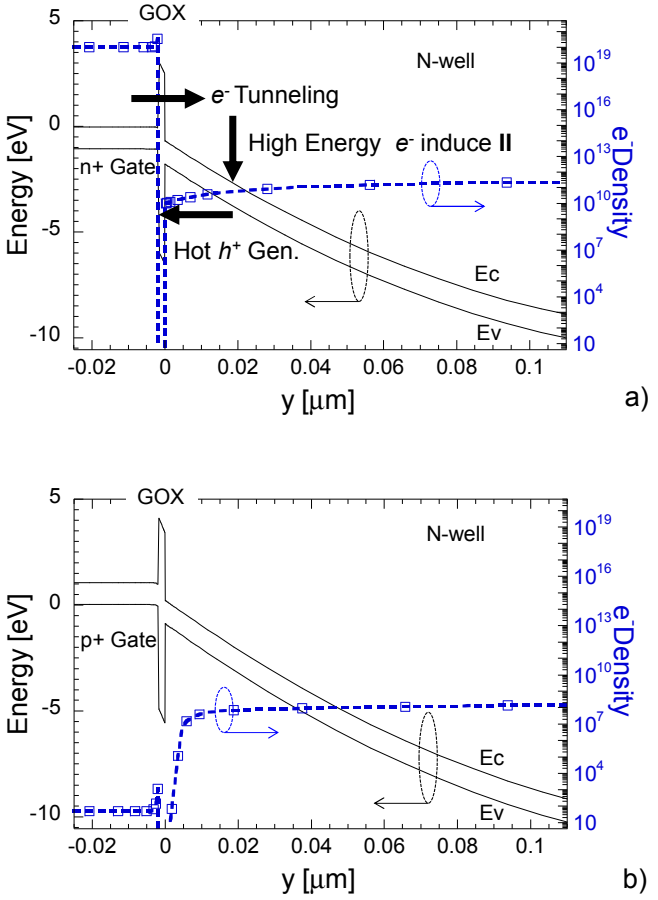

Fig. 2: Schematic band diagram and electron (e^-) density (refer to the vertical cut line in Fig. 1) in the gate to n-well overlap region of a) the conventional nLDMOS-SCR device with n+ doped gate and b) the proposed nLDMOS-SCR device with p+/n+ differential doped gate. The mechanisms relating to GOX degradation are depicted in a). A very low e^- density eliminates the possibility of e^- tunneling from gate to n-well in b).

B. *ESD Verification*

To investigate the ESD robustness, these devices were stressed by 100-ns TLP with 2 ns rise time and 2-ns VFTLP with 200 ps rise time. For both stress types, the ESD stress was applied to the anode, while the cathode and gate were grounded. The device DC leakage current was monitored after each stress step. A 10 % increase in leakage current was considered as device failure.

III. Results and Discussion

A. *TLP and VFTLP Verification Results*

Fig. 3 shows the VFTLP *IV* characteristics of the nLDMOS SCR devices with the conventional n-type doped gate and the proposed differential doped gate. The proposed device boosts the failure current *It2* level up to a factor of 3. On the other hand, the leakage current (I_{leak}) evolutions of these two devices also show a significant difference. The nLDMOS SCR device with only n-type doped gate has a progressive I_{leak} increase which suggests a GOX damage. However, the one with p+/n+ differential doped gate shows an abrupt I_{leak} increase which suggests thermal failure [5]. The nLDMOS SCR devices with different L_{GN} of 0.25 and 1 µm are also compared and the results are shown in Fig. 4.

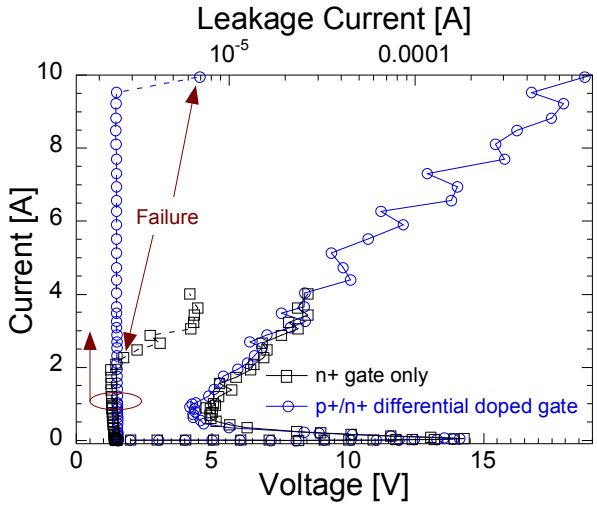

Fig. 3: VFTLP *IV* curves and corresponding DC leakage current evolution of the nLDMOS SCR devices with same L_{GN} of 0.5 µm but with different gate structures. The n+ doped gate shows a progressive leakage deterioration, but the differential gate shows an abrupt leakage increase.

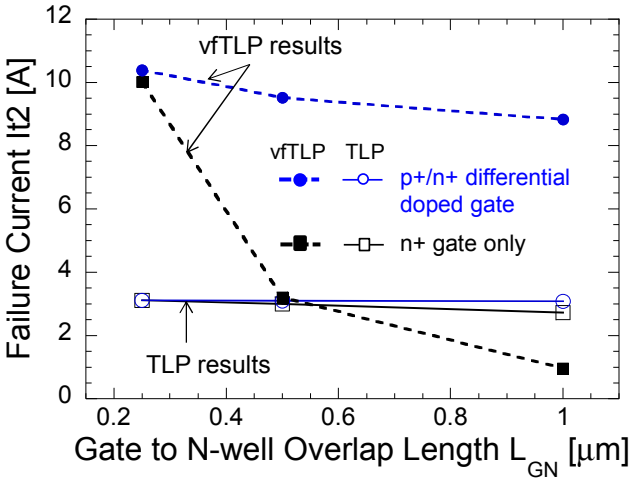

Fig. 4: Failure current *It2* as a function of the L_{GN} for the nLDMOS SCR devices with the conventional and proposed gate structures submitted to TLP and VFTLP stresses. The *It2* values are regardless of L_{GN} for TLP stress in both devices; however, VFTLP It2 values are significant difference in these two different gate doped type devices.

The TLP results show similar *It2* levels (3 A) in the devices with different L_{GN} and different doped gates. But, the VFTLP results show significantly different *It2* dependency on L_{GN} in the nLDMOS SCR devices with different gate structures. For the one with p+/n+ differential doped gate, the *It2* levels only slightly drop from 10.4 A to 8.9 A as L_{GN} increased from 0.25 to 1 µm. However, they drastically drop from 10 A to 1 A in the devices with n+ doped gate. The drastic VFTLP *It2* decrease for the latter one has been proven that the early failure for long L_{GN} device is attributed to GOX overstress inducing GOX deterioration [5]. Therefore, the devices with p+/n+ differential doped gate indeed prevent such GOX deterioration during VFTLP stress.

B. Physical Understanding

Besides CDM ESD (or VFTLP) stress, the conventional nLDMOS SCR ESD devices also show GOX degradation under off-state constant voltage stress [7]; therefore, TCAD simulations are used to further study the impact of different doped type gates on GOX deterioration. Fig. 5 shows the off-state gate I_{leak} varied with increasing drain (or anode) voltage. The devices with the differential doped gate show ~50 times less gate I_{leak} compared with the conventional device. This is firstly attributed to the very low e^- tunneling current from p-type gate to n-well in the proposed nLDMOS SCR device. In addition, the lower electrostatic potential on Si surface inside the n-well also contributes the lower gate I_{leak} of the proposed device in Fig. 6. It shows that even with a higher anode stress voltage, the device with differential doped gate has only less than half surface potential in the n-well close to the STI edge compared to the conventional device.

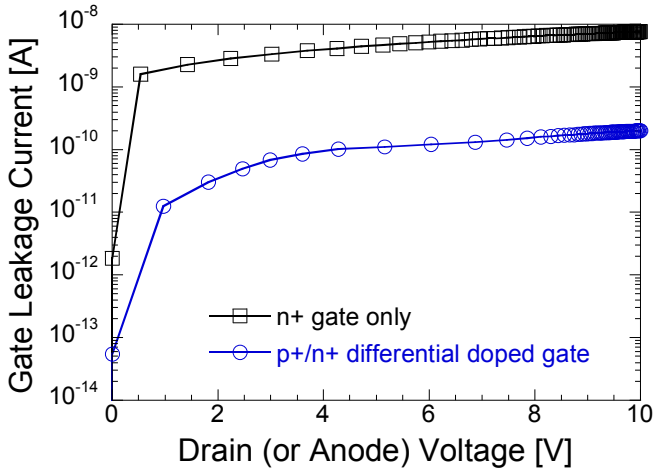

Fig. 5: TCAD simulated gate leakage currents as a function of drain voltage for the nLDMOS SCR devices (L_{GN}= 0.5 µm) with the conventional and proposed gate structures during the off-state bias condition which is gate and cathode terminals are grounded.

With very low e^- tunneling current and lower surface potential in the n-well, the device with differential doped gate shows differences of e^- and h^+ current distributions from conventional device, as shown in Figs. 7a~7d. Fig. 7a shows that the n+ doped gate can provide e^- tunneling current. These high energy tunneling e^- can further induce the impact ionization (II) to generate more e^- and h^+ carriers, increasing the total e^- and h^+ current density, as shown in Figs. 7a and 7c. Fig. 8 shows the impact ionization plots of these two devices. Compared to the impact ionization in the conventional device in Fig. 8a, the impact ionization is lower in the nLDMOS SCR device with differential doped gate (Fig. 8b). It is because of the relatively low e^- and h^+ current density, as shown in Figs. 7b and 7d.

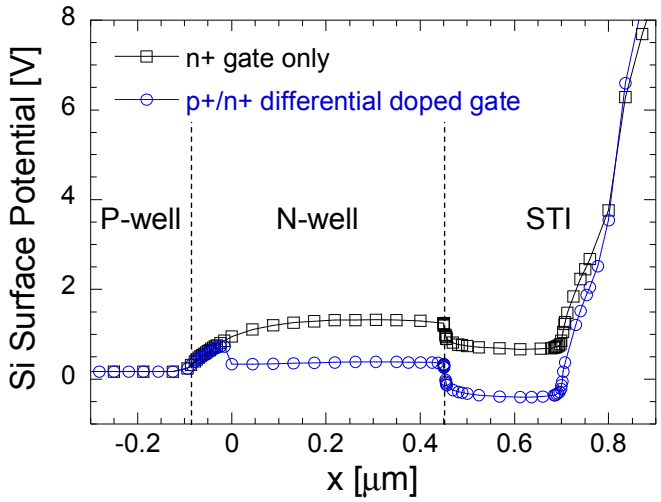

Fig. 6: TCAD simulated Si surface electrostatic potential versus horizontal distance in the nLDMOS SCR devices (L_{GN}= 0.5 µm) with the conventional and proposed gate structures submitted to the DC voltage of around 10 V stressed at the anode node during the off-state bias condition.

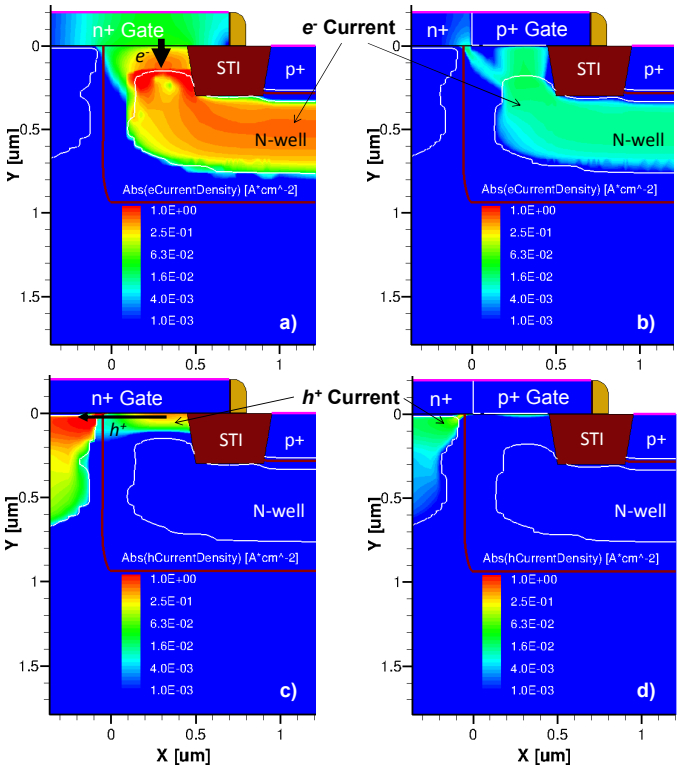

Fig. 7: 2D TCAD simulated a) and b) electron (e^-) current density and c) and d) hole (h^+) current density for the nLDMOS SCR devices (L_{GN}= 0.5 µm) with the conventional and proposed gate structures submitted to ~10 V anode stress voltage during off-state bias condition.

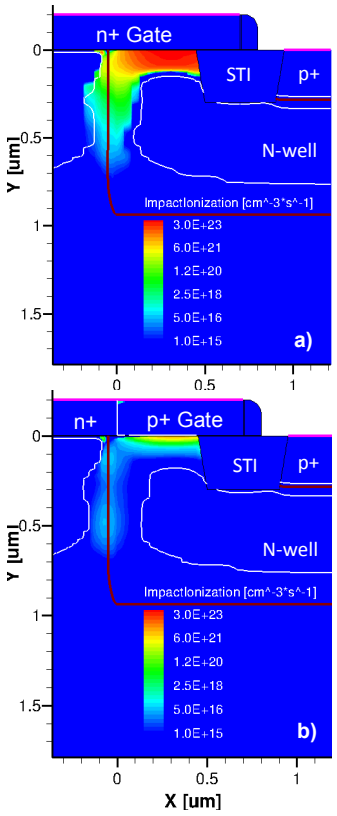

Fig. 8: 2D TCAD simulated impact ionization (II) plot for the nLDMOS SCR devices (L_{GN}= 0.5 µm) with a) the conventional and b) the proposed gate structures submitted to ~10 V anode stress voltage during off-state bias condition.

C. *Discussion on Long-term GOX Reliability*

Based on the above simulation results, the proposed p+/n+ differential doped gate can enhance the off-state GOX reliability of HV tolerant nLDMOS (or nLDMOS SCR) devices. In this part, the on-state GOX reliability will be further discussed. Figs. 9a and 9b show the on-state current distributions of the devices with the n+ doped and p+/n+ differential doped gates, respectively.

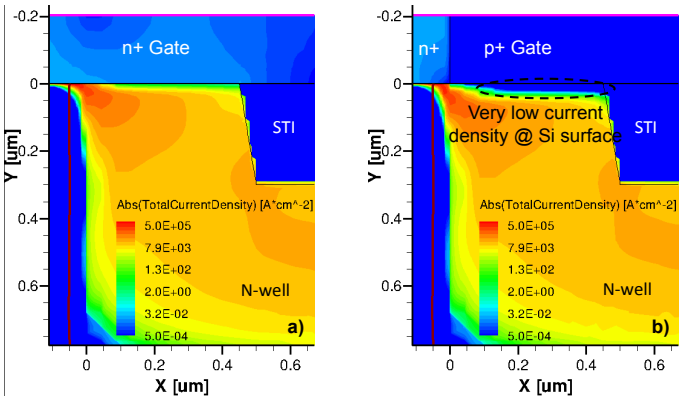

Fig. 9: 2D TCAD simulated total current density for the nLDMOS SCR devices (L_{GN}= 0.5 µm) with a) the conventional and b) the proposed gate structures submitted to ~2 V anode stress voltage when gate is biased at 1.32 V of the on-state bias condition.

The gate terminals are biased at 1.32 V and the drain terminals at ~2 V for these two different devices. The device with differential doped gate shows a very low current density at the Si surface inside the n-well, as shown in Fig. 9b. The on-state current seems to be blocked out from the Si surface inside the n-well. In addition, the on-state electrostatic potential on Si surface inside the n-well also shows a lower surface potential in the device with differential doped gate, as illustrated in Fig. 10. With a lower current density and surface potential, the proposed differential doped gate could also improve the on-state GOX reliability of HV tolerant nLDMOS (or nLDMOS SCR) devices. However, the maximum impact ionization location will not locate at the n-well close to STI. It will move to the edge between p-well can n-well due to the large on-state current from source to drain terminals in the on-state nLDMOS devices. Therefore, the impact of differential doped gate on GOX reliability needs to be investigated in the future.

IV. Conclusion

This work proposes a differential doped gate structure to suppress GOX degradation in HV tolerant nLDMOS SCR ESD devices. The VFTLP results show an enhancement of the *It2* levels by the proposed differential doped gate. The VFTLP *It2* levels boost ~9 times in the extreme case with L_{GN} of 1µm which can get lowest voltage overshoot under the VFTLP stress. The in-depth physical study further indicates the improvement on off-state GOX reliability in the devices with the proposed differential doped gate. The reasons can be attributed to a very low e^- tunneling current from p-type gate to n-well and a lower electrostatic potential on Si surface inside the n-well in the proposed nLDMOS SCR device. They indeed prevent such GOX deterioration during VFTLP stress. Finally, on-state GOX reliability may also be impacted by the gate doped type. With a lower current density and surface potential, the proposed differential doped gate could also improve the on-state GOX reliability of HV tolerant nLDMOS (or nLDMOS SCR) devices.

References

[1] A. Chatterjee, M. Shrivastava, H. Gossner, S. Pendharkar, F. Brewer, C. Duvvury, "An insight into the ESD behavior of the nanometer-scale drain-extended NMOS device- Part I: turn-on behavior of the parastic bipolar, *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 309–317, Feb. 2011.

[2] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part I: on the behavior of STI-Type DeNMOS device under ESD conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2235–2242, Sept. 2010.

[3] G. Boselli, V. Vassilev, and C. Duvvury, "Drain extended nMOS high current behavior and ESD protection strategy for HV applications in Sub-100nm CMOS technologies", in *Proc. International Reliability Physics Symposium - IRPS*, 2007, pp. 342-347.

[4] A. Concannon, V.A. Vashchenko, P. Hopper, and M. Ter Beek, "ESD protection of double-diffusion devices in submicron CMOS processes", in *Proc. ESSDERC*, 2004. pp. 261-264.

[5] A. Griffoni, S.-H. Chen, S. Thijs, D. Linten, M. Scholz, and G. Groeseneken, "Charged device model (CDM) ESD challenges for laterally diffused NMOS (nLDMOS) silicon controlled rectifier (SCR) devices for high-voltage applications in standard low-voltage CMOS technology," *in IEDM Tech. Dig.*, 2010, pp. 35.5.1-35.5.4.

[6] S.-H. Chen, S. Thijs, A. Griffoni, D. Linten, A. Keersgistere, and G. Groeseneken, "Unexpected failure during HBM ESD stress in

nanometer-scale nLDMOS-SCR devices," *in IEDM Tech. Dig.*, 2011, pp. 6.4.1-6.4.4.

[7] A. Griffoni, S.-H. Chen, S. Thijs, B. Kaczer, J. Franco, D. Linten, A. Keersgistere, and G. Groeseneken, "Off-state degradation of hig-voltage tolerant nLDMOS-SCR ESD devices," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 2061–2071, July 2011.

[8] S. Voldman, D. Hui, L. Warriner, D. Young, J. Howard, F. Assaderaghi, and G. Shahidi, "Electrostatic discharge (ESD) protection in Silicon-on-insulator (SOI) CMOS technology with aluminum and copper interconnects in advanced microprocessor semiconductor chips," in *Proc. EOS/ESD Symposium*, 1999, pp. 105-115.

[9] C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on different ESD protection strageies devoted to 3.3V RF applications (2GHz) in 0.18 mm CMOS process," in *Proc. EOS/ESD Symposium*, 2000, pp. 251-259.