Improving ESD Robustness of Stacked Diodes with Embedded SCR for RF Applications in 65-nm CMOS

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***Abstract* — To protect the radio-frequency (RF) integrated circuits from the electrostatic discharge (ESD) damage in nanoscale CMOS process, the ESD protection circuit must be carefully designed. In this work, stacked diodes with embedded silicon-controlled rectifier (SCR) to improve ESD robustness was proposed for RF applications. Experimental results in 65-nm CMOS process show that the proposed design can achieve low parasitic capacitance, low turn-on resistance, and high ESD robustness.**

Keywords – Diode, electrostatic discharge (ESD), radio-frequency (RF), silicon-controlled rectifier (SCR).

I. INTRODUCTION

Radio-frequency (RF) integrated circuits have been widely designed and fabricated in CMOS technologies due to the advantages of high integration and potential for mass production. The RF circuits realized in CMOS technologies are susceptible to the electrostatic discharge (ESD) events that may damage the IC products. Therefore, on-chip ESD protection circuits must be added at the RF transceiver that may be stressed by ESD, including the input/output (I/O) pads. Of course, adding ESD protection circuit causes RF performance degradation with several undesired effects. Parasitic capacitance of the ESD protection device is one of the most important design considerations for RF circuits. A typical specification for a gigahertz RF circuit on human-body-model (HBM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV and 200 fF, respectively [1].

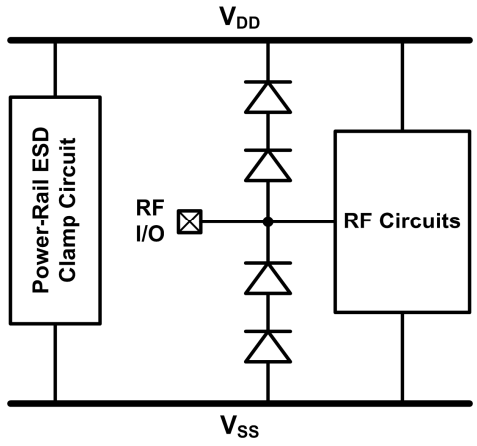

Fig. 1. ESD protection design with stacked diodes.

The conventional double-diode ESD protection scheme has been generally used for gigahertz RF circuits [2]. In order to reduce the parasitic capacitance or provide the large signal-swing tolerance, the ESD protection diodes in stacked configuration has also been presented, as shown in Fig. 1 [3]. The layout top view and the device cross-sectional view of the conventional stacked diodes are shown in Figs. 2 and 3. In Fig. 2, two STI-bound P+/N-well diodes (stacked P diodes) can apply to I/O-to-V_{DD}. In Fig. 3, two STI-bound P-well/N+ diodes (stacked N diodes) can apply to V_{SS}-to-I/O. However, the stacked configuration is adverse to ESD protection because the overall turn-on resistance and the clamping voltage of the stacked diodes during ESD stresses are increased as well. Therefore, a novel stacked diodes to improve ESD robustness is needed for RF applications.

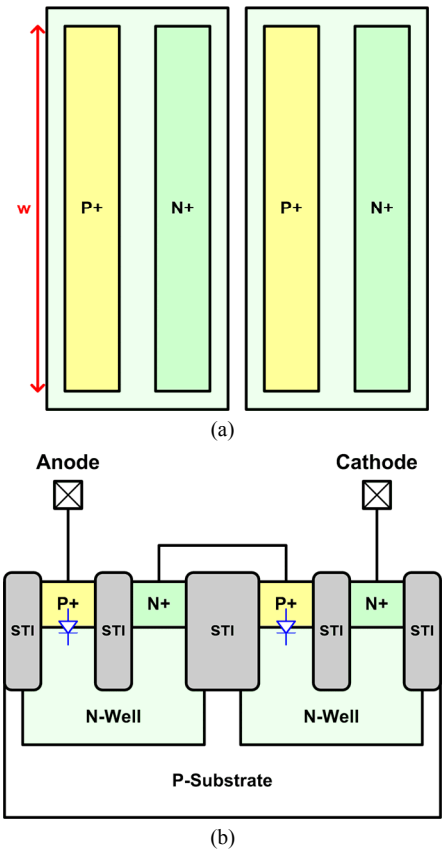

Fig. 2. (a) Layout top view, and (b) cross-sectional view, of conventional stacked P diodes.

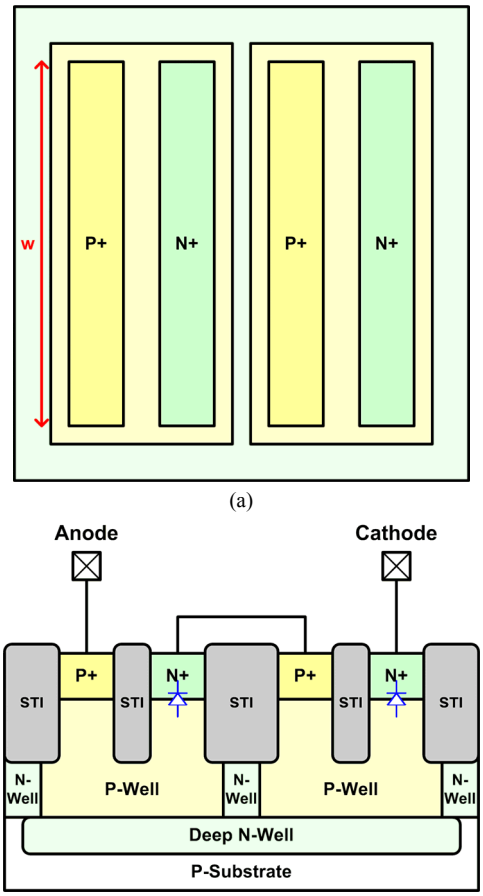

Fig. 3. (a) Layout top view, and (b) cross-sectional view, of conventional stacked N diodes.

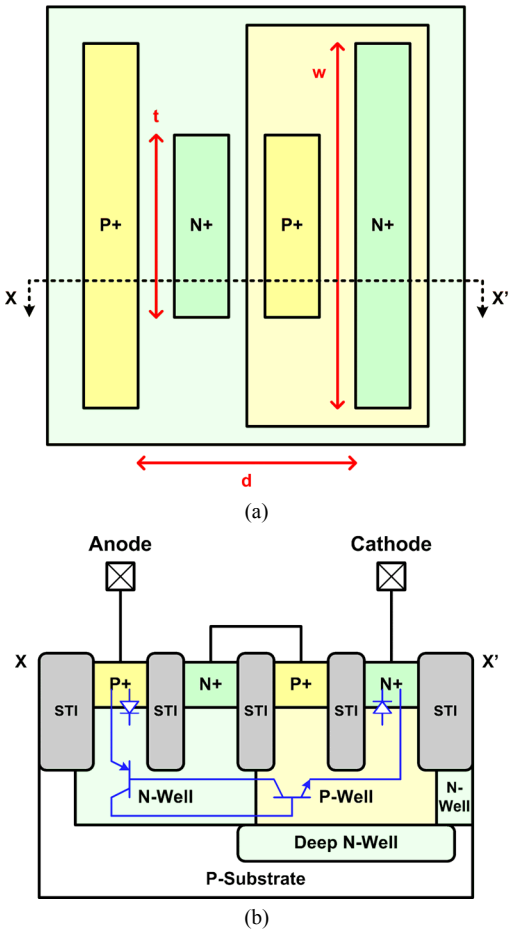

Fig. 4. (a) Layout top view, and (b) cross-sectional view, of proposed stacked diodes with embedded SCR.

II. Stacked Diodes with Embedded SCR

The silicon-controlled rectifier (SCR) device has been reported to be useful for ESD protection with low turn-on resistance, low parasitic effects, and high ESD robustness [4]. The equivalent circuit of the SCR consists of a PNP BJT and an NPN BJT. As ESD zapping, the positive-feedback regenerative mechanism of the PNP and the NPN results in the SCR device highly conductive to make SCR very robust against ESD stresses. A novel design of stacked diodes with embedded SCR is presented for effective on-chip RF ESD protection.

The proposed stacked diodes with embedded SCR is illustrated in Fig. 4. Fig. 4(a) shows the layout top view of the proposed design, and Fig. 4(b) shows the device cross-sectional view. In this design, one diode is realized by P+/N-well, and the other is realized by P-well/N+. The embedded SCR consists of P+, N-well, P-well, and N+. The deep N-well structure is used to isolate the P-well region from the common P-substrate. This stacked diodes with embedded SCR can apply to I/O-to-V_{DD} or V_{SS}-to-I/O. In the beginning of ESD stress, the stacked diodes will turn on to discharge the initial current, and then the embedded SCR will take over to discharge the primary current. The stacked diodes also play the role of trigger circuit of SCR, because the current drawn from N-well (injected into P-well) can also trigger the PNP (NPN) of SCR.

III. Experimental Results

The test devices have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. The widths of the test devices (w) are arranged as 20μm, 30μm, and 40μm. The dimensions of the center diffusions (t) are equal to w or w/4. The anode-to-cathode distance is selected to 1.02μm.

For comparison purpose, the stacked P and N diodes, as shown in Figs. 2 and 3, are also implemented in the same 65-nm salicided CMOS process.

All dimensions of test devices are listed in Table I. To facilitate two-port measurement on a probe station, all test devices are arranged with ground-signal-ground (G-S-G) pads.

A. Parasitic Capacitance

With the on-wafer measurement, the two-port S-parameters of the test devices are measured by using the vector network analyzer. In order to extract the intrinsic characteristics of the test devices in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the de-embedding technique [5]. The parasitic capacitance of each test device can be extracted from the S-parameters. Figs. 5 and 6 show the extracted parasitic capacitances of the test devices from 1 to 20 GHz. The intrinsic parasitic capacitances of the proposed designs with w=20μm/30μm/40μm are about 18fF/28fF/37fF.

Table I. Device dimensions and measurement results of test devices.

Test Device	Type	w (μm)	t (μm)	d (μm)	C (fF)	HBM (kV)	TLP V_{t1} (V)	TLP R_{on} (Ω)	TLP I_{CP} (A)	vf-TLP I_{CP} (A)	HBM / C (V/fF)	TLP R_{on} × C (Ω×fF)
A20	Proposed Design	20	5	1.02	17.9	1	1.65	2.9	0.66	1.59	55.9	51.9
B20			20		18.7	1	1.64	3.6	0.68	1.63	53.5	67.3
A30		30	7.5		27.3	1.5	1.63	2.2	1.01	2.33	54.9	60.1
B30			30		28.6	1.5	1.62	2.6	1.09	2.26	52.4	74.4
A40		40	10		36.2	2	1.62	1.2	1.35	3.01	55.2	43.4
B40			40		37.8	2	1.62	1.5	1.26	3.09	52.9	56.7
P20	Stacked P Diodes	20	N/A	N/A	14.7	0.75	1.64	7.1	0.49	1.33	51.0	104.4
P40		40			28.9	1.5	1.61	3.0	0.91	2.59	51.9	86.7
N20	Stacked N Diodes	20			18.0	0.75	1.65	7.4	0.46	1.28	41.7	133.2
N40		40			36.3	1.5	1.61	3.1	0.90	2.19	41.3	112.5

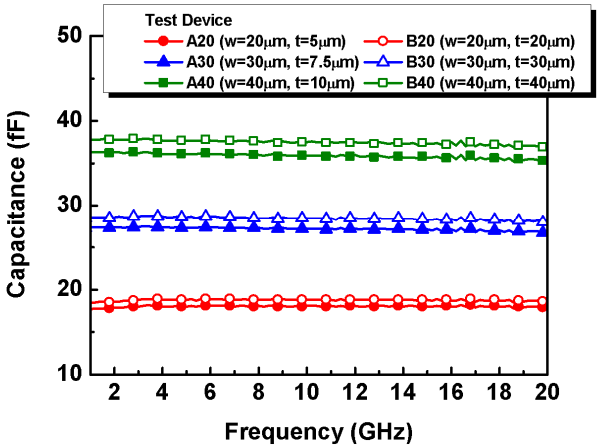

Fig. 5. Measured parasitic capacitances of proposed stacked diodes with embedded SCR.

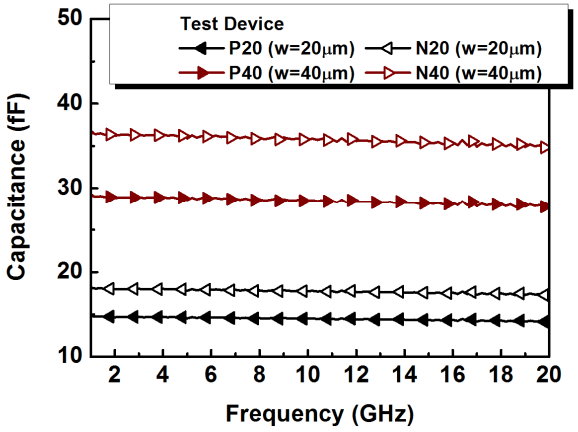

Fig. 6. Measured parasitic capacitances of conventional stacked diodes.

B. ESD Robustness

The HBM ESD robustness of the test devices are evaluated by the ESD tester. All these experimental results of test devices are listed in Table I. The proposed designs with w=40μm are improved to achieve 2kV HBM.

C. TLP and vf-TLP I-V Characteristics

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the ESD protection devices, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used. The TLP-measured I-V characteristics are shown in Figs. 7~9. The trigger voltages (V_{t1}) of all test devices are about 1.6V. Due to the assistance of embedded SCR, the turn-on resistances (R_{on}) of the proposed designs are significantly reduced. The TLP-measured current compression point (I_{CP}), which is defined as the current level deviates from the linearly extrapolated low-current curve by 20% [6], of the proposed designs with w=20μm/30μm/40μm are about 0.7A/1.1A/1.3A. The I_{CP} of the proposed designs are improved, as compared with those of the traditional stacked diodes.

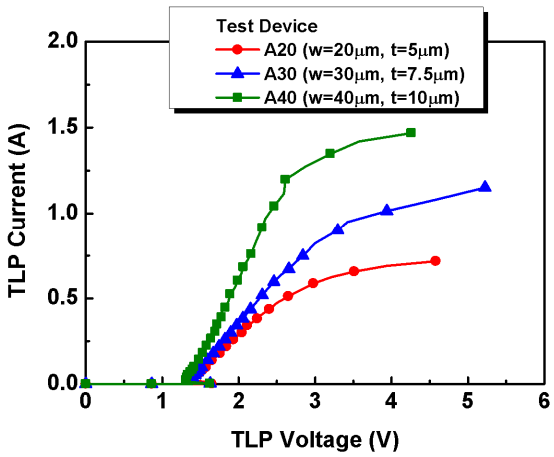

Fig. 7. TLP-measured I-V characteristics of proposed stacked diodes with embedded SCR (t=w/4).

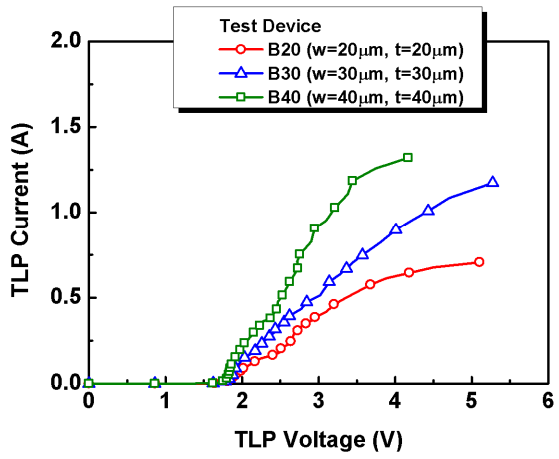

Fig. 8. TLP-measured I-V characteristics of proposed stacked diodes with embedded SCR (t=w).

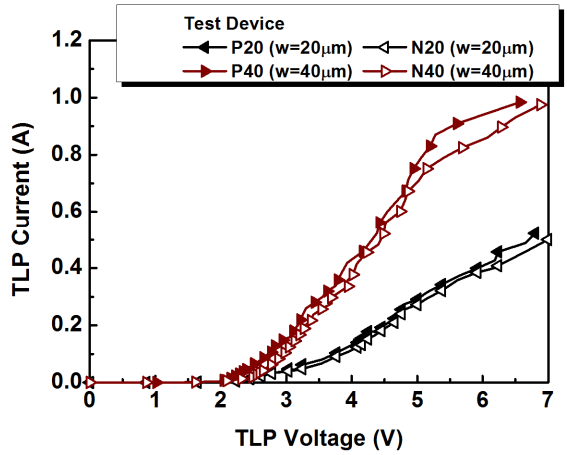

Fig. 9. TLP-measured I-V characteristics of conventional stacked diodes.

Another very-fast-TLP (vf-TLP) system is used to measure the I-V characteristics of the test devices in faster ESD-transient events. The vf-TLP-measured I_{CP} of test devices are listed in Table I. The proposed stacked diodes with embedded SCR is fast enough to be turned on under such a fast-transient pulse to improve the ESD robustness.

D. Comparison

The ratios of HBM ESD robustness and parasitic capacitance (HBM/C) of the test devices are compared, as shown in Table I. The HBM/C ratios of the proposed design are increased, as compared with those of the conventional stacked diodes. The products of turn-on resistance and parasitic capacitance (TLP R_{on} × C) of the test devices are also compared, as shown in Table I. The products of the proposed design are significantly reduced, as compared with those of the conventional stacked diodes. Therefore, the proposed stacked diodes with embedded SCR are more suitable for ESD protection due to its low turn-on resistance, low parasitic capacitance, and high ESD robustness.

IV. Conclusion

The novel stacked diodes with embedded SCR have been designed, fabricated, and characterized in a 65-nm CMOS process. Experimental results show that the proposed stacked diodes with embedded SCR can improve the ESD robustness, decrease the turn-on resistance, and lessen the parasitic capacitance. Therefore, the proposed design is more suitable for RF ESD protection.

Acknowledgments

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