Study on ESD Protection Design with Stacked Low-Voltage Devices for High-Voltage Applications

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***Abstract*—ESD protection with stacked low-voltage (LV) devices are proposed to form an area-efficient design for high-voltage (HV) applications in a 0.25-μm HV BCD process. By using the stacked configuration, the LV devices can provide scalable triggering voltage (V_{t1}) and holding voltage (V_h) for various HV applications. Experimental results in silicon chip have verified that the stacked LV devices can exhibit a higher ESD robustness per unit layout area as comparing to the ESD clamp circuit with HV device.**

I. Introduction

On-chip electrostatic discharge (ESD) protection design in smart power technology is a challenging issue due to high supply voltage and multiple doped layers in high-voltage (HV) processes [1]. In order to protect the internal circuits against ESD damage, HV ESD protection devices are applied to all input/output (I/O), power (V_{CC}/V_{SS}) and switch (SW) pads. To get sufficient ESD robustness, such HV devices were often fabricated with a large silicon area to meet the industry standards [2], [3]. By using the stacked configuration, low-voltage (LV) devices can be an area-efficient design with scalable trigger voltage (V_{t1}) and holding voltage (V_h) for various HV applications. In this work, experimental results in a 0.25-μm HV BCD process have verified that the stacked LV devices can provide a higher ESD robustness per unit layout area as comparing to the traditional RC-based ESD clamp circuit with HV device.

II. ESD Protection Design

A. RC-based ESD Clamp Circuit with HV Device

The circuit diagram of traditional RC-based ESD clamp circuit is shown in Fig. 1, where the device dimensions in RC-based ESD-transient detection circuit were chosen as R1 = 100 kΩ, C1 = 1 pF, W/L of HV-PMOS = 200 μm /0.4 μm, and R2 = 20 kΩ. The capacitor of C1 was realized by the metal-oxide-metal (MOM) capacitor with thick oxide between metal1 and metal2 layers that is required for the high breakdown voltage to sustain high operating voltage (V_{CC}) under normal circuit operation [4]. The RC time constant in the ESD-transient detection circuit was designed around ~0.1μs in this work to distinguish the ESD transient event from the power-on transition. The W/L of HV-NMOS with minimum spacing in layout design was drawn as 400 μm /0.7 μm, 800 μm /0.7 μm, and 1600 μm /0.7 μm, respectively, for the comparison of experiment results.

B. LV Devices with Stacked Configuration

The stacked configurations with LV-NMOS and LV-PMOS are shown in Fig. 2(a) and 2(b), respectively. The device dimensions were chosen as W/L of HV-NMOS = 800 μm /0.5 μm and HV-PMOS = 800 μm /0.5 μm with minimum spacing, where the HV N-well and N-buried layer (NBL) were used to isolate the bias between each device and bulk. All devices were in off state and stacked with different stacking numbers of 1, 2, and 4, respectively, for the comparison of experiment results. Such LV devices were fabricated with 5-V standard devices in a 0.25-μm HV BCD process.

III. Experimental Results

The TLP *I-V* characteristics of the ESD clamp circuit with HV-NMOS under positive ESD stress from V_{CC} line to V_{SS} are shown in Fig. 3. The TLP-measured failure current (I_{t2}) with HV-NMOS widths of 400, 800, and 1600 μm are 0.19, 0.41, and 0.8 A, respectively. Fig. 4 and 5 show the TLP-measured results of stacked LV-NMOS and LV-PMOS with different stacked numbers, respectively. All LV-NMOS were failed to enter snapback and showed extremely low failure current. On the contrary, the experimental results of stacked LV-PMOS showed the increased triggering voltage (V_{t1}) and holding voltage (V_h) with different stacked numbers and exhibited high failure current greater than 1.5 A. In addition, the breakdown voltage of each LV device was ~9V, and it was increased to ~36V with 4 stacked LV devices.

The human-body-model (HBM) ESD levels of the different ESD protection designs are listed in Table I. From the measurement results, the 4 stacked LV-PMOS showed the highest HBM level per unit layout area, and the 4 stacked LV-NMOS showed the worst. The reason can be found by SEM pictures, as shown in Fig. 6 and 7. The ESD failure locations imply that LV-NMOS suffered the non-uniform turn-on phenomenon seriously, which was caused by strong current crowding effect due to use of minimum spacing in layout design [5]. On the contrary, LV-PMOS with no snapback was turned on uniformly and exhibited an excellent ESD robustness.

IV. Conclusion

HV ESD protection design by using stacked LV devices has been proposed in a 0.25-μm HV BCD process. With the stacked configuration, the LV PMOS devices can be used as an area-efficient ESD protection design to fit different ESD protection windows for various HV applications.

Acknowledgement

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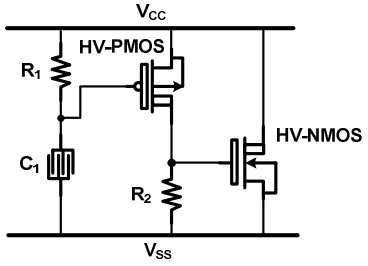

Fig. 1. The RC-based ESD clamp circuit with HV NMOS in a 0.25μm high-voltage BCD process.

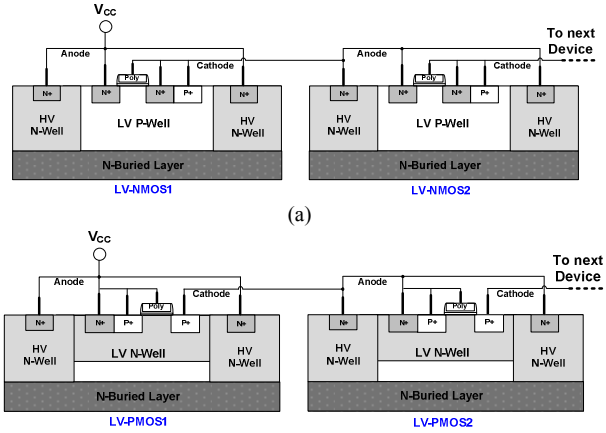

Fig. 2. The cross-sectional view of (a) stacked LV-NMOS, and (b) stacked LV-PMOS, with each device surrounded by N-buried layer in a 0.25μm high-voltage BCD process.

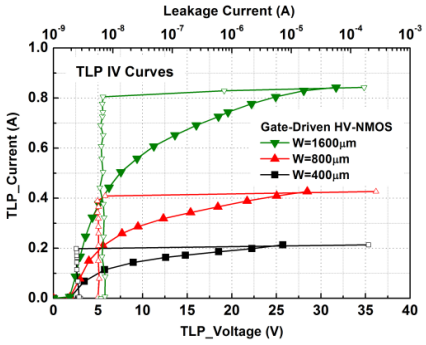

Fig. 3. TLP *I-V* characteristics of RC-based ESD clamp circuit with different HV-NMOS channel widths of 400, 800, and 1600 μm.

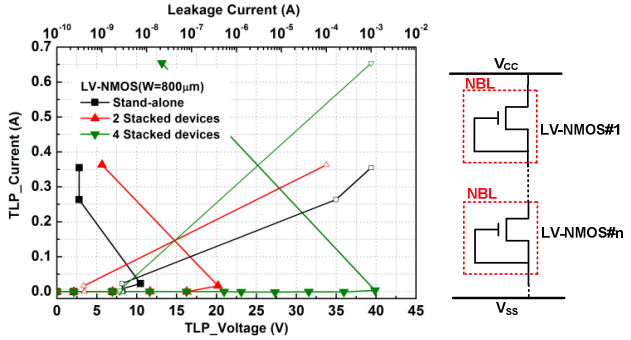

Fig. 4. TLP *I-V* characteristics of stacked LV-NMOS with different stacking numbers of 1, 2, and 4.

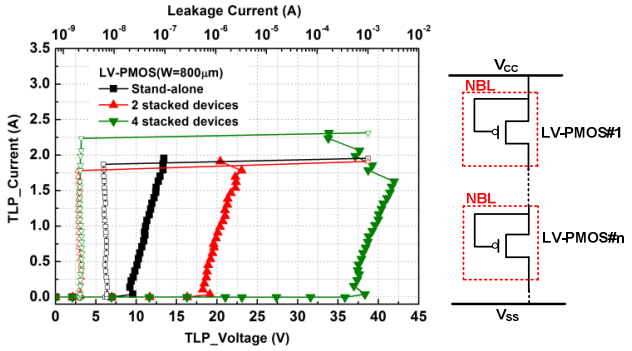

Fig. 5. TLP *I-V* characteristics of stacked LV-PMOS with different stacking numbers of 1, 2, and 4.

TABLE I
COMPARISON OF ESD ROBUSTNESS AMONG THE ESD PROTECTION DESIGNS

Types	W/L(μm) of each MOS	Layout Area (μm^2)	HBM(V)	HBM per unit Layout Area ($V/\mu m^2$)
HV-NMOS (with RC-based ESD Circuit)	400	122.84x143.72	300	0.017
	800	122.84x171.42	600	0.028
	1600	122.84x227.72	1300	0.046
4 Stacked LV-NMOS	800	107.16x114.84	200	0.016
4 Stacked LV-PMOS	800	107.16x114.84	2400	0.195

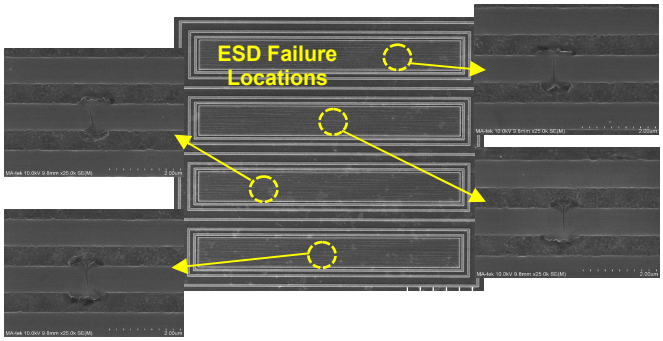

Fig. 6. The SEM picture of 4 stacked LV-NMOS after 400-V HBM ESD stress.

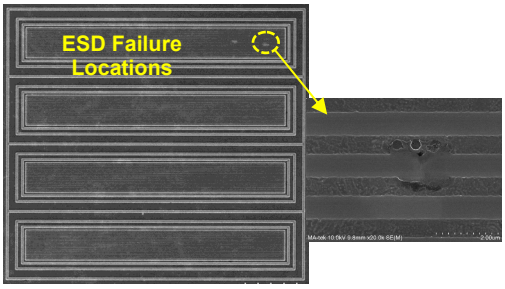

Fig. 7. The SEM picture of 4 stacked LV-PMOS after 2500-V HBM ESD stress.