A High-Voltage-Tolerant Stimulator Realized in the Low-Voltage CMOS Process for Cochlear Implant

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***Abstract* — A biomedical stimulator with four high-voltage-tolerant output channels, combined with on-chip positive high voltage generator, is proposed. For the purpose of integration with other circuit blocks into a system-on-chip (SoC) for cochlear implant biomedical applications, this design has been realized with the 1.8-V/3.3-V transistors in a 0.18-µm CMOS process. This stimulator only needs one single supply voltage of 1.8 V, but the maximum stimulation voltage can be as high as 7 V. The dynamic bias technique and stacked MOS configuration are used to implement this stimulator in the low-voltage CMOS process, without causing the issues of electrical overstress and gate-oxide reliability during circuit operation.**

I. INTRODUCTION

System-on-chips (SoC) for medical applications, such as retinal prosthesis [1] and epileptic seizure controller [2], had been proposed to implant into human body. The cochlear implant system is also one kind of medical applications for the profound deafness [3]. Cochlear implant system is based on stimulating surviving auditory nerve in the inner ear to restore the hearing of deaf persons [4]. The cochlear implant SoC for implanting into the human ear is illustrated in Fig. 1. The output from the stimulator is requested to provide adjustable high voltage to the electrodes those are implanted into the cochlea. The stimulator of the cochlear implant system may have a single channel or multiple channels, monopolar or bipolar stimulation, monophasic or biphasic pulse, and constant-current mode or constant-voltage mode [1], [5]. The well-developed CMOS processes had been attractive to realize the implantable device for biomedical electronic applications. When the operation voltage of the stimulator is higher than the device normal operating voltage of a low-voltage CMOS process, the stimulator was usually implemented in the high-voltage CMOS process [6].

From the biomedical application in our cochlear implant project, a stimulator with four-channel outputs in bipolar fashion, biphasic pulse, and constant-voltage mode is requested. According to the request of our biomedical project for cochlear implant, the required maximum voltage for stimulation is as high as 7 V. For SoC integration purpose, the other circuit blocks including data converter, DSP processor, and filters in the implant SoC device are all designed and realized in low-voltage CMOS process to reduce power consumption. So, the stimulator combined with high voltage generator implemented in low-voltage CMOS process is needed [7].

Before any human test, the animal test to verify the function of SoC chip should be performed in advance. To design a power efficient output stage, the loading impedance of the specified biomedical application should be investigated first. So, the impedance of the cochlea of guinea pig was measured with the implanted electrodes, as that shown in Fig. 2(a). According to the measured impedance, the circuit model of the implanted electrodes with the cochlea has been calculated as that shown in Fig. 2(b). In this work, the stimulator with four-channel outputs is developed to drive the cochlea via the implanted electrodes, and it is implemented in a 0.18-µm 1.8-V/3.3-V CMOS process.

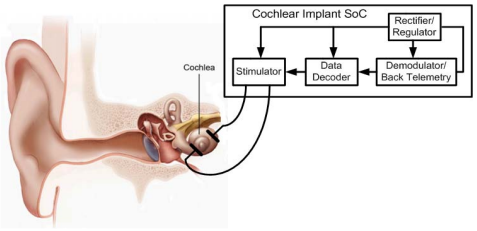
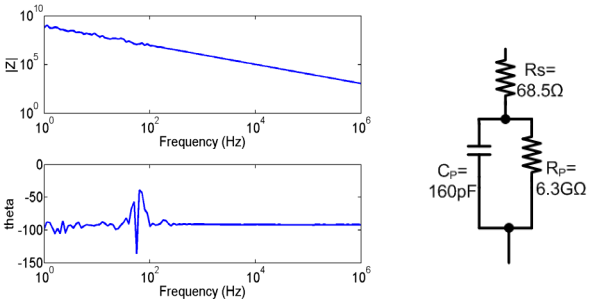
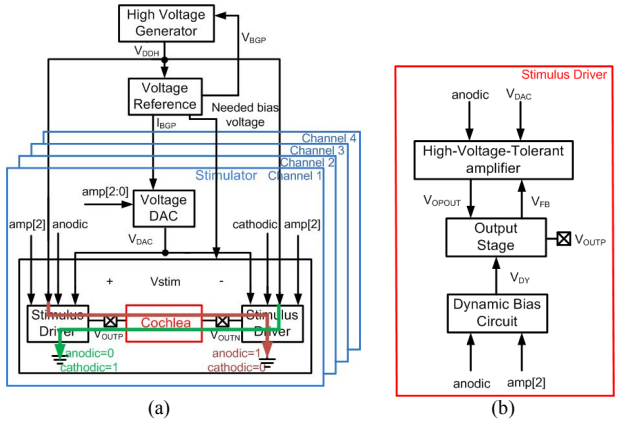


Fig. 1. An implanted SoC with stimulator to stimulate the cochlea of human.



(a) (b)

Fig. 2. (a) The measured impedance, and (b) the equivalent circuit model, of the cochlea with the implanted electrodes from animal test.



(a) (b)

Fig. 3. (a) Architecture of the whole stimulation system. (b) Circuit block of stimulus driver in the stimulator. In each channel, one pair of stimulus drivers is used to provide the stimulus voltage (Vstim) across the cochlea.

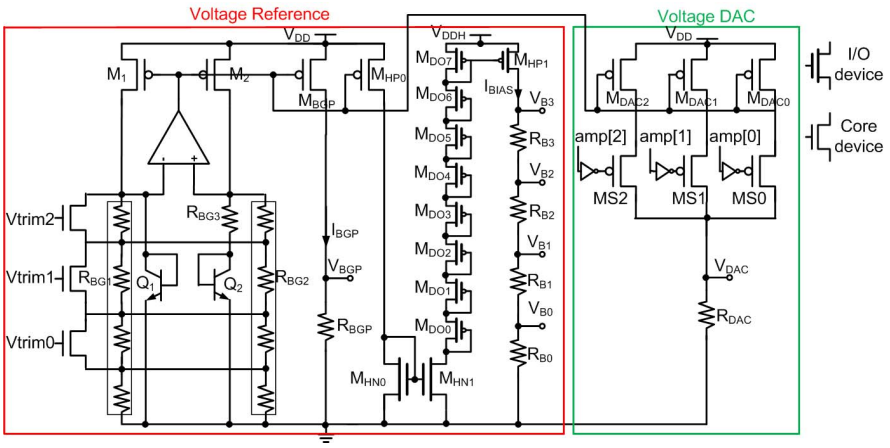


Fig. 4. Voltage reference and voltage DAC used in the proposed stimulator.

II. THE PROPOSED DESIGN

The proposed stimulator consists of four-channel outputs, a voltage reference, and a high voltage generator, as shown in Fig. 3(a). This design needs only one supply voltage V_{DD} (1.8 V), and the high voltage generator is used to pump V_{DD} to V_{DDH} (8.4 V) for the stimulus output. The voltage reference provides the desired reference voltages for the high voltage generator and stimulator. The stimulus driver can deliver the stimulus voltage (Vstim) to the cochlea according to the control signals (anodic / cathodic), where the Vstim is defined as V_{OUTP} - V_{OUTN}. In this design, the bulk voltages of all the MOS transistors are connected to their source voltages.

The left stimulus driver in Fig. 3(a) is the same as the right stimulus driver, the difference between them is only the control signal "anodic" and output node "V_{OUTP}" are changed to "cathodic" and "V_{OUTN}". The circuit block of stimulus driver in the stimulator is shown in Fig. 3(b). Each channel in the stimulator consists of two stimulus drivers and a voltage DAC. A 3-bit signal (amp) is used to control the amplitude of Vstim, and the anodic and cathodic signals are used to control the polarity and pulse width of Vstim. When anodic is logic 1 and cathodic is logic 0, the left stimulus driver in Fig. 3(a) will deliver a voltage pulse at V_{OUTP} node; as well as the V_{OUTN} node will be connected to ground by the right stimulus driver, so the Vsitm is with a positive polarity. When anodic is logic 0 and cathodic is logic 1, the right stimulus driver will deliver a voltage pulse at V_{OUTN} and V_{OUTP} will be shorted to ground, so the Vsitm is with a negative polarity. Through the control of anodic and cathodic signals to reach the biphasic stimulation, the negative voltage source was not needed in this design.

A. Voltage Reference and Voltage DAC

The voltage reference shown in Fig. 4 is modified from [8]. The voltage reference can generate a current I_{BGP} inversely proportional to the R_{BG2}, and this current is not sensitive to the process variation, supply voltage, and temperature. V_{BGP} is generated by I_{BGP} flowing through R_{BGP}, so it is only affected by the relative mismatch between R_{BG2} and R_{BGP}. V_{BGP} can be adjusted by 3-bit Vtrim signal, and V_{BGP} is used as the reference voltage for the high voltage generator to regulate its output voltage V_{DDH}.

As shown in Fig. 4, the current I_{BIAS} mirrored from M_{BGP}, M_{HP0}, M_{HN0}, M_{HN1}, and M_{HP1} flowing through R_{B3}, R_{B2}, R_{B1}, and R_{B0} to generate bias voltage (V_{B3}, V_{B2}, V_{B1}, and V_{B0}) for stimulus drivers. A series of diode-connected I/O PMOS M_{DO0}~M_{D07} are used to prevent M_{HN1} from electrical overstress.

In Fig.4, the amplitude of V_{DAC} is decided by 3-bit amp signal. The relationship between 3-bit amp signal and V_{DAC} is shown in Table I.

TABLE I. RELATIONSHIP BETWEEN 3-BIT AMP SIGNALS AND V_{DAC}.

amp[2:0]	000	001	010	011	100	101	110	111
V_{DAC} (V)	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7

B. Stimulus Driver

Feedback loop is necessary for stimulus driver to deliver constant voltage across the cochlea. But the feedback loop could have the problem of stability, the poles and zeros of the loading impedance from the cochlea become important. The impedance model fits the measured impedance, which includes R_S = 68.5 Ω, R_P = 6.3 GΩ, and C_P = 160 pF, as that shown in Fig. 2(b). This impedance and the feedback resistors (R_1 and R_2 in Fig. 5) can generate one pole and one zero. This zero is located at very high frequency, so it can be neglected it. Thus, only one pole at ~1 kHz will be induced in the output stage.

When the anodic signal is logic 1, the stimulus driver shown in Fig. 5 will deliver a voltage pulse at V_{OUTP}. The NMOS current path of output stage will be turned off, and the high-voltage tolerant amplifier can force the voltage level of V_{FB} the same as V_{DAC}. The resistance of R_2 and R_1 are in 1:9 ratio, so the voltage level of V_{OUTP} is ten times of the voltage level of V_{DAC}.

When the stimulator delivers negative stimulus voltage or not in stimulation (anodic is at logic 0), V_{OUTP} should be shorted to ground and V_{OPOUT} should be shorted to V_{DDH} to turn off the PMOS current path of the output stage.

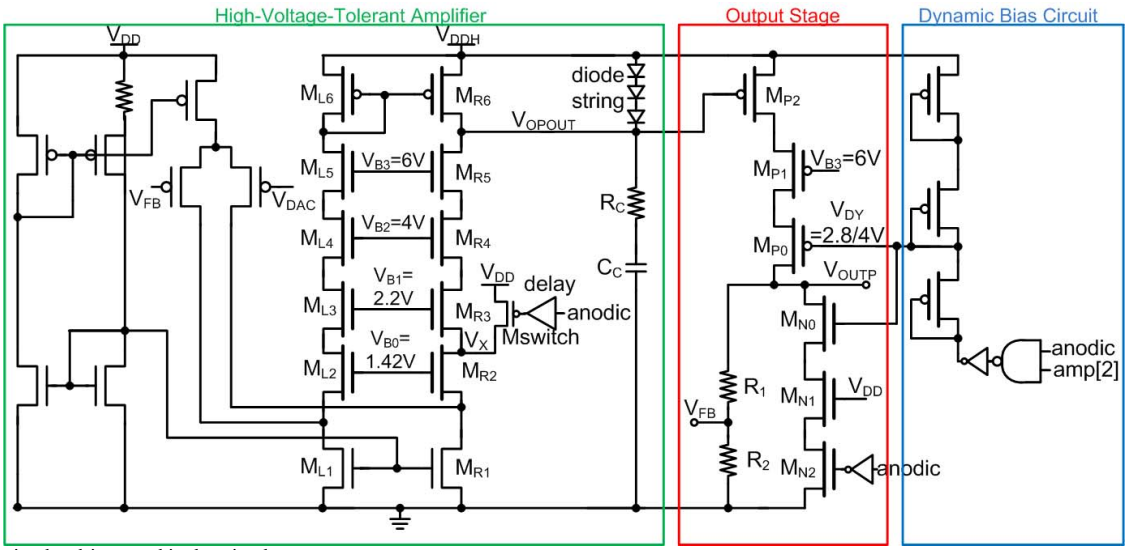


Fig. 5. The stimulus driver used in the stimulator.

When anodic is at logic 0, Mswitch will be turned on, and V_X will be shorted to V_{DD}. So, the M_{R3} is off, and $I(M_{R6})=0$. But the gate voltage of M_{R6} is biased by diode-connected MOS M_{L6}, and $I(M_{L6}) \neq 0$, V_{OPOUT} is therefore shorted to V_{DDH}.

In the output stage, stimulus driver can deliver different amplitude of voltage pulse at V_{OUTP}, according to the 3-bit amp signal and anodic signal low or high. For the purpose of preventing MOS in the output stage from electrical overstress, dynamic bias technique is needed. When V_{OUTP} is at low voltage level (< 4V), dynamic bias circuit can bias the gate voltage of M_{P0} and M_{N0} at 2.8V, so gate-to-source and drain-to-source voltage of all MOS in output stage are < 3.3V. When V_{OUTP} is at high voltage level (> 4V), dynamic bias circuit can bias gate voltage of M_{P0} and M_{N0} at 4V, so gate-to-source voltage of all MOS in output stage is < 3.3V. To keep the drain-to-source voltages of all MOS < 3.3V, source voltage of M_{P0} should be the same as its gate voltage when anodic signal is at logic 0. But when anodic signal is from logic 1 to logic 0, due to charge sharing, the source voltage of M_{P0} cannot be the same as its gate voltage V_{DY}. To solve this issue, V_{OUTP} should be shorted to ground before V_{OPOUT} shorted to V_{DDH}, so a delay in the timing operation is inserted between the anodic signal and Mswitch.

Diode string in the high-voltage tolerant amplifier is used to prevent the output stage draws large current immediately from V_{DDH}. Rc and Cc are used to generate a zero to compensate the pole at V_{OPOUT}.

C. *High Voltage Generator*

The architecture of the high voltage generator used in this work is shown in Fig. 6. A five-stage charge pump is used to pump V_{DD} to higher voltage level. For the purpose of regulating the voltage level of V_{DDH} at 8.4 V, the positive high voltage generator adopts the pulse frequency modulation (PFM) to regulate V_{DDH}. When $V_{F2} < V_{BGP}$, the frequency of clkr will arise until $V_{F2} > V_{BGP}$; and when $V_{F2} > V_{BGP}$, the frequency of clkr will decrease until $V_{F2} < V_{BGP}$. V_{F2} can be almost the same as V_{BGP}, therefore the voltage level of V_{DDH} can be regulated.

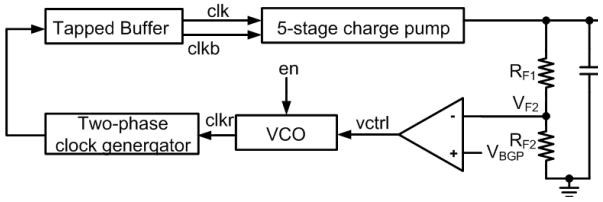


Fig. 6. Architecture of the high voltage generator.

III. Experimental Results

The proposed stimulation system has been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. The microphotograph of the fabricated chip is shown in Fig. 7. The 3-bit amp signal and pulse width of anodic and cathodic signals are used to adjust the amplitude, polarity, and pulse width of the stimulus voltage (Vstim) on the loading impedance. So, the proposed stimulator is an adjustable design that can cover some range of loading impedance.

When the 3-bit amp signal is set to 111, the pulse width of anodic signal and cathodic signal is 1 ms, and the interphase delay between anodic signal and cathodic signal is 0.25 ms. With such a control setting, the biphasic stimulus voltage waveform is measured in Fig. 8. When the 3-bit amp signal is set to 011, the pulse width of anodic signal and cathodic signal is only 100 μs, and the interphase delay between anodic signal and cathodic signal is 25 μs. Under such setting, the biphasic stimulus voltage waveform is shown in Fig. 9. As verified in Fig. 8 and Fig. 9, the pulse width and amplitude of biphasic stimulus voltage are adjustable.

Fig. 10 shows this stimulator can deliver four channels of different stimulus voltages, simultaneously. The performances of the stimulator chip are summarized in Table II.

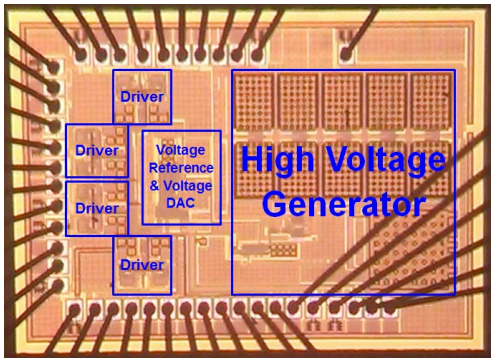


Fig. 7. The microphotograph of the fabricated stimulator chip. The die size is 1.167mm X 1.648mm realized in a 0.18-µm 1.8-V/3.3-V CMOS process.

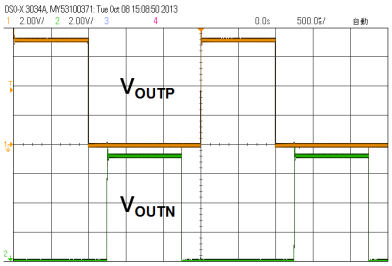


Fig. 8. When the 3-bit amp signal is set to 111, the biphasic stimulus voltage has the voltage magnitude of ± 7 V, and the pulse width controlled by the anodic and cathodic signals are set to 1 ms.

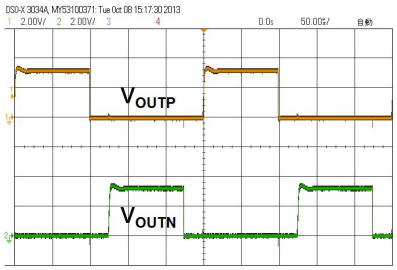


Fig. 9. When the 3-bit amp signal is set to 011, the biphasic stimulus voltage has the voltage magnitude of ± 3 V and the pulse width controlled by the anodic and cathodic signals are set to 100 µs.

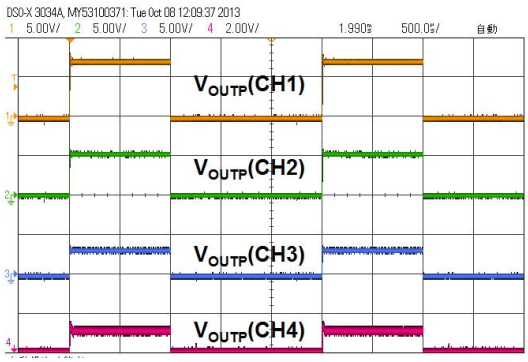


Fig. 10. The stimulator can simultaneously deliver four channels of different stimulus voltages, V_{OUTP} (7V, 5V, 3V, and 1V), under the pulse width of 1 ms.

TABLE II. SUMMARY OF THE FABRICATED STIMULATOR CHIP.

Technology	0.18-µm 1.8-V/ 3.3-V CMOS process
Output Channels	4
Supply Voltage	1.8 V
Amplitude Resolution	3 bits
Maximum Stimulus Voltage	±7V
Power consumption of each channel (±7V, 1-ms pulse width)	270 µW

IV. CONCLUSION

Design of four-channel high-voltage-tolerant stimulator combined with a high-voltage generator for cochlear implant SoC in a 0.18-µm 1.8-V/3.3-V CMOS process is proposed. The proposed design realized with 1.8-V and 3.3-V transistors can be operated up to 8.4 V without causing electrical overstress issues. This high-voltage-tolerant design will be integrated with the other circuit blocks, such as data converter and DSP processor, into a SoC chip for cochlear-implant biomedical applications. The functions of this stimulator design have been successfully verified in silicon chip, which can successfully deliver the required adjustable stimulus voltage to the output load.

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