ESD Protection Design for Wideband RF Applications in 65-nm CMOS Process

Li-Wei Chu[1], Chun-Yu Lin[2], Ming-Dou Ker[3], Ming-Hsiang Song[1], Jen-Chou Tseng[1], Chewn-Pu Jou[1], and Ming-Hsien Tsai[1]

[1] Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan
[2] Department of Applied Electronics Technology, National Taiwan Normal University, Taipei, Taiwan
[3] Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

***Abstract* — All wireless communication products must meet the reliability specifications during mass production. To prevent from electrostatic discharge (ESD) damages, the ESD protection designs must be added at all input/output pads in chip. Some ESD protection designs with low parasitic capacitance for radio-frequency (RF) applications are reviewed in this paper. Besides, a novel ESD protection design is proposed and realized in a 65nm CMOS process to protect the wideband RF circuits. In this work, diodes are used for ESD protection and inductors are used for high-frequency performance fine tuning. Experimental results of the test circuits have been successfully verified.**

***Index Terms* — Diode, ESD, radio-frequency (RF), T-coil, wideband.**

I. Introduction

Nanoscale CMOS technologies have been used to realize the high-frequency/high-speed integrated circuits. However, the transistors currently used in nanoscale CMOS technologies are vulnerable to electrostatic discharge (ESD) events. All integrated circuits used in the high-frequency/high-speed communication products need to be equipped with ESD protection designs. However, ESD protections cause high-frequency/high-speed performance degradation with several undesired effects. Parasitic capacitance is one of the most important design considerations for the integrated circuits. A typical specification for a radio-frequency (RF) circuit on human-body-model (HBM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV and 200 fF, respectively [1]. As the operating frequencies of integrated circuits increase, the parasitic capacitance was more strictly limited.

In this paper, several on-chip ESD protection designs with very low parasitic capacitance are reviewed in Section II. A new ESD protection design for wideband RF applications with good high-frequency performance and high ESD robustness is presented in Section III.

II. Conventional ESD Protection Designs with Low Parasitic Capacitance

A. ESD Protection Diodes

Fig. 1 shows the ESD protection scheme with diodes (D_{ESD}) at I/O pad and the power-rail ESD clamp circuit between V_{DD} and V_{SS} [2]. This scheme is only suitable for small ESD protection diodes because the parasitic capacitance of the ESD protection diode is directly contributed at the I/O pad.

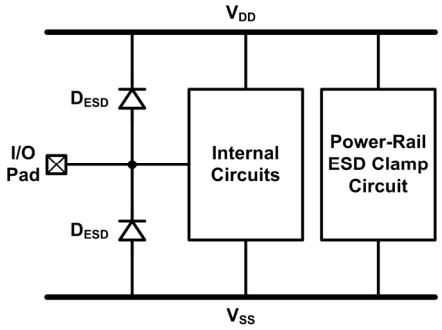

Fig. 1. ESD protection design by diodes.

B. Parallel LC Resonator

The parallel LC resonator can be realized as shown in Fig. 2 [3]. The inductor (L_{ESD}) can resonate with the parasitic capacitance of D_{ESD}. The inductor also serves as an ESD protection device between I/O pad and V_{DD}. The placement of the inductor and the ESD protection diode can be interchanged to provide the same function. Since the inductor is dc short, a dc blocking capacitor (C_{block}) is required to provide a separated dc bias for the internal circuits.

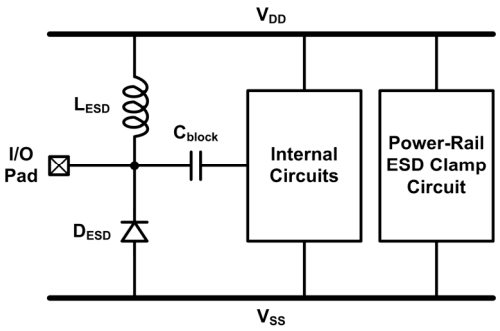

Fig. 2. ESD protection design by parallel LC resonator.

C. ESD Protection Inductor

ESD protection design for RF circuits by using inductor as the ESD protection device had been reported, as shown in Fig. 3 [4]. Since the frequency component of ESD current is much lower than that of the RF signal, the inductor can pass the ESD current while block the RF signal. Besides, a dc blocking capacitor is needed to provide a separated dc bias for the internal circuits.

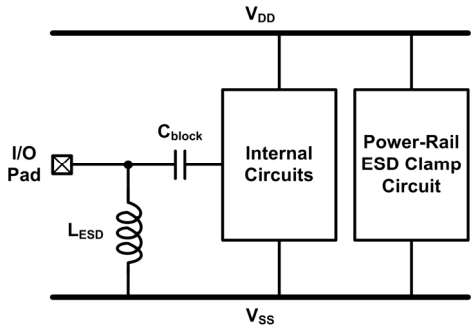

Fig. 3. ESD protection design by inductor.

D. Series LC Resonator

ESD protection design utilizing the series LC resonator is shown in Fig. 4 [5]. At high frequencies, the L_{ESD} dominates the impedance of the series resonator. Thus, wideband ESD protection can be achieved by designing the application band of the series LC resonator to cover the frequency band of the RF signal. During ESD stresses, the ESD current can be discharged through the L_{ESD} and D_{ESD}. However, the transient voltage across the series L_{ESD} and D_{ESD} should be reduced to improve the ESD robustness.

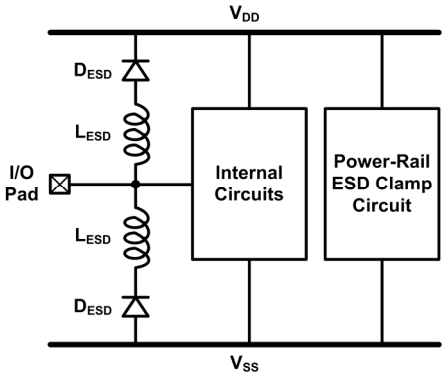

Fig. 4. ESD protection design by series LC resonator.

E. LC-Tank

As shown in Fig. 5, a pair of the LC-tanks is placed at the I/O pad [6]. At the resonant frequency of the LC-tank, there is ideally infinite impedance from the signal path to the ESD protection diodes. Consequently, the parasitic capacitances of the ESD protection diodes are isolated, which can mitigate the parasitic effects of ESD diodes.

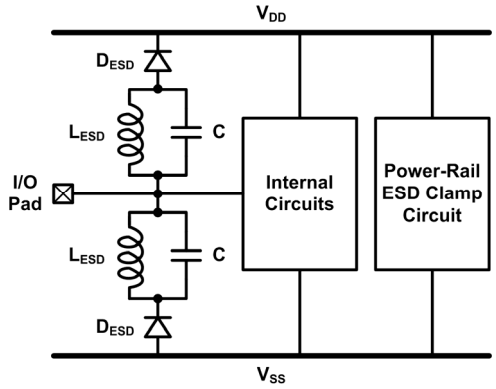

Fig. 5. ESD protection design by LC-tank.

F. Modified LC-Tank

Fig. 6 shows the circuit design of modified LC-tank ESD protection [7]. The series LC is designed to resonate at low frequency. At the frequency above the resonant frequency, the inductance dominates the impedance of the series LC, and then the inductance can eliminate the parasitic capacitance of ESD diodes.

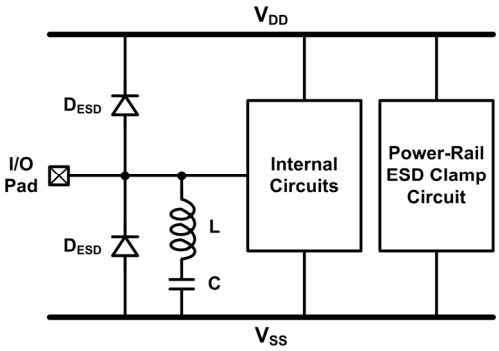

Fig. 6. ESD protection design by modified LC-tank.

G. Distributed ESD Protection Diodes

The distributed ESD protection scheme had been presented, as shown in Fig. 7 [8]. With the ESD protection diodes divided into small sections and matched by the inductor, such a distributed ESD protection scheme can achieve wideband impedance matching. The number of ESD protection diodes can be varied to optimize the performance.

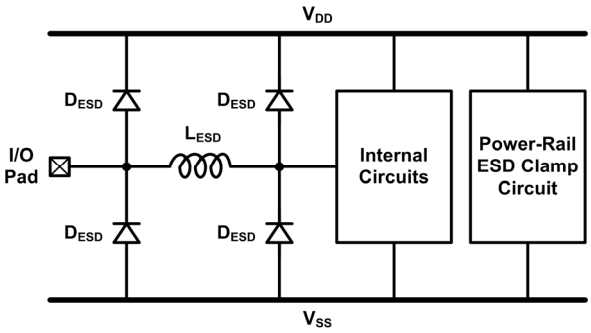

Fig. 7. Distributed ESD protection scheme.

H. T-Coil

The ESD protection design with T-coil for wideband applications had been reported [9], as shown in Fig. 8. The other T-coil-based ESD protection designs had been reported [10], [11]. With proper impedance matching design, this circuit can provide a purely resistive input impedance of R_T. However, the ESD robustness of the traditional T-coil ESD protection design can be further improved.

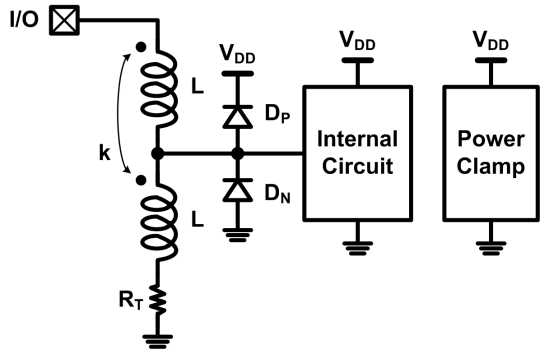

Fig. 8. T-coil with traditional ESD diodes.

III. Proposed ESD Protection Design

In this work, a robust ESD protection design for wideband RF applications is proposed in a 65nm CMOS process. Fig. 9 shows the novel design of T-coil with distributed ESD protection diodes. Such ESD protection design consists of a pair of inductors (L) with coupling factor (k), a terminate resistor (R_T), and three pairs of ESD protection diodes (D_{P1}, D_{N1}, D_{P2}, D_{N2}, D_{P3}, and D_{N3}). The distributed diodes can reduce the ESD-generated heat across each diode, and the ESD robustness can be improved. When the ESD protection diodes are under forward-biased condition, they can provide efficient discharging paths from I/O pad to V_{DD} or from V_{SS} to I/O pad. Besides, the power clamp provides the ESD current paths between V_{DD} and V_{SS}.

Suppose the parasitic capacitances of D_{P1}-D_{N1} pair, D_{P2}-D_{N2} pair and high-speed circuits, and D_{P3}-D_{N3} pair are C_1, C_2, and C_3, respectively. This design can be recognized that at low frequencies, the inductors (L) short the input to R_T, and at high frequencies, L, C_1, C_2, and C_3 are also matched by using distributed ESD protection scheme [8]. The transfer function (V_x/I_{in}) of the proposed ESD protection circuit can be calculated as Eq. (1). The sizes of inductors and ESD protection diodes can be designed to expand the bandwidth and minimize the performance degradations.

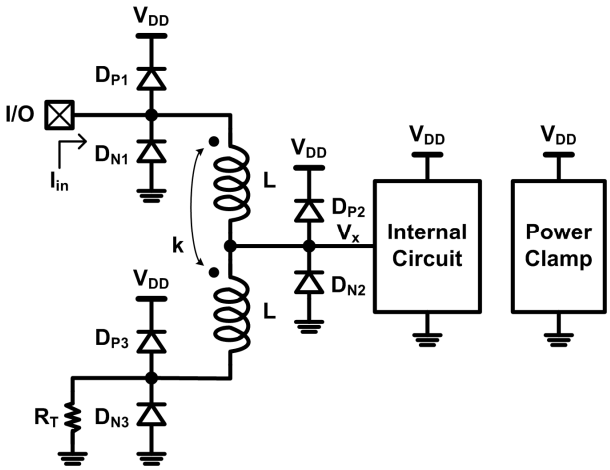

Fig. 9. Design of T-coil with distributed ESD diodes.

IV. Test Circuits

The test circuits have been implemented in a 65-nm CMOS process. In the proposed design, the width of D_{P1}, D_{P2}, and D_{P3} (D_{N1}, D_{N2}, and D_{N3}) are selected to 24μm, 12μm, and 24μm, respectively. The inductors are both ~0.23nH in the proposed design. For comparison purpose, the T-coil with traditional ESD protection diodes is also implemented. The width of D_P and D_N are selected to 60μm. The inductors are both ~0.25nH in the T-coil network. Each test circuit occupies an area of 95x85μm^2.

V. Experimental Results

A transmission-line-pulsing (TLP) system with a 10ns rise time and a 100-ns pulse width is used to evaluate the secondary breakdown current (I_{t2}), which indicated the current-handling ability in the time domain of HBM ESD event, of ESD protection circuit. Fig. 10 shows the measured TLP I-V curves of the test circuits. The T-coil with traditional and distributed ESD diodes can achieve the TLP-measured I_{t2} of 1.08A and 1.75A, respectively.

Another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1ns pulse width is also used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) event. Fig. 11 shows the measured VF-TLP I-V curves of the test circuits. The VF-TLP-measured I_{t2} of T-coil with traditional and distributed ESD diodes are 1.71A and 2.95A, respectively.

The HBM ESD robustness of the test circuits are evaluated by the ESD tester. The measured HBM ESD robustness of the T-coil with traditional and distributed ESD diodes are 1.75kV and 2.5kV, respectively. All these experimental results of test circuits are listed in Table I.

$$\frac{V_x}{I_{in\ ,\ Proposed\ design}} = \frac{R_T}{1+sC_3R_T} \times \frac{1+\frac{L(1+k)}{R_T}s+2C_BL(1+k)s^2}{1+C_2R_Ts+[2C_BL(1+k)+C_2L]s^2+2C_BC_2R_TL(1+k)s^3+C_BC_2L^2(1-k^2)s^4} // \frac{1}{sC_1} \quad (1)$$

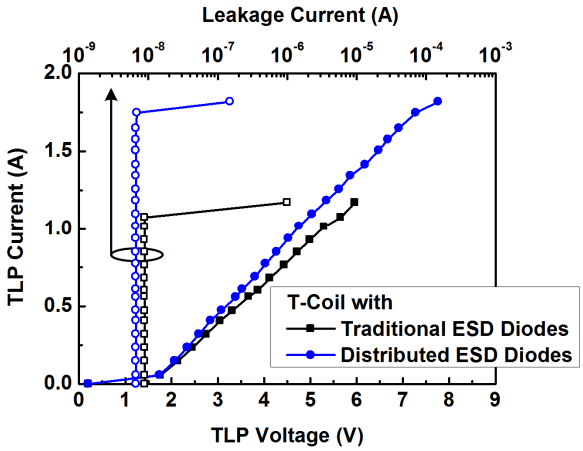

Fig. 10. TLP I-V characteristics of test circuits.

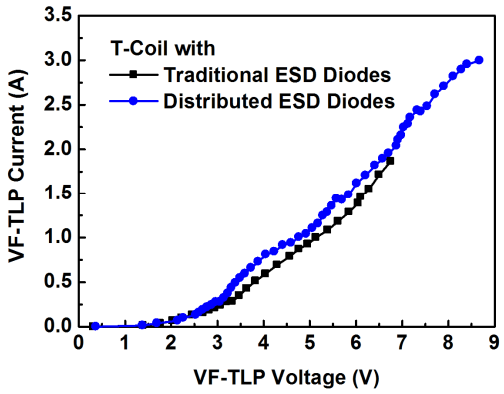

Fig. 11. VF-TLP I-V characteristics of test circuits.

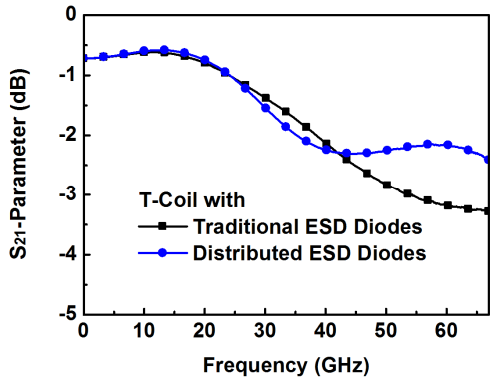

Fig. 12. S_{21}-parameters of test circuits.

Table I. Measurement results of test circuits.

	T-Coil with Traditional ESD Diodes	T-Coil with Distributed ESD Diodes
HBM ESD Robustness	1.75 kV	2.5 kV
TLP I_{t2}	1.08 A	1.75 A
VF-TLP I_{t2}	1.71 A	2.95 A

Fig. 12 shows the measured S_{21}-parameters of the T-coil with traditional and distributed ESD diodes. The S_{21}-parameters of the proposed design perform better than those of traditional design for frequencies as high as 60 GHz.

VI. Conclusion

The new ESD protection design with good high-frequency performance and high ESD robustness has been developed for wideband RF applications. The test circuits have been investigated in 65-nm CMOS process. Experimental results validate the feasibility of the new ESD protection design.

Acknowledgements

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