Power-Rail ESD Clamp Circuit with Embedded-Trigger SCR Device in a 65-nm CMOS Process

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***Abstract*— SCR is the preferred ESD protection device in nanoscale CMOS technologies due to the better area efficiency compared the BIGFET, virtually no leakage current and smaller capacitance. The main drawback of the SCR is the slow turn-on speed, which is solved by adding dummy gates to block the STI formations inside the SCR structure. This work demonstrates that the dummy gate inside the SCR can be effectively used as an embedded trigger transistor, eliminating the need of an external trigger transistor in the ESD protection circuit and so further reducing silicon area and standby leakage current.**

I. INTRODUCTION

Electrostatic Discharge (ESD) is a major reliability concern in integrated circuits [1]. ESD are fast transient waveforms that happen when two bodies with different electrostatic potential reach contact as a result of the charge balance. Such discharges may have peak voltages of several thousand volts and peak currents in the order of amperes, and may damage the internal devices of an IC. To avoid such damage, ESD protections are placed around the IO pads and the power rails to provide a safe discharge path between any pin-to-pin combination of ESD testing. A schematic representation of such ESD protection scheme is shown in Fig. 1. The ESD diodes (D_p/D_n) couple any ESD zapping between two IO pads to the power rails (V_{DD} and V_{SS}), then the power-rail ESD clamp circuit discharges the ESD current through the power rails. Therefore, the ESD current will not flow through the internal circuits, thus avoiding ESD damage. In such a protection scheme, the power-rail ESD clamp circuit plays an important role [2].

The power-rail ESD clamp circuit consists of an ESD detection circuit and an ESD clamp. The ESD detection circuit detects the ESD event across the power rails of IC, typically using an RC delay to detect the fast rise-time characteristic of ESD, and triggers the ESD clamp, which is a device capable of manage such high currents. In the older technologies, a large sized MOSFET (called BIGFET) was used to discharge the ESD current, but in nanoscale CMOS processes due to the leakage current issue [3] they have become practically obsolete, as the leakage current through the gate results too large. The ESD detection circuit also suffers from gate leakage issue, though previous works have addressed this issue [4], [5]. The silicon-controlled-rectifier (SCR) is used as a replacement of the BIGFET. In addition, the SCR has shown to have better ESD performance than the BIGFET [6]. The SCR with the parasitic bipolar junction transistors between the P+, NW, PW, and N+ regions is shown in Fig. 2. The SCR is

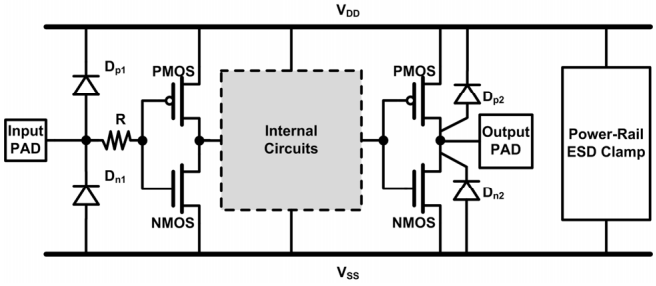

Fig. 1. Whole-chip ESD protection scheme with the power-rail ESD clamp.

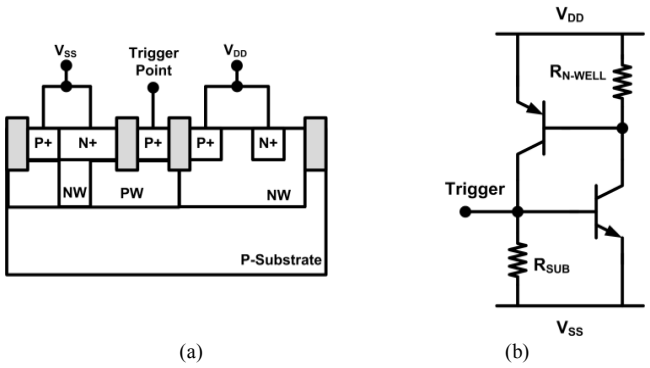

Fig. 2. (a) SCR cross-sectional view, and (b) its equivalent circuit.

triggered at the P-well with the aid of a trigger transistor controlled by the ESD detection circuit. The main drawback of the SCR is the slow turn-on speed, which can be fatal for fast ESD events. Some previous works have addressed the issue by using advanced trigger-assist techniques, such as the GGSCR [7], DTSCR [8], DGSCR [9], or ETSCR [10]. GGSCR would not be suitable for advanced CMOS processes as it depends on the breakdown junction of the NMOS, which would be higher than the gate oxide breakdown voltage of the internal devices. The DTSCR used a diode string to sink the ESD current while the SCR was triggered, but they require excessive area and may have serious leakage issue under high temperature. The DGSCR used dummy gates to block the STI formations inside the SCR structure and therefore enhance the turn-on speed. This device still requires an external trigger PMOS which adds area and leakage current to the ESD clamp circuit. The ETSCR embeds the trigger MOS into the SCR layout and uses a merged layout style to block the STI with a P+ (or N+) region, at the expense of a larger SCR path.

In this work, a new design of power-rail ESD clamp circuit with embedded-trigger SCR device is proposed and verified in

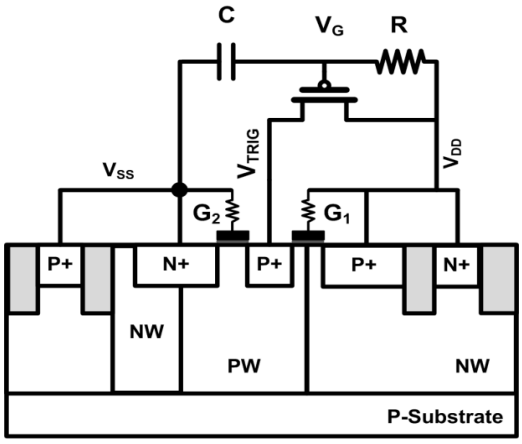

Fig. 3. Traditional SCR with dummy gates [9] using a simple ESD detection circuit.

a 65-nm CMOS process. The dummy gate of the DGSCR can be used as an embedded trigger, thus eliminating the need of an external trigger transistor. Compared to the previous works, this work can embed the trigger MOS using less area and shorter SCR path.

II. Power-Rail ESD Clamp Circuits

A. Traditional design

The DGSCR is shown in Fig. 3, including an ESD detection and trigger circuit. The STI formations in the SCR path have been blocked by using two dummy gates (G_1 and G_2). G_1 and G_2 are connected to V_{DD} and V_{SS}, respectively, through protection resistors to avoid ESD damage in these gates. Under an ESD zapping at V_{DD}, the RC delay cannot follow up the fast rise time of the ESD event, so the voltage drop across the resistor R turns the PMOS on, which sends the trigger current into the trigger pint to turn SCR on. Under normal circuit operation, the PMOS is kept off and the trigger point is biased at V_{SS} through the substrate resistance. Simulation results of the traditional design under the ESD-stress condition and power-on transition are shown in Fig. 4.

The dummy gate G_1 has the particularity that half of its substrate is P-type and half of the substrate is N-type. Under normal circuit operation, V_{TRIG} is driven to the stable V_{SS} voltage, the N-well is also tied to V_{DD}, and the P-well is tied to V_{SS}. The voltage at G_1 is biased at V_{DD}. The equivalent structure can be described as a diode connected between V_{DD} and the P-well, which is in reverse connection so no conduction will happen in this case, as expected. If G_1 were connected to a lower potential (V_{SS} for example) instead of V_{DD}, the voltage across G_1 and N-well would cause a P-channel to form in the N-well and connect the right P+ region with the P-well. In this case, a current would flow through said P-channel, causing some current conduction to trigger SCR on for ESD protection. The equivalent structure for this case could be described as a resistor connected between V_{DD} and the P-well. These effects depicted with the SCR device structures and the equivalent circuits are shown in Fig. 5.

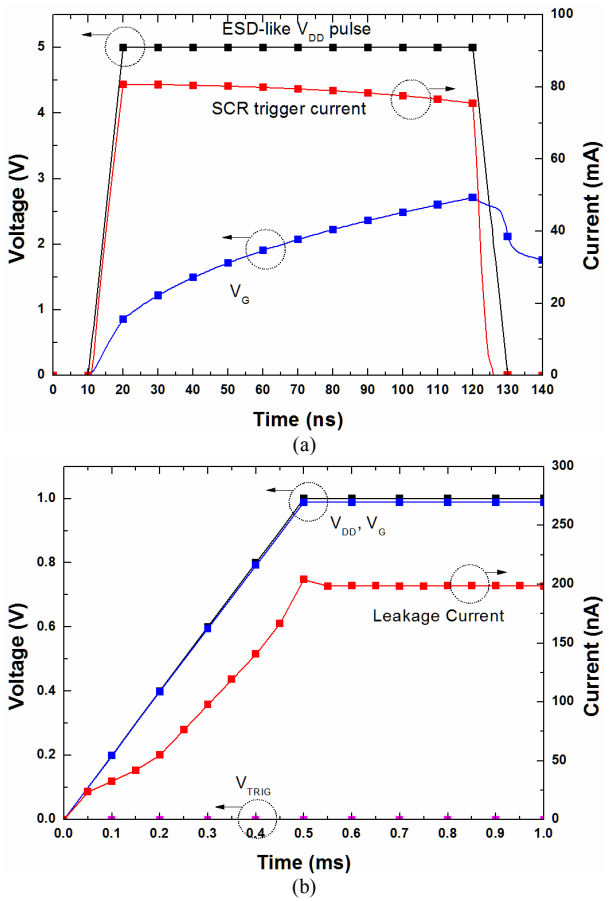

Fig. 4. Simulation results for the traditional power-rail ESD clamp circuit, using a time constant of 100ns and a PMOS trigger with size W/L=100µm/120nm. The substrate resistance is simulated with a 50Ω resistor. (a) Simulation under ESD-like event; and (b) simulation under power-on event.

B. Proposed power-rail ESD clamp circuit

The particular behaviour of G_1 can be used to trigger the SCR by actively controlling its voltage. Instead of tying G_1 to V_{DD} as reported in [9], it is directly connected to the ESD detection circuit, thus eliminating the external trigger transistor. The proposed circuit is shown in Fig 6. Under normal circuit operation, V_{TRIG} is driven to V_{DD} though the resistor R, and the circuit behaves as that in Fig. 5(a). Under a positive ESD zapping at V_{DD}, V_{TRIG} raises much slower than V_{DD} due to the larger RC time constant. This voltage drop causes a P-channel to appear in the N-well and connect the P+ region tied to V_{DD} with the P-well, as that in Fig. 5(b). The current through the P-well causes the SCR to be triggered on and clamp V_{DD} to the SCR holding voltage, thus providing the desired ESD protection function to the internal circuits of IC.

The proposed circuit has been versified via silicon chip in a 65-nm CMOS process. The DGSCRs shown in Fig. 3 and Fig. 6 are designed with the same structure and dimensions of 40µm x 7µm for performance comparison. The dummy gates are drawn with the gate oxide of core devices. The RC time constant is designed as 100ns, by using a thick-oxide PMOS to realize the capacitor (C) to avoid leakage issue. The trigger

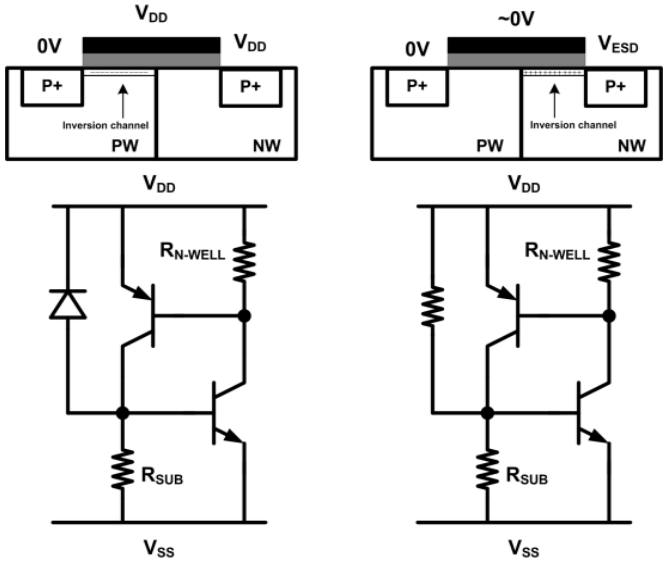

Fig. 5. Representation of G1 operation modes. (a) The operation under normal circuit operation and the equivalent circuit. (b) The operation under ESD event and the equivalent circuit. The N+ pick up of the N-wells have been omitted for clarity, and are connected as that shown in Fig. 3.

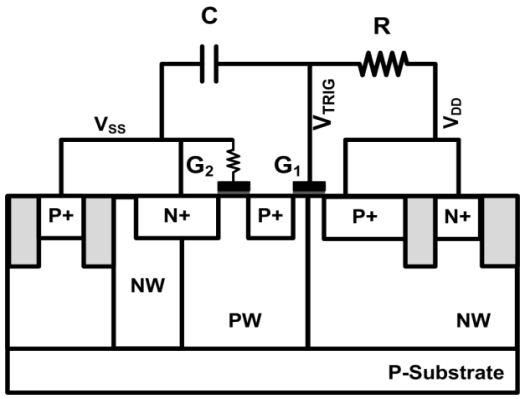

Fig. 6. Proposed SCR using the embedded trigger transistor.

PMOS transistor used in the traditional design of Fig. 3 is sized as W/L=100μm/120nm.

III. Measurement Results

A. Leakage Current Measurement

Leakage current was measured on die under different DC bias voltages with controlled temperatures, and the measured results are shown in Fig. 7. The leakage current of the traditional design is 116nA at 25 ºC and 931nA at 125 ºC under 1-V bias. The leakage current of the proposed design is 24nA at 25 ºC and 83nA at 125 ºC under 1-V bias. The traditional design has higher leakage current at both low and high temperatures. At low temperature, the dominant leakage is due to gate tunnelling, whereas for high temperature the leakage current is mainly due to junction leakage. For both cases, the cause of the larger leakage current is due to the external trigger PMOS transistor. For the proposed SCR, the

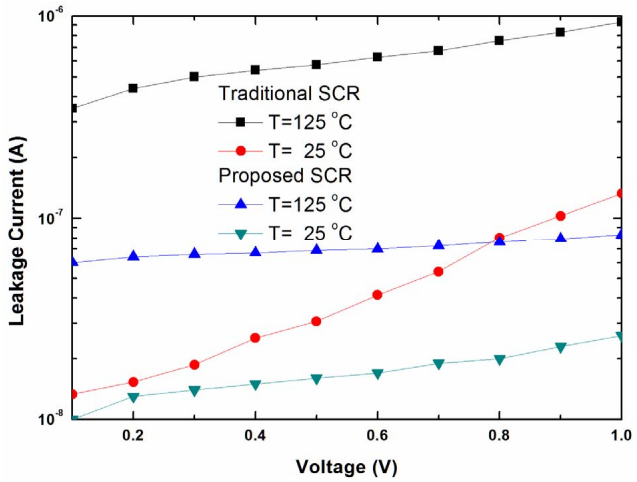

Fig. 7. The measured standby leakage current under different temperatures.

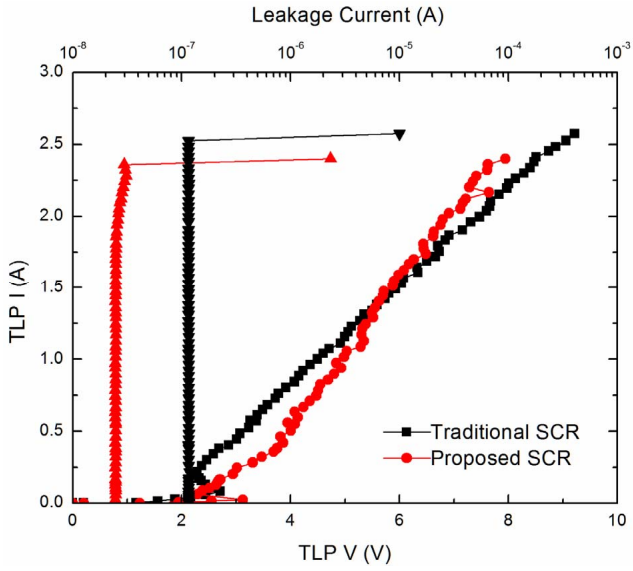

Fig. 8. TLP I-V curves of the measured devices.

leakage current at low temperature is due to gate leakage in the gate-PW overlap, and for high temperature is due to junction leakage in the PW-NW junction.

B. TLP Test

The transmission-line-pulse (TLP) system is used to measure the SCR trigger voltage (V_{t1}), holding voltage (V_h), and maximum current-sustaining ability (I_{t2}). Failure criterion is defined as a leakage current higher than 1μA under 1-V bias.

The TLP measurement results are shown in Fig. 8. The trigger voltage V_{t1} is 2.73V and 3.12V for the traditional and proposed SCRs, respectively. The failure point I_{t2} is 2.57A and 2.39A for the traditional and proposed SCRs, respectively. The holding voltage is roughly ~2V for both devices. The higher I_{t2} and lower V_{t1} for the traditional SCR are attributed to a higher trigger current due to the external trigger transistor. In addition, the leakage current of the traditional SCR is much larger than the leakage current of the proposed SCR due to the

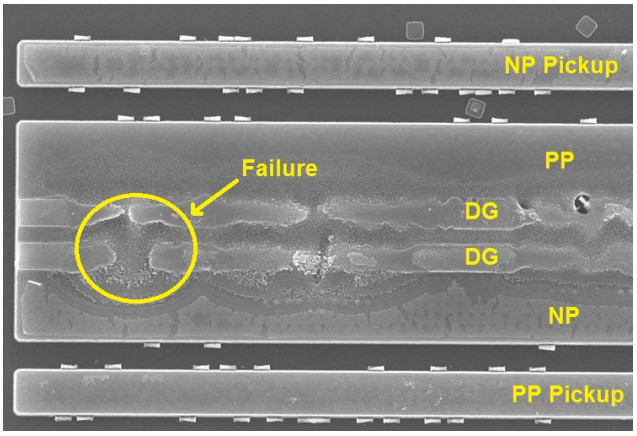

Fig. 9. Failure analysis SEM picture of the proposed SCR after 5kV HBM stress. The damaged regions are highlighted and all located on the SCR device.

external PMOS transistor used to trigger the SCR, which has the gate leakage issue in a 65-nm CMOS process.

C. ESD Robustness

The ESD robustness is measured with the HBM [10] and MM [11] models. The failure criterion is 30% deviation from its original fresh I-V curve. The traditional SCR can pass 5kV HBM and 250V MM, and the proposed SCR can pass 4.5kV HBM and 250V MM. The lower HBM level for the proposed SCR is consistent with the results of the TLP test. Table I summarizes the results of the traditional SCR (Fig. 3) and the proposed SCR (Fig. 6).

D. Failure Analysis

After ESD test, the dies are de-layered to expose the substrate and then analysed by scanning electron microscopy (SEM) to find the failure location. Fig. 9 shows the proposed SCR failure point after 5kV HBM stress. Failure analysis on the traditional SCR shows the failure occurs on the same spot, those are on the SCR device structure. If a higher ESD level was needed, the SCR device width should be enlarged in layout to meet the application specification.

IV. Discussions

The P+ region in the P-well is used as trigger point in the traditional SCR, so it needs enough width to accommodate one or two rows of vias to sink the trigger current. In the proposed SCR the P+ region is floating so it could be drawn smaller, thus reducing the SCR current path and therefore reducing the holding voltage. For the test devices in this work, the area of the P+ region has not been modified in order to only measure the effect of G_1 as trigger transistor. Also, this P+ region cannot be eliminated (thus merging G_1 with G_2), because this way, under normal circuit operation the N-channel formed under G_1 would then make contact with the N+ region connected to V_{SS} and cause some leakage current. Therefore, the spacing between G_1 and G_2 is needed, and to avoid STI formation, the layout arrangement with the P+ region is the best choice.

TABLE I
Measurement Results

Structure	Leakage Current (1V)	TLP		ESD	
		V_{t1}	I_{t2}	HBM	MM
Traditional SCR	116nA	2.73V	2.57A	5kV	250V
Proposed SCR	24nA	3.12V	2.39A	4.5kV	250V

* Leakage current is measured at T=25ºC

V. Conclusion

A new design of power-rail ESD clamp circuit with embedded-trigger SCR device has been proposed and verified. Silicon measurements have verified that the dummy gate used to enhance the turn-on speed of the SCR can be effectively used as trigger transistor, thus reducing silicon area and leakage current. Moreover, TLP test and HBM/MM tests have also confirmed that the ESD robustness is comparable to the traditional design.

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