Impact of Guard Ring Layout on the Stacked Low-Voltage PMOS for High-Voltage ESD Protection

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***Abstract*— Electrostatic discharge (ESD) protection and latchup prevention are two important reliability issues to the CMOS integrated circuits, especially in high-voltage (HV) applications. In this work, the stacked low-voltage (LV) PMOS devices have been successfully verified in a 0.5-μm HV process to provide high ESD level with high holding voltage for HV applications. In addition, the guard-ring layout on the stacked LV PMOS devices was further investigated in silicon chip to get high ESD robustness and latchup-free immunity for HV applications.**

I. Introduction

Electrostatic discharge (ESD) may occur accidentally during the fabrication, package, and assembling processes of IC products, which often caused serious damages on ICs. High-voltage (HV) ICs were found with bad ESD robustness [1]-[2]. Lateral DMOS (LDMOS) was often used as ESD protection device in HV process, but the holding voltage (V_h) of LDMOS after snapback was smaller than the circuit operating voltage (V_{CC}) [3]-[4]. During normal circuit operation, the noise might unpredictably trigger the parasitic BJT of the ESD devices, and the supply voltage (V_{CC}) keeps the parasitic BJT to be continually turned on. Such on-chip ESD device would be burned out after a period of time, under the circuit normal operating condition. Thus, the LDMOS was sensitive to latchup issue.

The typical I-V characteristics of ESD protection devices are illustrated in Fig. 1. Breakdown voltage (V_{BD}) and supply voltage (V_{DD} or V_{CC}) of the internal circuits divide the plot into three parts. The middle part is the desired ESD protection window. The green curve is an example of the desired ESD device's I-V characteristics. To get an effective ESD protection, the trigger voltage (V_{t1}) should be smaller than breakdown voltage of the internal circuits. Furthermore, to avoid latchup issue, the holding voltage (V_h) should be larger than the supply voltage of the internal circuits. The on-resistance of an ESD protection device should be as small as possible to get a high ESD robustness. The I-V characteristics of ESD devices should fit into this window for both effective ESD protection and latchup-free design. Therefore, the stacked configuration of LV devices is a way to achieve a high holding voltage for ESD protection in HV circuits [5]-[7]. The schematic of stacked LV PMOSs for HV ESD protection are illustrated in Fig. 2(a). The holding voltages of stacked LV PMOSs with different stacking numbers can be found in Fig. 2(b). The total holding voltage of stacked PMOSs is the multiple of the holding voltage of single PMOS. The total trigger voltage of stacked PMOSs is also the multiple of the trigger voltage of single PMOS. The secondary breakdown current (I_{t2}) of stacked PMOSs are almost the same in spite of different stacking numbers [8]. Therefore, the trigger voltage and the holding voltage of stacked configuration can be adjusted to meet different HV applications.

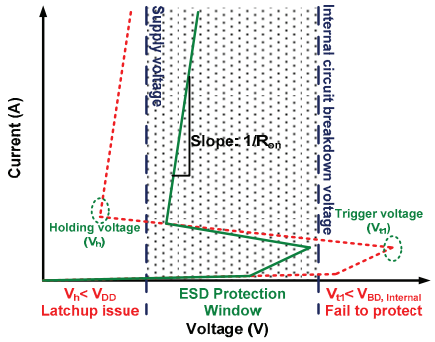
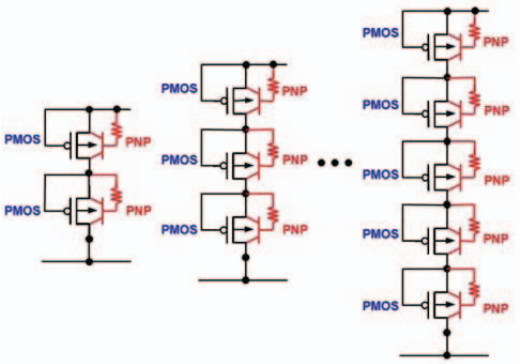
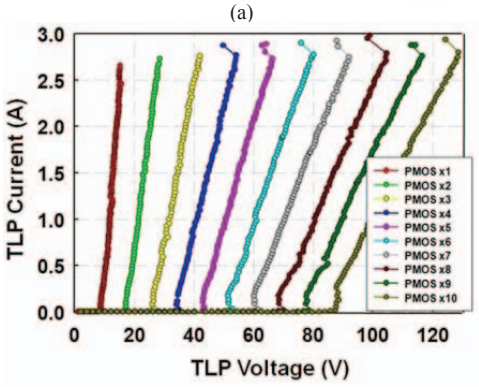


Fig. 1 The I-V characteristics of ESD protection device to meet ESD protection window.



(a)



(b)

Fig. 2 The (a) schematic, and (b) TLP-measured I-V characteristics, of stacked LV PMOSs with different stacking numbers in a HV process [8].

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In addition, the ESD devices should be surrounded by the guard ring in real circuit application. The ESD device without the guard ring can reduce the layout area, but it might cause the latchup issue under the normal circuit operation. During latchup test, the positive or negative current of up to 200mA will be directly applied to the I/O pin [9]. Such latchup-test current will be injected into the substrate through the on-chip ESD device that is often drawn with the I/O pad together to provide ESD protection. Therefore, the on-chip ESD devices were often surrounded by the guard ring to prevent latchup issue in the IC products.

In this work, the stacked LV PMOSs with two or three stacking numbers for HV applications were fabricated and verified in the silicon chip. Especially, different guard ring layouts on the stacked PMOSs were investigated to study its impact to ESD protection performance. The transmission line pulse (TLP) and ESD tester are used to verify the stacked PMOSs with different guard ring layouts for HV applications.

II. Stacked PMOS with Different Guard Ring Layouts

The test structures of stacked PMOSs with different stacking numbers and layout arrangements were fabricated in a 0.5-μm high-voltage process. The stacked LV PMOSs with two and three stacking numbers are investigated in this work, which are designed to meet 20-V and 30-V HV applications. Each LV PMOS in the stacked configuration is drawn with the total channel width of 800μm and a channel length of 0.5μm. The cross-sectional view of stacked structure with two LV PMOSs is shown in Fig. 3. The NWELL spacings of the two LV PMOSs are drawn with 4μm and 8μm in Fig. 3(a) and Fig. 3(b), respectively. The gate of each PMOS is connected to its local high potential point, so each PMOS in the stacked structure is kept in the off state during the normal circuit operation. The P+ diffusion (drain) of the bottom PMOS in the stacked PMOSs is connected to the cathode. The P-ring is connected to the cathode, which is typically biased at ground with the common p-substrate. If the deep N-Well is provided in the process, the P-ring can be isolated to the common substrate.

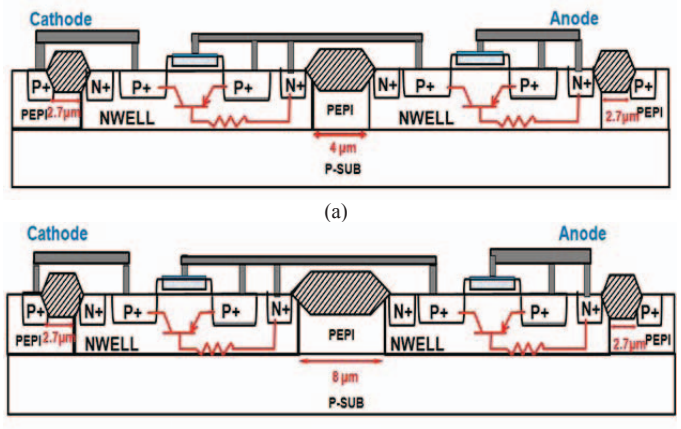

Fig. 3 The cross-sectional views of stacked structure with two LV PMOSs drawn with (a) the NWELL spacing of 4μm and (b) the NWELL spacing of 8μm. Each LV PMOS has its own separated N-well in the stacked structure.

There are four types (type A, type B, type C, and type D) of the guard ring layouts to surround the stacked PMOSs, as shown in Fig. 4, where 3-PMOSs stacked structure is demonstrated. In type A, the stacked PMOSs were not surrounded by P-ring, which is used as the base line for reference. In type B and type C, the stacked PMOSs were surrounded by one P-ring that is typically connected to cathode. The NWELL spacing between each N-well in the type B (type C) is 4μm (8μm). In type D, each PMOS in the N-well of the 3-PMOSs stacked structure was fully surrounded by the P-ring. The clearance of P-ring to the N-well edge is kept at 2.7μm, which is a layout rule specified by the foundry in the given 0.5-μm process.

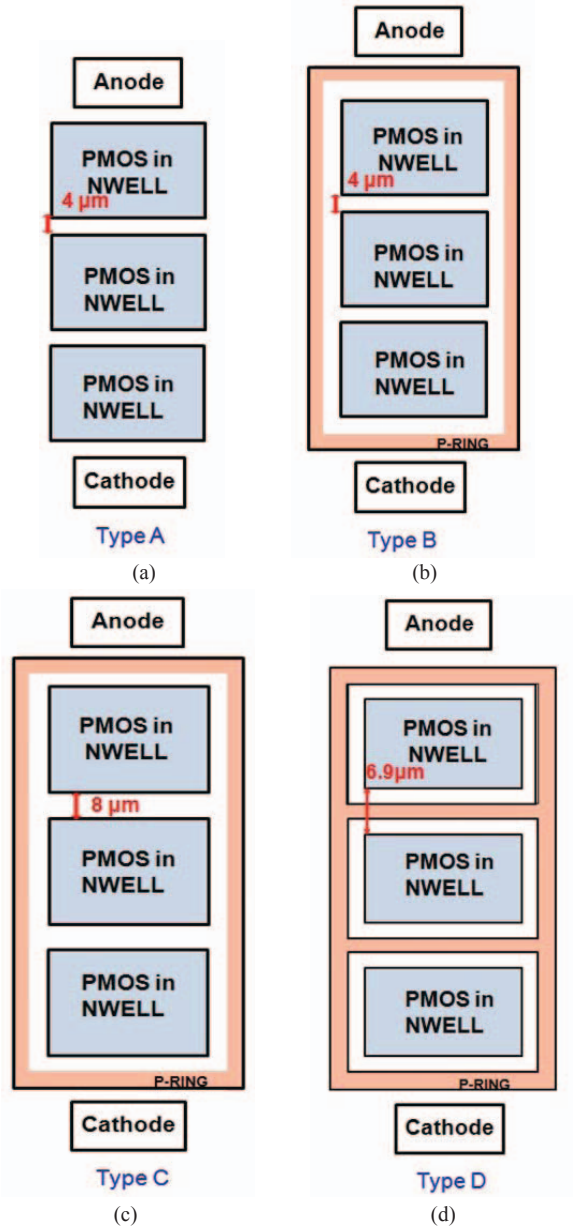

Fig. 4 The four types of guard-ring layout for 3-PMOSs stacked structure, (a) without p-ring, (b) with one whole p-ring and NWELL spacing of 4μm, (c) with one whole p-ring and NWELL spacing of 8μm, and (d) with inserted p-ring to surround each LV PMOS.

III. Experimental Results

All test devices of stacked PMOSs had been fabricated in a 0.5-μm HV process. Each PMOS in all stacked structure is drawn with a channel width of 800μm and a channel length of 0.5μm. Every layout type has 2-PMOSs and 3-PMOSs stacked structures. The TLP-measured I-V characteristics of two stacked PMOSs with the four types of guard ring layout are shown in Fig. 5.

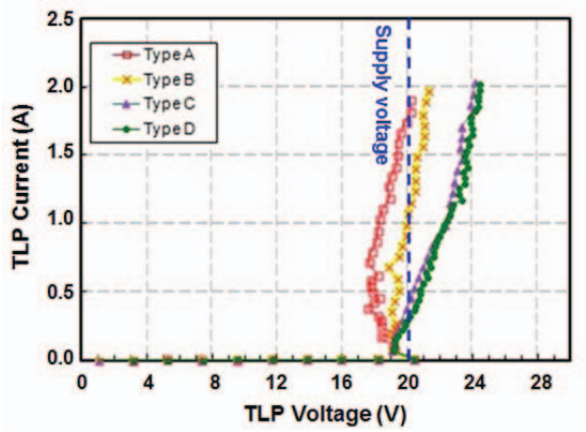

Fig. 5 The TLP-measured I-V characteristics of 2-PMOSs with different guard-ring layouts.

In Fig. 5, the holding voltage of 2-PMOSs stacked structure is two times of the holding voltage of single PMOS. The trigger voltage of 2-PMOSs stacked structure is also double of the trigger voltage of single PMOS in TLP measurement. In Fig. 5, the trigger voltages of the 2-PMOSs stacked structure with different guard-ring layouts are almost the same, but the holding voltage of type A is smaller than those of other types. Type B is better than type A, because it adds one guard ring to surround itself. The holding voltage of type B still suffers latchup risk for 20V application. The holding voltages of type C and type D are better (higher) than that of type A and type B, and they can achieve latchup-free design for 20V application. However, the layout area of type D is smaller than the layout area of type C, as well as the type D has the best I_{t2} among all guard-ring types.

The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table I. The breakdown voltages of type C and type D are almost the same as those of type A and type B in DC measurement. All of 2-PMOSs stacked structure with different guard-ring types can pass 3.5 kV in the human-body-model (HBM) ESD test and 250 V in the machine-model (MM) ESD test.

TABLE I
Summary of 2-PMOSs stacked structure with different guard-ring types

2-PMOSs Stacked Structure	TLP (100-ns)			DC	ESD Level	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	20.4	17.59	1.82	22.3	3.5	250
Type B	20.4	18.87	1.89	22.3	3.5	250
Type C	20.36	19	1.94	22.6	3.5	250
Type D	20.37	19.1	1.98	22.6	3.5	250

The TLP-measured I-V characteristics of three stacked PMOSs with the four types of guard ring layout are shown in Fig. 6. As seen in Fig. 6, the trigger voltage of 3-PMOSs stacked structure is triple of the trigger voltage of single PMOS. In Fig. 6, the trigger voltages in different guard-ring types are almost the same, but the holding voltage of type A is still the smallest among the four types of guard ring layout. Type A and type B would suffer latchup risk for 30V high voltage application. The holding voltages of type C and type D are better (higher) than those of type A and type B, which can achieve latchup-free design for 30V application. The total layout area of type D is also smaller than that of type C, as well as the type D has the best I_{t2} among the four guard-ring types.

The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table II. The breakdown voltages of all guard-ring types almost have the same value. The MM ESD level (300V) of type C and type D are better than that (250V) of type A and type B. Except type A, all layout types of 3-PMOSs stacked structure can pass 3.5 kV in the HBM ESD test.

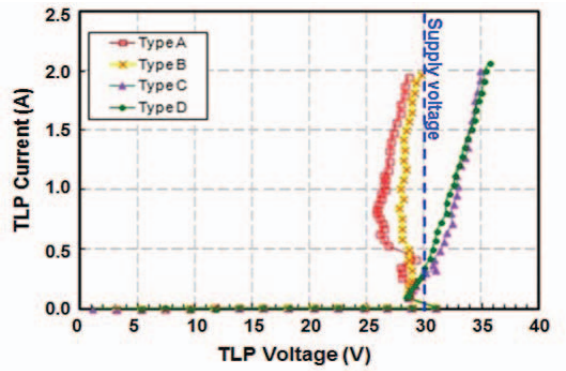

Fig. 6 The TLP-measured I-V characteristics of 3-PMOSs with different guard-ring layouts.

TABLE II
Summary of 3-PMOSs stacked structure with different guard-ring types

3-PMOSs Stacked Structure	TLP (100-ns)			DC	ESD Level	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	30.99	25.9	1.87	30.7	3	250
Type B	31.01	27.84	1.9	30.5	3.5	250
Type C	31.02	28.53	1.92	30.7	3.5	300
Type D	31.02	28.43	2	30.7	3.5	300

From above results with TLP-measured I_{t2} and ESD test, the type D among the four types of guard-ring layout is the best choice for the stacked PMOSs structure for HV ESD protection. The TLP-measured I-V characteristics of the stacked 2-PMOSs and 3-PMOSs with the guard-ring layout of type D are compared in Fig. 7. As seen in Fig. 7, the holding voltage can be linearly increased in the PMOSs stacked structure by adjusting the stacking number. The trigger voltage can also be linearly increased in the PMOSs stacked structure. Moreover, the I_{t2} of PMOSs stacked structure with different stacking numbers can be kept almost the same. Different stacking numbers on the stacked PMOSs can be

adjusted for various HV applications to achieve latchup-free immunity on the ESD protection device.

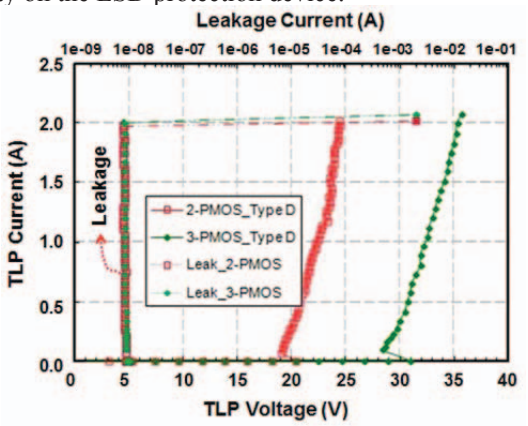

Fig. 7 The TLP-measured I-V characteristics of the stacked 2-PMOSs and 3-PMOSs with the guard-ring layout of type D.

IV. Applications

A typical whole-chip ESD protection scheme is shown in Fig. 8. The ESD stresses on each I/O pin have four stress modes of pin combination with the relatively grounded GND pin or VDD/VCC pin [10]. The ESD stresses could also happen from the VCC pin to the GND pin with positive or negative voltage pulses [10]. Stacked PMOSs can be the ESD protection cells at the input or output pads or the power-rail ESD clamp between the VCC/GND power lines.

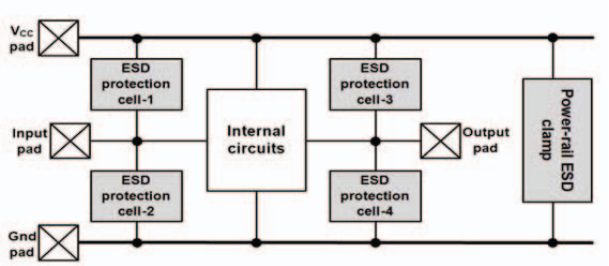

Fig. 8 A typical whole-chip ESD protection scheme. The stacked PMOSs can be placed as the ESD protection cells and the power-rail ESD clamp.

If the stacked PMOSs are used as ESD protection cell-2 or ESD protection cell-4 in Fig. 8, the P-ring should be connected to GND. The ESD current gets through stacked parasitic PNPs in the PS (positive-to-VSS) ESD-stress mode, and gets through forward diode in the NS (negative-to-VSS) ESD-stress mode. The parasitic PNP path in each PMOS is also drawn in Fig.3. The diode path exists from the P+ diffusion of P-ring to the N+/NWELL of the top PMOS that connected to anode. If the stacked PMOSs are used as ESD protection cell-1 or ESD protection cell-3, the P-ring should be separated from the cathode of the bottom PMOS, and connected to GND to avoid the leakage current under the normal circuit operation. In that situation, ESD current in the PD (positive-to-VDD/VCC) ESD-stress mode flows through several forward diodes, where the diode path exists from the P+ diffusion (drain) to the N+/NWELL in each PMOS device structure. The ESD current in the ND (negative-to-VDD/VCC) ESD-stress mode flows through stacked parasitic PNPs. Stacked PMOSs can also be used as the power-rail ESD clamp. When stressing a positive ESD pulse on VCC, the current gets through stacked parasitic PNPs in the stacked PMOSs. By stressing a negative ESD pulse at VCC, the current gets through forward diode (P-ring to the N+/NWELL of the top PMOS).

V. Conclusion

Stacked PMOSs with different guar-ring layouts has been investigated in a 0.5-μm HV process for HV applications. From the measurement results, the stacked PMOSs with guard-ring layout of type D can achieve both of good ESD robustness and high latchup-free immunity with reasonable total layout area. By adjusting the stacking numbers of stacked PMOSs, it can provide effectively ESD protection for various HV applications. To meet much higher voltage applications, the deep N-Well structure with light doping concentration should be applied to surround each LV PMOS. The stacked configuration of LV devices with optimized guard-ring layout is recommended for on-chip ESD protection design in HV IC products.

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